

Hot Air Solder Levelling (HASL) Process Parameter Optimization for SN100CL

By

Fatin Afeeqa Mohd Sobri (1430411393)

A thesis submitteed in fulfillment of the requirements for the degree of Master of Science in Materials Engineering

School of Material Engineering UNIVERSITI MALAYSIA PERLIS

UNIVERSITI MALAYSIA PERLIS

	DECLARATION OF THESIS
Author's full name :	Fatin Afeeqa Binti Mohd Sobri
Date of birth :	15 May 1990
Title :	"Hot Air Solder Levelling (HASL)" Process Parameters Optimization for SN100CL
Academic Session :	2014/2015
I hereby declare that the the at the library of UniMAP. The	esis becomes the property of Universiti Malaysia Perlis (UniMAP) and to be placed
at the library of Offinant . Th	is triesis is classified as .
CONFIDENTIAL	(Contains confidential information cinder the Official Secret Act 1972)*
RESTRICTED	(Contains restricted information as specified by the organization where research was done)*
OPEN ACCESS	I agree that my thesis is to be made immediately available as hard copy or on-line open access (full text)
	on to the UniMAP to reproduce this thesis in whole or in part for the purpose of ange only (except during a period of years, if so requested above).
, , , , , , , , , , , , , , , , , , , ,	.6
	Certified by:
.×2	
SIGNATUR	SIGNATURE OF SUPERVISOR
900515-07-5	Ascc. Prof. Dr. Che Mohd Ruzaidi Ghazali
(NEW IC NO. / PAS	
Date :	Date :
11	

NOTES: * If the thesis is CONFIDENTIAL or RESTRICTED, please attach with the letter from the organization with period and reasons for confidentially or restriction.

APPROVAL AND DECLARATION SHEET

This thesis titled "Hot Air Solder Levelling (HASL)" Process Parameter Optimization for SN100CL was prepared and submitted by Fatin Afeeqa binti Mohd Sobri (Matric Number: 1430411393) and has been found sasticfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the award of degree Master of Science (Materials Engineering) in University Malaysia Perlis (UniMAP).

Check and Approved by

(ASSOCIATE PROFESSOR DR. CHE MOHD RUZAIDI GHAZALI)

Project Supervisor

School of Materials Engineering

University Malaysia Perlis

(Date:)

School of Materials Engineering

2016

University Malaysia Perlis

ACKNOWLEDGEMENT

I would like to take this opportunity to acknowledge those who have provided me with help along the way to complete this dissertation during my studies at the School of Materials Engineering, University Malaysia Perlis.

A special thanks goes to my helpful supervisor Associate Professor Dr. Che Mohd Ruzaidi Ghazali. The supervision and support that he gave truly help the progression and smoothness of the project work. The time spends and co-operation is greatly appreciated. His enthusiasm for electronic technology has always invigorated me with a desire to explore more on this area of field. He has guided me with constant encouragement and invaluable suggestion which is the key to success of this project.

I am also grateful to my co-supervisor, Mr. Pavithiran Narayanan from Nihon Superior Co. Ltd. and also to Mr. Mohd Arif Anuar Mohd Salleh for their patient guidance, constant encouragement and invaluable suggestions for my research work. I wish to express my gratitude to School of Materials Engineering and Nihon Superior Co. Ltd. Research and Development Department staffs for their arrangement and assistance as to accomplish my project. Their technical information has helped me to complete this project without facing many troubles. The skills and learning process during the project will be nothing without the keenness and help from them.

A big thank also dedicated to my friends and fellow course mates, especially under the same supervisor for their helpful advices and cooperation throughout this project. Most importantly, I am eternally grateful to my family for their continuous support, understanding and love.

TABLE OF CONTENT

		PAGE
THES	SIS DECLARATION	i
ACK	NOWLEDGEMENT	ii
TABI	LE OF CONTENT	iii
LIST	OF TABLES	vii
	OF FIGURE	ix
	of Figure	
LIST	OF ABBREVIATIONS	xiii
LIST	OF SYMBOLS	xiv
ABST	OF TABLES OF FIGURE OF ABBREVIATIONS OF SYMBOLS TRAK TRACT PTER 1 INTRODUCTION Background Problem Statements Aims and Objectives	xvi
ABST	TRACT	XV
	0.	
CHAI	PTER 1 INTRODUCTION	
	De de servicio	1
1.1	Background	1
1.2	Problem Statements	3
1.3		4
1.4	Work Scope	5
1.5	Thesis Outline	6
	is a second of the second of t	
CHAI	PTER 2 LITERATURE REVIEW	
2.1	Soldering in Electronic Packaging Area	7
2.2	Lead-Based Solder	8
2.3	Solder Joint Reaction	9
2.4	Legislation of Pb Solder	12
2.5	Factors Affecting Interfacial IMC Reaction	13
	2.5.1 Thermal Exposure	13
	2.5.2 Elements Compositions	14
	2.5.3 Activation Energy	15

2.6	Surface Finish	18
	2.6.1 Function	19
	2.6.2 Solderability	20
	2.6.3 Surface Finish Alternatives	21
2.7	Hot Air Solder Levelling (HASL)	23
	2.7.1 HASL Process	24
	2.7.2 Advantages and Disadvantages	25
2.8	HASL Issues	27
	2.8.1 Wettability	27
	2.8.2 Oxidation	28
	2.8.3 Coating Surface Planarity	30
	2.8.4 Shelf Life	32
	 2.8.1 Wettability 2.8.2 Oxidation 2.8.3 Coating Surface Planarity 2.8.4 Shelf Life 	
СНА	APTER 3 MATERIALS AND EXPERIMENTAL PROCEDU	RES
3.1	Experimental Work Overview	33
3.2	Phase I: Relationship between Solderability and Free Solder Thickness	33
3.3	Phase II: HASL Process Parameter Optimization	34
3.4	Raw Materials	37
3.5	Solderability Investigation	38
	3.5.1 Methods, Equipment and Measurement Procedures	38
	3.5.2 Gen3 Wetting Balance Test	38
,	3.5.3 Solder Bath Method	41
	3.5.4 Globule Method	42
3.6	Flux Preparation	43
3.7	Sample Preparation	44
	3.7.1 Solder Fabrication	44
	3.7.2 Free Solder Removal	45
3.8	Testing	46
	3.8.1 Reflow	46
	3.8.2 Aging test	46

3.9	Measurement Procedures	47
3.10	HASL Machine Operation	49
	3.10.1 PCB Design	49
	3.10.2 Parameter Optimization	51
3.11	Microsection and Microstructure	52
	3.11.1 Sample preparation	52
3.12	SEM Observations	53
3.13	Microstructure Analysis	53
СНА	PTER 4 RESULTS AND DISUSSIONS Introduction	
4.1	Introduction	55
4.2	Relationship between Solderability and the Free Solder Thickness	55
	4.2.1 Effect of Dipping Time	55
	4.2.2 Free Solder Removal	60
4.3	4.2.2 Free Solder Removal Effect of Aging 4.3.3 Microstructure	62
	4.3.3 Microstructure	62
	4.3.2 Thickness Measurement	66
	4.3.3 Activation Energy	69
	4.3.4 Solderability Evaluation	72
	4.3.5 Correlation between Free Solder and IMC Thickness	74
4.4	HASL Process Parameter Optimization	75
	4.4.1 Solder Compositions	75
(4.4.2 Solder Alloy Preparation	76
`	4.4.3 Yellowing Effect Test	77
	4.4.4 Dipping Test	79
	4.4.5 Globule Test	81
	4.4.6 Microstructure Observation	82
	4.4.7 Optimum Compositions Analysis	86
4.5	Parameters Optimization	89
4.6	HASL Coating	88
4.7	Comparison Analysis	98

CHAPTER 5 CONCLUSIONS AND RECOMMENDATIONS

5.1	Conclusion	102
5.2	Recommendations	104
REF	ERENCES	105
APP	ENDIX	111
LIST OF PUBLICATIONS		114

This item is protected by original copyright

LIST OF TABLES

NO		PAGE
2.1	Tin-lead in printed circuit board (Trumble, 1998).	9
2.2	The comparison on activation energy (Q) by different solder and soldering methods.	17
2.3	The advantages and disadvantages of current surface finish (Song & Liu, 2003).	22
2.4	Benefits and limitation of HASL finish (Roberts & Johal, 2007).	26
2.5	Thickness range of common Pb-free HASL deposits (Roberts & Johal, 2007).	32
3.1	Description of raw materials use in the research experiment.	37
3.2	Tin-alloy compositions.	37
3.3	Parameter setting for dipping process by Gen3 wetting balance test.	41
3.4	Parameter setting for dipping process by Gen3 wetting balance test.	43
3.5	Time sequence of test operation of Gen3 machine.	48
3.6	HASL machine parameter and descriptions.	51
4.1	IMC thickness, free solder thickness and total coating thickness measurement for 20 s, 60 s, 120 s, 180 s and 240 s of dipping time.	58
4.2	The n values and k values at 120 °C, 150 °C and 180 °C.	70
4.3	Analysed results of solder alloy used in Gen3 wetting balance test machine.	76
4.4	Overall results of solderability test by Gen3 wetting balance test showing the best of wetting time and maximum force.	87
4.5	Overall results of yellowing effect test and Gen3 dipping test.	87
4.6	HASL machine process parameters and capability.	88
4.7	Ideal cross section coating layer for Area 1, 2 and 3 with the area dimension.	99
4.8	Overall results from HASL process for Area 1, 2 and 3.	100

LIST OF FIGURES

NO		PAGE
1.1	HASL surface finishes coating layer illustration, International Circuit Inc. (2012).	3
2.1	The growth thickness (X) of the IMCs formed during the Sn3.5Ag0.5Cu/Ag interfacial reactions at various temperatures as a function of the square root of reaction time (t ^{1/2}) (Wu et al., 2011).	14
2.2	Backscattered SEM micrographs of cross-sectional view of Sn= 3.0 Ag=0.5Cu= xTiO2 solder joints aged at 190°C for 240 h; (a) x = 0.0, (b) x = 0.02, (c) x = 0.05, (d) x = 0.1, (e) x = 0.3, and (f) x = 0.6 wt.% (Tang et al., 2014).	15
2.3	HASL application in electronic industries as compared to other finishes (Kellner, 2004).	24
2.4	HASL process flow chart (Song & Liu, 2003).	25
2.5	XPS-Cu spectra of the uppermost layer of the surface (Ramireza et al., 2011).	29
3.1	Flow cart of research work.	36
3.2	Gen3 wetting balance test machine and computer controller.	40
3.3	Evaluation of wetting curve.	40
3.4	Gen3 wetting balance test in solder bath mode.	41
3.5	Gen3 wetting balance test in globule mode.	43
3.6	Calculation chart for mixing of solder.	45
3.7	Experimental setup for etching process.	45
3.8	Reflow profile for SN100CL solder.	46
3.9	Time sequence explanation figure of test operation items.	48
3.10	Illustration of designed FR4 PCB for HASL machine operation.	50
3.11	Images showing the (a) solder bar and (b) HASL machine.	52

3.12	Image from J-image software showing the area of measuring the layer thickness.	54
4.1	SEM image showing the solder coating on copper strips surface with (a) 20 s, (b) 60 s, (c) 120 s, (d) 180 s, and (e) 240 s of dipping time.	57
4.2	Thickness of IMC, total solder coating and free solder at different dipping time.	59
4.3	SEM observation of IMC for as soldered samples at 2500X magnification.	60
4.4	Globule wetting test result from Gen3 wetting balance test for etched specimens.	62
4.5	Schematic diagram showing the coarsening of IMC grain. Growth of interfacial IMC after aging for 120°C for	64
4.6	Growth of interfacial IMC after aging for 120°C for (a) 24 hours, (b) 120 hours and (c) 240 hours.	65
4.7	Growth of interfacial IMC after aging for 150°C for (a) 24 hours, (b) 120 hours and (c) 240 hours.	65
4.8	Growth of interfacial IMC after aging for 180°C for (a) 24 hours, (b) 120 hours and (c) 240 hours.	66
4.9 (a)	Graph of interfacial IMC (µm) versus aging time (hours).	67
4.9 (b)	Graph of free solder thickness (µm) versus aging time (hours).	68
4.10	The relationship between interfacial IMC thickness (μm) and aging time (h).	71
4.11	Arrhenius plot for the growth of interfacial IMC of SN100CL solder.	71
4.12	Wetting time (t) of SN100CL coated copper strips with different free solder thickness (μ m)	73
4.13	Maximum force (mN) of SN100CL coated copper strips with different free solder thickness (μm).	73
4.14	Correlation between free solder (μm) and IMC layer thickness (μm).	75
4.15	OM micrograph of coated copper strips of (a) before reflow and after reflow with Ge compositions of (b) 0 wt% (c) 0.002 wt% (d) 0.006 wt% (e) 0.010 wt% and (f) 0.020 wt%	78
4.16	Graph of wetting time for 0 wt%, 0.00 wt2%, 0.006 wt%, 0.010 wt% and 0.020 wt% of Ge by dipping test.	80

4.17	Graph of maximum force for 0 wt%, 0.002 wt%, 0.006 wt%, 0.010 wt% and 0.02 wt% of Ge by dipping test.	80
4.18	Wetting time of 0 wt%, 0.002 wt%, 0.006 wt%, 0.010 wt% and 0.020 wt% of Ge in globule test method.	81
4.19	Maximum force of 0 wt%, 0.002 wt%, 0.006 wt%, 0.010 wt% and 0.020 wt% of Ge in globule test method.	82
4.20	SEM micrograph showing the interfacial IMC growth for Sn-0.7Cu-0.05 Ni with aging temperature of (a) 24 hours (b) 120 hours (c) 240 hours.	83
4.21	SEM micrograph showing the interfacial IMC growth for Sn-0.7Cu-0.05 Ni with aging temperature of (a) 24 hours 120 hours (c) 240 hours and Sn-0.7Cu-0.05Ni-0.006Ge at aging temperature of (d) 24 hours (120) hours and (f) 240 hours.	84
4.22 (a)Interfacial IMC thickness measurement and (b) free solder thickness measurement for Sn-0.7Cu-0.05Ni and Sn-0.7Cu-0.05Ni-0.006Ge solder.	85
4.22 (b)Free solder thickness measurement and (b) free solder thickness measurement for Sn-0.7Cu-0.05Ni and Sn-0.7Cu-0.05Ni-0.006Ge solder.	86
4.23	Designed PCB with cross section area 1, 2 and 3.	89
4.24 (i)SEM micrograph of HASL cross section Area 1 for 2 seconds with level time of (a) 3 seconds, (b) 4 seconds, (c) 5 seconds and (d) 6 seconds.	90
	ii)SEM micrograph of HASL cross section Area 1 for 3 seconds with level time of (a) 3 seconds, (b) 4 seconds, (c) 5 seconds and (d) 6 seconds.	91
4.25 (i)SEM micrograph of HASL cross section Area 2 for 2 seconds with level time of (a) 3 seconds, (b) 4 seconds, (c) 5 seconds and (d) 6 seconds.	93
4.25 (ii)SEM micrograph of HASL cross section Area 2 for 3 seconds with level time of (a) 3 seconds, (b) 4 seconds, (c) 5 seconds and (d) 6 seconds.	92
4.26 (ii)SEM micrograph of HASL cross section Area 3 for 2 seconds with level time of (a) 3 seconds, (b) 4 seconds, (c) 5 seconds and (d) 6 seconds.	93

4.26 (i	i)SEM micrograph of HASL cross section Area 3 for 3 seconds	
	with level time of (a) 3 seconds, (b) 4 seconds, (c) 5 seconds and (d) 6 seconds.	94
4.27	Evaluation of HASL coating board showing the (a) wetting time and (b) maximum force.	97

This item is protected by original copyright

LIST OF ABBREVIATION

Cu Copper

ENIG Electroless Nickel Immersion Gold

Ge Germanium

HASL Hot Air Solder Levelling

ImmAg Immersion Silver

ImmTin Immersion Tin

IPA 2-Propanol / Isopropyl Alcohol

JIS Japanese Industrial Standard

Ni Nickel

OM Optical Microscope

OSP Organic Solderability Preservative

OPS Oxide Polishing Suspension

PCB Printed Circuit Board

PLCC Plastic Leaded Chip Carrier

QFP Quad Flat Package

ROHS Reduction of Hazardous Substrate

SEM Scanning Electron Microscope

SMT Surface Mount Technology

SOIC Small Outline Integrated Circuit

Sn Tin

UBM Underbump Metallurgy

XPS X-ray Photooelecron spectroscopy

LIST OF SYMBOLS

t Time

Q Activation Energy

Pb Lead

oThis item is protected by original copyright

Proses Mengoptimum Parameter "Hot Air Solder Levelling" (HASL) untuk SN100CL

ABSTRAK

Pembungkusan elektronik yang boleh dipercayai kini menjadi faktor paling kritikal dalam industri elektronik. Ramalan kegagalan pateri dan jangka hayatnya menjadi lebih mencabar kerana permintaan yang semakin tinggi untuk prestasi yang lebih bagus dalam peranti elektronik. Dalam pembungkusan elektronik, kemasan permukaan memainkan peranan penting untuk proses pematerian dan pemasangan Kajian ini dilakukan untuk menentukan kebolehbasahan oleh permukaan penyalutan SN100CL dan proses mengoptimumkan parameter mesin Hot Air Solder Levelling (HASL). Kajian ini dibahagikan kepada dua fasa. Fasa pertama adalah untuk mengkaji hubungan diantara kebolehbasahan terhadap jumlah ketebalan lapisan, ketebalan pateri yang tidak bertindakbalas dan sebatian antara logam (IMC). Fasa kedua pula adalah kajian komposisi yang berbeza pada elemen Germanium (Ge) dalam pateri SN100CL. Lima komposisi Ge berbeza yang digunakan adalah 0 wt%, 0.002 wt%, 0.006 wt%, 0.010 wt% and 0.020 wt% dalam pateri Sn-0.7Cu-0.05Ni. Kajian ini menunjukkan kesan kebolehbasahan salutan SN100CL dengan perbezaan komposisi Ge. Kaedah ujian imbangan kebolehbasahan oleh Gen3 digunakan untuk menilai tahap kebolehbasahan. Kualiti kebolehbasahan dinilai dengan perbandingan relatif dengan masa pembasahan dan daya kebolehbasahan maksimum terhadap permukaan salutan. Didapati bahawa masa membasahkan adalah lebih lama dan daya maksimum pembasahan adalah lebih rendah dengan mengurangkan ketebalan pateri yang tidak bertindakbalas yang disebabkan oleh pertumbuhan lapisan IMC yang telah menghasilkan permukaan yang tidak boleh dibasahkan. Selain daripada itu, komposisi 0.006 wt% Ge merupakan komposisi terbaik dalam solder SN100CL. Keputusan ini ditentukan dengan salutan SN100CL yang telah didedahkan kepada proses pateri balikan dan penuaan. Ketebalan IMC dan ketebalan pateri yang tidak bertindak balas oleh 0 wt% dan 0.006 wt% dikaji menggunakan Mikroskop Imbasan Elektron (SEM) dan keputusan menunjukkan bahawa IMC daripada 0 wt% adalah lebih tinggi berbanding 0.006 wt% Ge. Seterusnya, pateri aloi Sn-0.7Cu-0.05Ni-0.006Ge telah digunakan dalam proses HASL. Proses mengoptimumkan parameter telah dijalankan dan salutan HASL yang terbaik diperhatikan menggunakan SEM. Secara keseluruhannya, kebolehbasahan telah dipengaruhi oleh lapisan pateri yang tidak bertindakbalas dan 0.006 wt% Ge merupakan komposisi terbaik dalam proses HASL dengan parameter 2 saat untuk masa statik dan 5 saat masa celupan.

"Hot Air Solder Levelling (HASL)" Process Parameters Optimization for SN100CL

ABSTRACT

Reliability of electronic packaging has now become the most critical factor in electronic industries. The prediction of solder joint failure and its shelf life becomes more challenging as the increasing demand for superior performance of electronic devices. In electronic packaging, surface finish plays an important role for soldering and assemblies process. This study was made to determine the solderability of SN100CL coating surface and optimized the Hot Air Solder Levelling (HASL) process parameters. This research work was divided into two phases. The first phase is to study the relationship between solderability and the total coating thickness, free solder thickness and interfacial intermetallic compound (IMC). The second phase was the investigation of different composition of Germanium (Ge) in SN100CL solder. Five different composition of Ge used are 0 wt%, 0.002 wt%, 0.006 wt%, 0.010 wt% and 0.020 wt% in Sn-0.7Cu-0.05Ni solder alloy. This research reveals the effect on solderability of SN100CL coating with different Ge compositions. Gen3 wetting balance test method was used to evaluate the solderability. The quality of wetting was evaluated by relative comparison on the wetting time and maximum wetting force exerted on the coated copper surface. It was found that the wetting time was longer and the maximum wetting force was lower with decreasing of free solder thickness layer due to growth of interfacial IMC layer and produced less wettable surface of solder coating. Apart from that, 0.006 wt% of Ge was observed to have the best composition of Ge in SN100CL solder. The results was determined with SN100CL coated surface when introduced to reflowed and aged conditions. The IMC and free solder thickness of 0w wt% and 0.006 wt% was observed under Scanning Electron Microscope (SEM) and the results shows that IMC of 0 wt% Ge growth higher compared to 0.006 wt% of Ge. Sn-0.7Cu-0.05Ni+0.006Ge solder alloy was then deployed in HASL process. The parameter optimization was performed and the good HASL coating was observed under SEM. Overall, the solderability are found to be affected by free solder thickness and 0.006 wt% of Ge shows the best composition in HASL process with 2 seconds and 5 seconds of dwell time and level time respectively.

CHAPTER 1

INTRODUCTION

1.1 Background

Solder plays a crucial role in assembly and interconnection of electronic products. As an interconnection, solders provide electrical, thermal and mechanical functions. Environmentally conscious manufacturing is becoming a very important objective for the electronics industry. It is highly desirable to minimize the environmental impact of electronic manufacturing processes. The electronics industry is being forced to eliminate lead from products, due to the undeniable evidence of lead toxicity (Sun et al., 2007).

Lead-free soldering has become one of the most important trends in recent years in the electronics industry due to worldwide environmental and health concerns. All soldering materials must be lead-free, including the solders as well as the surface finishes that are used on the pads of printed circuit boards (PCB) and underbump metallurgy (UBM) on the chip side. Copper is commonly used as the base metal of the soldering pads on PCBs because of its good wetting property with solder. Today, more lead-free surface finishes have been investigated and applied on the Cu base metal of the soldering pads, such as organic solderability preservative (OSP) and electroless nickel immersion gold (ENIG) (Zhang et al., 2009).

The development and minimizing trends of microelectronic packaging technology triggers the component to be smaller and the density of the integrated circuit grows higher. It is now a trend of having smaller gadgets as an urban lifestyles. Continuing the miniaturization the microelectronic components have make the solder joint and its performance becomes the primary focus while choosing the solder and soldering techniques. The processability and manufacturing of the components should be considered regardless of its commercial perspective. With the development of microelectronic packaging technology, components are getting ever smaller and the density of integrated circuits grows higher. It is necessary to understand the mechanical behaviour of the solder alloy for a high reliability of the electronic devices (Kumar et al., 2013; Plumbridge et al., 2004).

Apart from miniaturizing the components and devices, the solder components itself are critical factors that determining the solder joint reliability. Properties such as non-toxicity and non-harmful to the environment are now being resolute by the researchers. A product will be considered lead-free when any of the individual materials used to construct it, contains less than 0.1 percent lead. PCB is the foundation of all kinds of electronic devices ranging from cell phone, personal computer to military products. The surface finish of PCB is one of the key factors which has a significant influence on its reliability performance (Yan et al., 2013).

The significant of solder deploy in assemblies are as important as the surface finish of the PCB. The insufficient of PCB with surface finish coating are correspond to the demands of electronic products as it is being produced more and more every day. These demands are increasing and pressuring the performance of surface finish to

continue to operate under extremely harsh environmental conditions. As a results, the precision in choosing the surface finish is important. The criteria of choosing the best PCB surface finish should be considered on its shelf life and the cleanliness on the surface (Toscano & Long, 2014). According to Wayne and Sweatman (2012), Hot Air Solder Levelling (HASL) finish was one of the popular finishing due to its long shelf life and low cost compared to other finishes such as electroless nickel immersion gold (ENIG), immersion silver (Ag) and immersion tin (Sn). Figure 1.1 shows the HASL surface finish coating layer on PCB. The HASL coating layer is on top of the copper substrate. An interfacial IMC layer are formed between the surface finish layer and copper substrate.

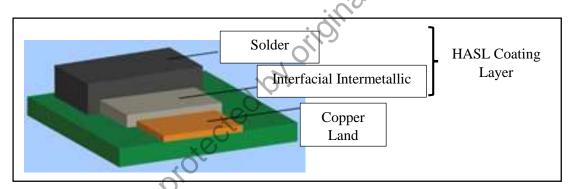


Figure 11: HASL surface finishes coating layer illustration, International Circuit Inc. (2012).

1.2 Problem statement

Despite the wide use of HASL finish in coating of PCB, the coating thickness that are required to ensure good solderability are not well studied. HASL finish provide excellent shelf life, shorter solder wetting times in assembly and the formation of an intermetallic bond prior to the assembly process. However, the issues arise in HASL finish including solderability, oxidation, surface planarity and shelf life is still not fully

solved and other surface finish becomes competitive in the electronic area. With a very thin solder coating, HASL finish may face a high risk in dewetting which then lead to electric circuit failure. Thus, SN100CL is a new solder in market and yet the properties of HASL process have not been fully explored. It is important to understand the properties of SN100CL HASL coating relating to its solderability performance. This includes in understanding the effect of interfacial IMC growth and free solder thickness to its solderability performance and determining the best Ge content levels in the compositions. The ability of molten solder to react with the substrate at the interface of solder and substrate to form a certain amount of interfacial IMC are referred as wetting.

SN100CL solder is a superior type of surface finish solder on the PCB with composition of Sn-0.7Cu-0.05Ni-0.01Ge. However, there is not much experience or confidence in the use of the SN100CL HASL process and the information on the shelf life is very limited. The composition of SN100CL that having the superior characteristics are not being distinguish as the composition previously in a large range of percentage. The problem occurs is the coating thickness is too thin to provide solder free area for soldering process. Since the interactions determine the shelf life of the PCB, the HASL coating on the copper area are required to be determined.

1.3 Objectives

This study will focus on several objectives listed as below:

 To investigate the optimum SN100CL HASL coating thickness for excellent solderability. This includes in understanding the effect of the total coating thickness, free solder thickness and interfacial intermetallic layer to the solderability performance.

- To determine the effect of accelerated aging to the growth of IMC in SN100CL ii. coating.
- iii. To identify the effect of Ge content in Sn-0.7Cu-0.05Ni solder to the coating solderability performance.
- iv. To optimize the HASL coating parameters using actual HASL coating machine inal copyrids for SN100CL HASL coating application.

1.4 Work Scope

In this study, the coating thickness that is required for a good solderability will be conducted using Gen3 wetting balance test. In phase I of study, initial coating process optimization of coating dipping time using copper strips with dimension of 10 mm (length) X 3 mm (width) X 0.3 mm (thickness). For determining the relationship between interfacial IMC, free solder thickness and coating thickness, accelerated aging test are conducted and cross section were observed under SEM. The thickness of interfacial IMC, free solder thickness and coating thickness are measured by J-image software. A plotted graph is constructed to observe the relationship of the thickness versus aging time.

In phase II of experiment, the best composition of Ge are determined by using a range of Ge composition which are 0 wt%, 0.002 wt%, 0.006 wt%, 0.010 wt% and 0.020 wt%. The best solder compositions are deploy in HASL machine and the thickness of the solder coating are visually observed and further observe are conducted under SEM observation. To support the results from SEM cross sections, solderability testing by Gen3 wetting balance test machine is performed on the coated PCB.

1.5 Thesis Outline

The chapter of this thesis are outlined as follows:

Chapter 1 is the introduction to the solder, soldering process and surface finish that being utilize in the electronic area. It provides the problem statement, objective, and the work scope of the experimental project descriptions.

Chapter 2 is the literature review on the focused topic of the research. The raw materials, background study and the related solder finish process in electronic packaging industries are being introduced and discussed. The roles and features of solder finish were disclosed further at the end of the chapter.

Chapter 3 presents the experimental procedures which includes the experimental procedures and testing involved. This includes the equipment details which was used throughout the study.

Chapter 4 contains the results and finding with detail discussions and explanation.

The root cause and reason behind the results are being studied based on theoretical and experimental results and from previous studies from other research.

Chapter 5 draws the overall conclusion from the experimental studies. Apart from that, some recommendation are being suggested for future works in order to empower and generate more scientific findings.

CHAPTER 2

LITERATURE REVIEW

2.1 Soldering in Electronic Packaging Area

Soldering is a method used to produce permanent electrical and mechanical connections between metallic materials. The four basic components in soldering process are including the base metals, solder, flux and heat. The base metal reacts with the molten solder to form an interfacial IMC. The formation of interfacial IMC establishes a successful solder joint or bond between two or more components. The heat supplied must be sufficient to melt the solder but not enough to cause any melting of the base metals. It also have to prevent from any damage to the board or components. The thickness of an interfacial IMC layer increases with temperature and soldering time and may become embrittled and weak if the IMC layer is too thick. In solder electronics area, the base metal is generally copper. It is usually found on the PCB metallic circuitry and component leads or pins (Efzan & Marini, 2012; Plumbridge et al., 2004).

Solders are metal alloys that having a role that are used to bond or join two or more components and are used extensively in the electronics industry to physically hold assemblies together. They must allow expansion and contraction of the various components, must transmit electrical signals, and also dissipate any heat that is generated. The bonding action is accomplished by melting solder material, allowing it to flow among and make contact with the components to be joined (Efzan & Marini, 2012). Some