UNIVERSITI
MALAYSIA
PERLIS

Investigation of Plasma Induced Etch Damage/Changes in AlGaN/GaN HEMTs

A Ofiare[1], S Taking[1], K Karami[1], A Dhongde[1], A Al-Khalidi[1], E Wasige[1]

[1] High-Frequency Electronics group, division of Electronics and Nanoscale Engineering, James Watt School of Engineering, University of Glasgow, Glasgow, G12 8LT, United Kingdom

ABSTRACT

In this work, we report on the processing and device characteristics of AlGaN/GaN HEMT devices to investigate the effects of silicon dioxide (SiO_2) etching using Fluoroform (CHF_3) gas prior to gate metal deposition. Three different GaN device structures were fabricated: (a) device #1 in which the device passivation (using SiO_2) and gate metallisation are done in one lithography step, (b) device #2 in which the device passivation and gate metallization are done in 2 separate steps, (c) device #3, in which the gate metallization is deposited prior to passivation. 100 nm of plasma enhanced chemical vapor deposition (PECVD) SiO_2 was deposited for surface passivation to the devices. As fabricated, devices #1 and #2 exhibited very poor device characteristics with very low output currents which we attribute to surface plasma induced damage or changes on the gate region after the SiO_2 etching. A two-step post gate annealing step was performed on the devices to recover this damage. The highest maximum drain current of over 1100 mA/mm was observed on device #3 after the first anneal step compared to other devices which showed higher maximum drain current after the second anneal step. All three devices show an improvement in self-heating behavior after the second anneal step along with more stable transfer characteristics. The highest maximum peak transconductance of over 250 mS/mm was observed on devices #2 and #3 after the first anneal step. This reduces slightly for all devices but with more stable characteristics. The measured threshold voltage values (V_{TH}) are also consistent and stable after performing the second anneal step. These results indicate that avoiding exposing the active region of GaN devices is important in achieving expected and stable characteristics. It also observed that further device improvement can be done by performing a two-step post gate annealing process.

Keywords: AlGaN/GaN, high electron mobility transistors (HEMTs), plasma induced damage, post-gate annealing.

1. INTRODUCTION

GaN-based high-electron-mobility transistors (HEMTs) have demonstrated remarkable device performances due to their high two-dimensional electron gas (2DEG) concentration, high breakdown voltage, and high electron mobility [1][2][3][4]. The use of surface passivation such as Si_3N_4 and SiO_2 is a common technique to minimize surface traps on these devices [5][6][7][8]. The crucial step is the removal of surface passivation layer in the gate region prior to gate metal deposition. Plasma reactive ion etching (RIE) with fluoride-based chemistry has been widely used to etch Si_3N_4 and SiO_2 and such process can lead to surface damage on the devices [9][10][11]. The most common technique used to recover the plasma induced etch damage is by performing the post gate annealing [12][13][14] and this provides better improvement in the device performance.

In this work, we discuss the fabrication and device characteristics of three different processing steps used for fabrication of AlGaN/GaN HEMT devices. The aim is to identify the impact of the RIE etching of the SiO_2 passivation deposited using plasma enhanced chemical vapor deposition

(PECVD). Details of processing steps for all the devices and their device characteristics are discussed in the next sections of the paper.

2. DEVICE STRUCTURE AND FABRICATION

The epitaxial structure used in this work was grown by Cambridge University, UK, using metal organic chemical vapour deposition (MOCVD) on high resistivity silicon substrate. The wafer structure consists of (from top to bottom), a 2-nm GaN cap layer, 21-nm $Al_{0.25}GaN$ barrier layer, 1-nm AlN inclusion layer, 200-nm GaN channel layer, and 850-nm GaN and 1.7-µm AlGaN buffer layer on a 250-nm AlN nucleation layer. The experimental work was carried out to investigate the effects of SiO_2 etching prior to gate metal deposition. All the devices were fabricated utilizing the wrap-around gate design (where the gate encircles the drain) for fast device evaluation.

Three different GaN device structures were investigated: (a) device #1 in which the SiO_2 passivation is deposited first and after etching it to expose the gate region, the gate metallization is deposited. Here, only one lithography step is used, see Figure 1; (b) device #2, same as device #1 for SiO_2 patterning but a lithography step is used to define the gate region after etching of the SiO_2, see Figure 2; and (c) device #3, the gate is deposited before the SiO_2 deposition, see Figure 3. Both for devices #1 and #2, the SiO_2 layer in the gate region was removed using CHF_3 gas prior to gate metal deposition. For device #1, there is gap spacing between SiO_2 and the gate metal while for device #2, there is no gap spacing between SiO_2 and the gate metal (the gate metal is completely filled in the opening region of SiO_2). For device #3, there is no contact of CHF_3 plasma to the gate region prior to gate metal deposition.

The Ohmic source and drain contacts on all the devices were obtained by the evaporation of Ti/Al/Ni/Au (20/180/30/100 nm) followed by rapid thermal annealing (RTA) at 800 ^{0}C for 30 secs in N_2 environment. This was followed by PECVD deposition of 100 nm SiO_2 on devices #1 and #2, and the gate region was etched using CHF_3 gas with 100 W power on the reactive ion etching (RIE) tool for both. The Schottky gate contacts consisting of Ni/Au (20/200nm) was then deposited on all three devices. Device dimensions used in this work are as follows: gate length, L_G, of 4 µm, gate-to-source distance, L_{GS}, of 4 µm, gate-to-drain distance, L_{GD}, of 5 µm, and gate width, W_G, of 75 µm.
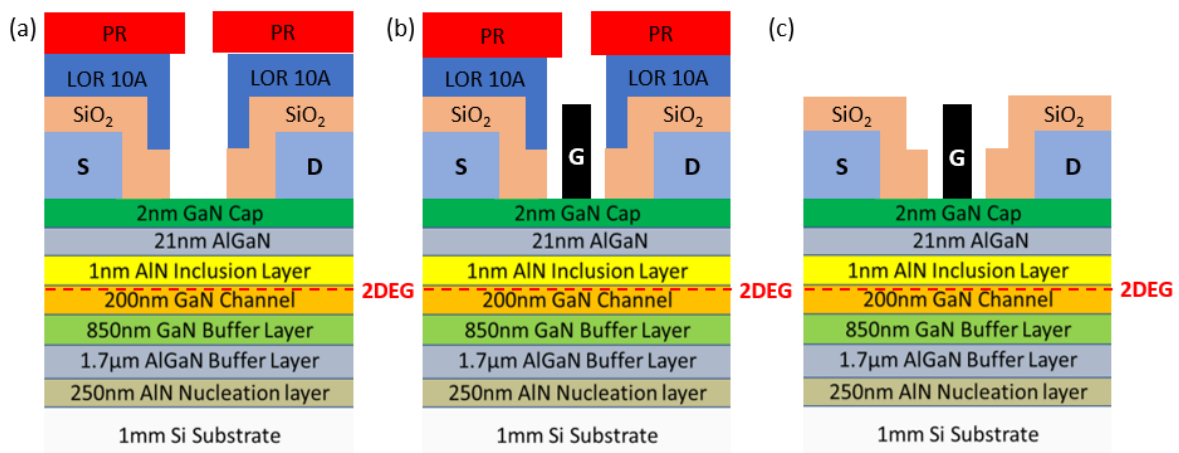

Figure 1. Processing steps of device #1, (a) patterned photoresist S1818 and LOR 10A, followed by a 100-nm SiO_2 etching (b) gate metallisation and (c) gate with gaps (after lift-off).
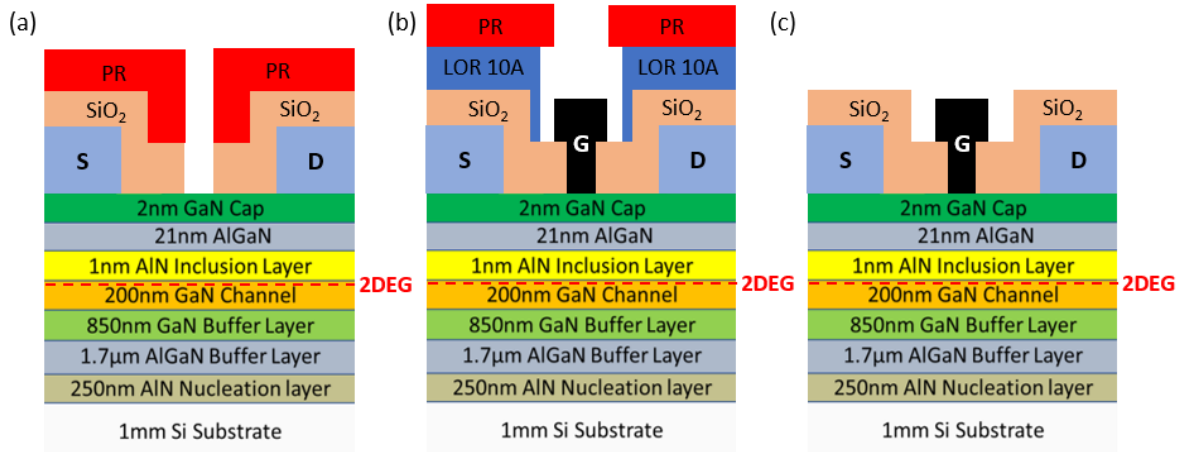
Figure 2. Processing steps of device #2, (a) patterned photoresist S1818, followed by a 100-nm SiO$_2$ etching (b) gate metallisation and (c) gate with no gaps (after lift-off).
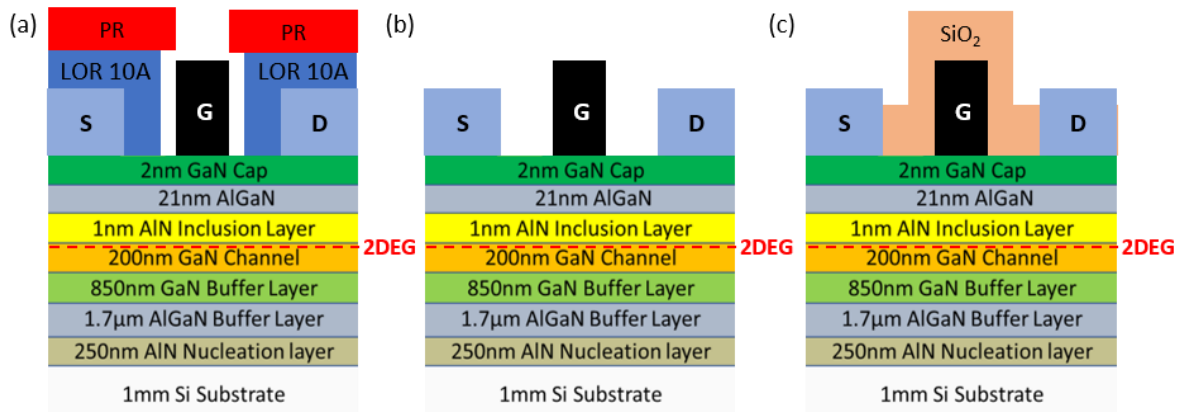

Figure 3. Processing steps of device #2, (a) patterned photoresist S1818, followed by a 100 nm SiO$_2$ etching (b) gate metallisation and (c) gate with no gaps (after lift-off).

3. RESULTS AND DISCUSSION

All devices were initially characterized as fabricated, and the measured output characteristics show very poor device characteristics with very low output currents, 60 µA and 260 µA for devices #1 and #2, respectively, as shown in Figures 4(a) and 4(b). We attribute this to the plasma induced damage using CHF$_3$ plasma. The output characteristics for device #3 are shown in Figure 4(c), where the measured maximum output current of 480 mA/mm and good pinch-off behaviour. These results demonstrate clearly that good device characteristics are achieved when no contact of CHF$_3$ plasma is used prior to gate metal deposition.

Surface damage from the plasma etching has been widely observed in the GaN-based devices, resulting in poor device characteristics [9][10][11]. The RIE plasma etch creates damages such as N$_2$ vacancies which act as shallow donors, reduces the GaN surface potential and leads to GaN band bending [12][13][14][15][16]. Post gate annealing is the most common technique used in fabrication of GaN-based devices to recover from plasma induced etch damage. It is known that by performing the post gate annealing can restore the N$_2$ vacancies and increases the GaN surface potential thus improving the device performance.
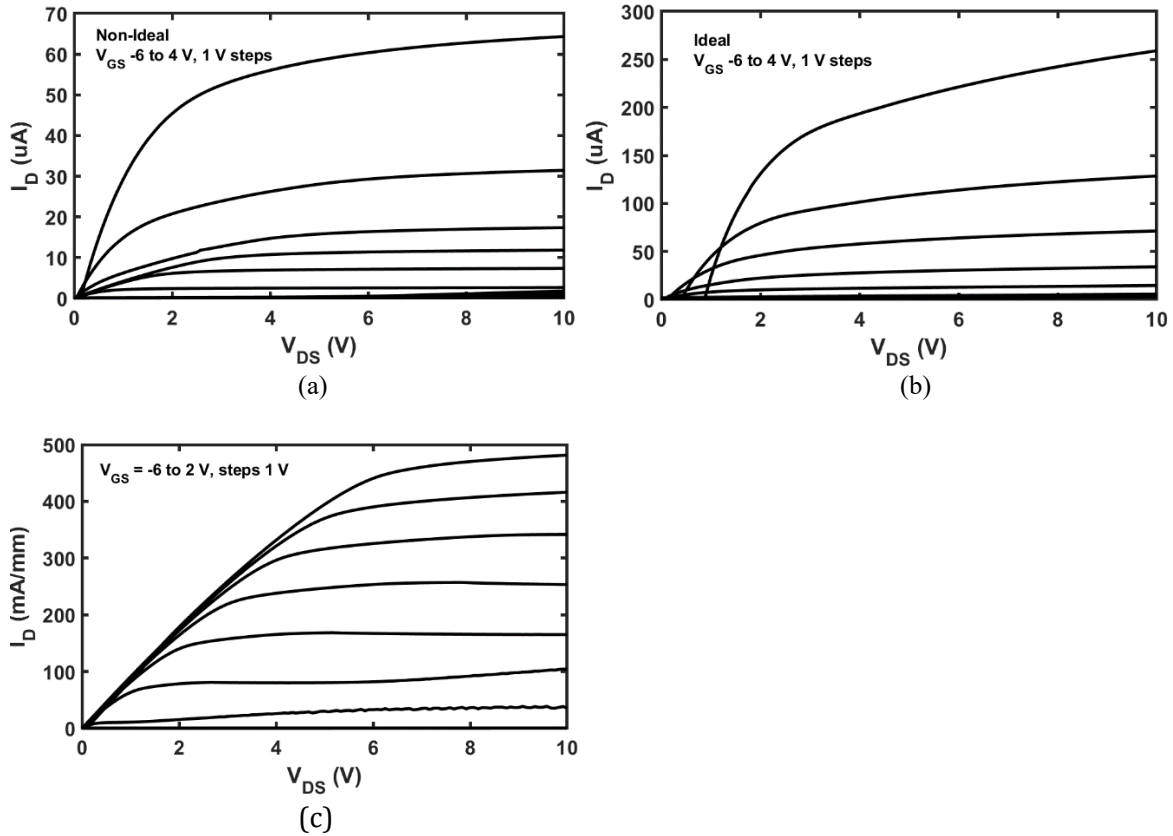
(a)

(b)

(c)

Figure 4. Measured output characteristics (a) device #1 biased at V_{GS} -6 V to 4 V in 1 V step, (b) device #2 biased at V_{GS} -6 V to 4 V in 1 V step and (c) device #3 biased at V_{GS} -6 V to 2 V in 1 V step.

The annealing time and temperature need to be optimized to improve the GaN device characteristics. In this work we used the optimized conditions reported in Refs. [17] for the post gate annealing. The fabricated devices were annealed in N_2 ambient at 400 °C for 10 mins. An additional annealing step (two-step anneal) was also conducted as it was reported in Ref. [18], significant improvement in the GaN device performances were observed after performing the second post gate annealing at 500°C for 5 mins in N_2 ambient.

The output characteristics of device #1 are shown in Figure 5(a) after the first annealing. The maximum drain current was 850 mA/mm and this value improves after the second annealed step to over 900 mA/mm with better self-heating characteristics. Figure 5(b) shows the maximum peak transconductance after the first annealed was ∼ 230 mS/mm and this value reduces slightly after the second annealed step to 200 mS/mm with more stable characteristics. For device #2, the maximum drain current after the first annealing step was 900 mA/mm and this value improves after the second annealed step to 1000 mA/mm with better self-heating characteristics, see Figure 6(a). Figure 6(b) shows the maximum peak transconductance after the first annealing was over 250 mS/mm and this value reduces slightly after the second annealed step to ∼ 230 mS/mm with more stable characteristics. For device #3, the maximum drain current after the first annealing was over 1100 mA/mm and this value reduces slightly after the second annealed step to ∼ 1100 mA/mm but with better self-heating characteristics, see Figure 7(a). Figure 7(b) shows the maximum peak transconductance after the first annealing was over 250 mS/mm and this value reduces slightly after the second annealed step to ∼ 230 mS/mm with more stable characteristics. Note that the output drain currents for devices #1 and #2 before the post gate metal annealing cannot seen in the output characteristics shown in Figure 5(a) and Figure 6(a) due to very low measured currents for the devices, 1.5 mA/mm and 5.9 mA/mm for devices #1 and #2 respectively.

The measured threshold voltage values (V_{TH}) are almost consistent and stable after performing the second anneal step and the values are -3 V, -2.6 and - 3.5 V for devices #1, #2 and #3, respectively, as shown in Figure 5(b), Figure 6(b) and Figure 7(b). The obtained results show that the two-step annealing is a better approach to process the devices especially if a surface passivation layer is employed in the device fabrication.
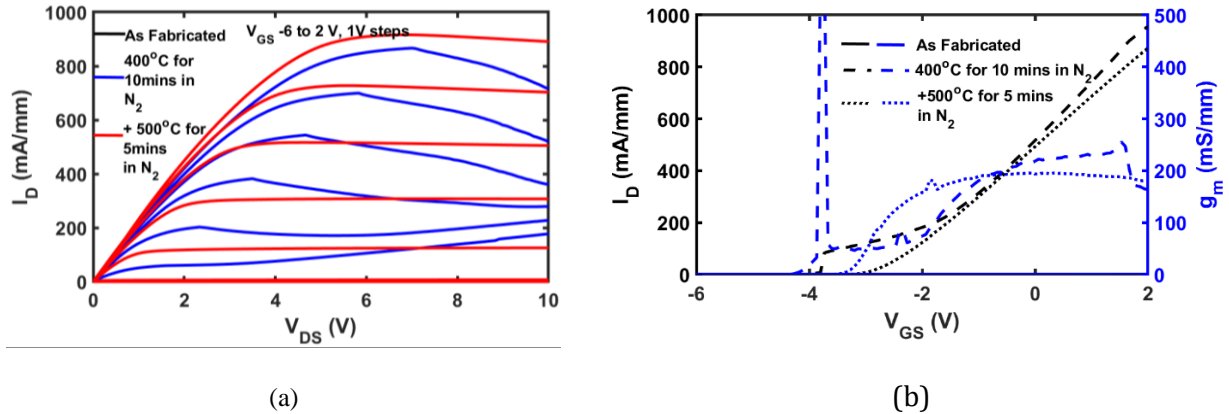

(a)   (b)

Figure 5. (a) Measured output characteristics at gate-to-source voltage biasing, V_{GS}, from -6 V to 2 V (b) Measured transfer characteristics at V_{DS} = 7 V before and after two-step annealing process for device #1.
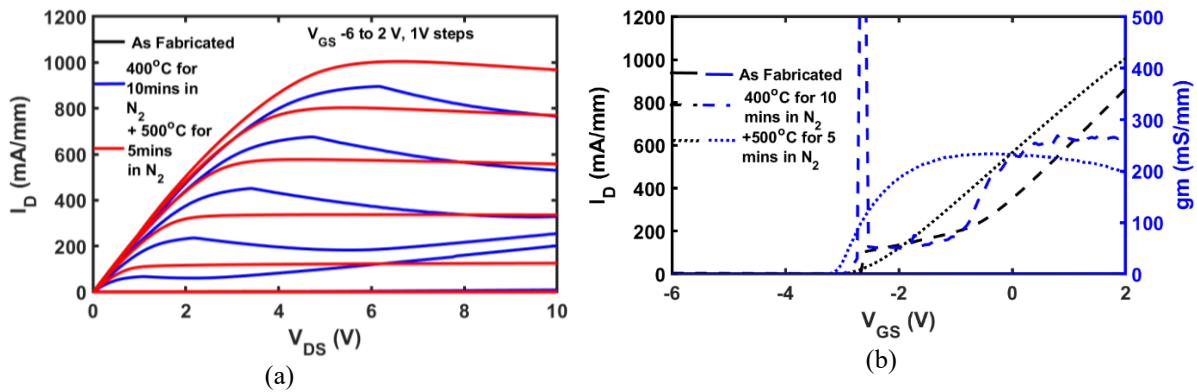

(a)   (b)

Figure 6. (a) Measured output characteristics at gate-to-source voltage biasing, V_{GS}, from -6 V to 2 V (b) Measured transfer characteristics at V_{DS} = 7 V before & after 2-step annealing process for device #2.
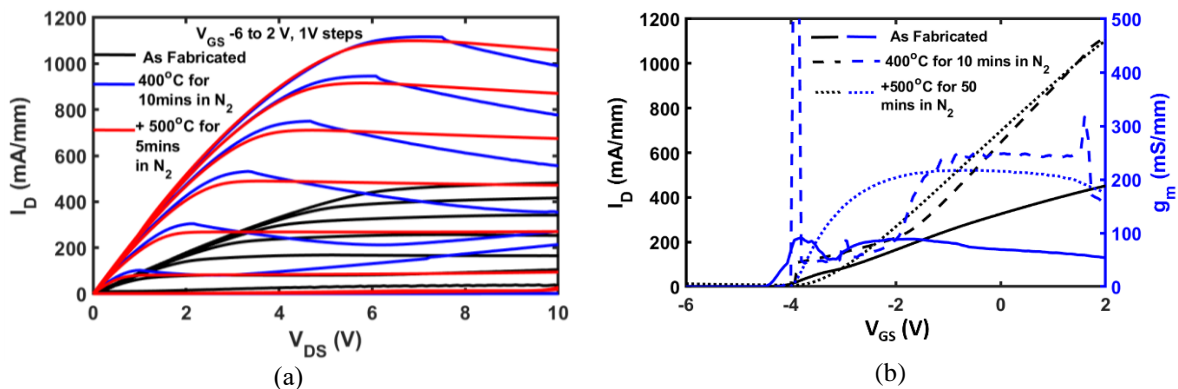

(a)   (b)

Figure 7. (a) Measured output characteristics at gate-to-source voltage biasing, V_{GS}, from -6 V to 2 V (b) Measured transfer characteristics at V_{DS} = 7 V before & after two-step annealing process for device #3.

The measured gate leakage current characteristics for all devices are shown in Figure 8. There is no obvious difference in the gate leakage current for device #1 after the first and second annealing steps, while the leakage current is lower after the second anneal step for the device #2. However, for the gate-first device it is higher after the second anneal step. This observation is not fully understood and needs further investigation.
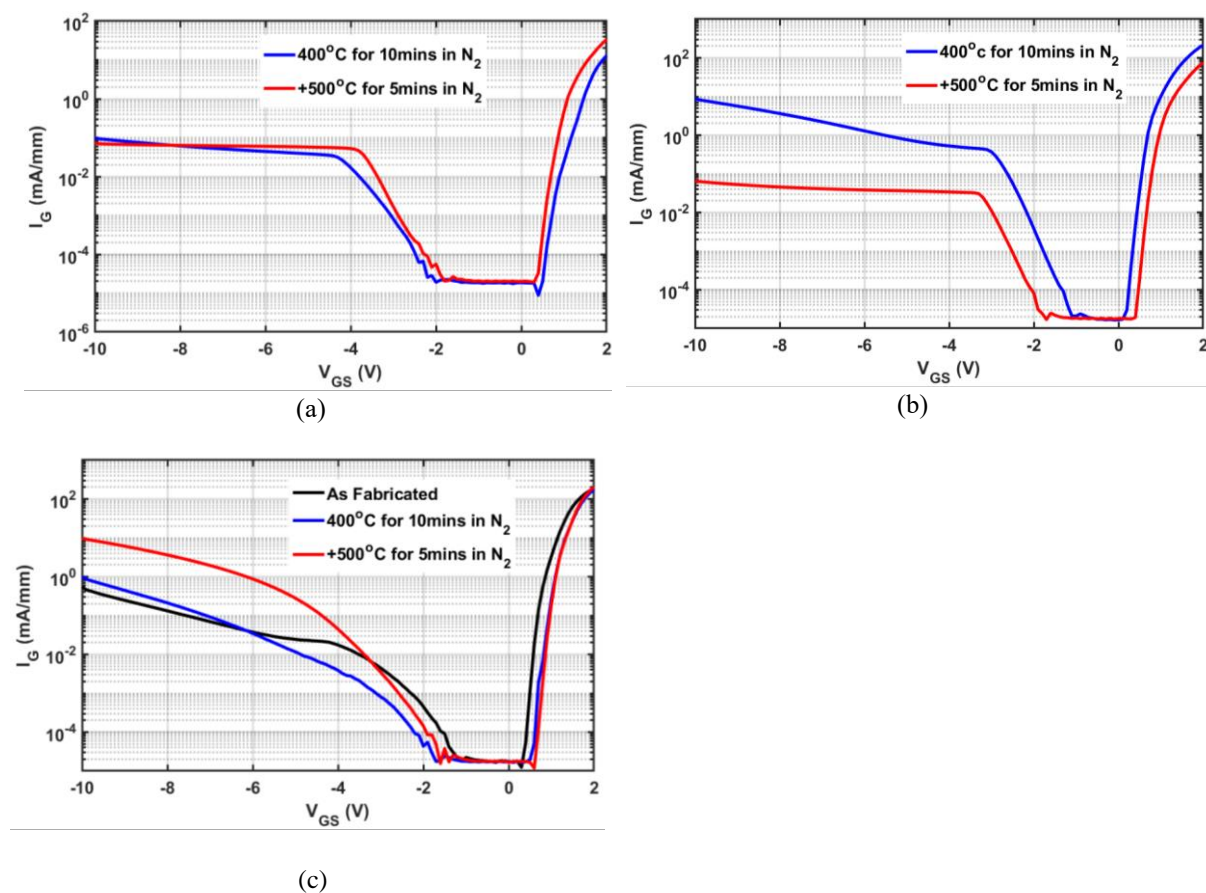

(a)

(b)

(c)

Figure 8. Measured gate leakage before & after two-step annealing for devices (a) #1, (b) #2 & (c) #3.

The measured breakdown voltage, VBR, for device #1 exceeds the maximum compliance of the measurement set up of 200 V after the first anneal and this is reduced to ~ 180 V after the second anneal. As for device #2, all devices exceed the maximum compliance of the measurement set up after performing the first and second anneal. For the device #3, the measured VBR as fabricated device is ~ 94 V while the VBR of the device after performing the first and second anneal exceeds the maximum compliance of the measurement set up.

4. CONCLUSION

Three different structures were fabricated to investigate the effects of SiO_2 etching using CHF_3 plasma prior to gate metal deposition. Very poor device characteristics with very low output currents were initially observed both for the devices in which the gate region was exposed to the etching plasma. To recover the plasma damage, the two-step post gate annealing was performed. The highest maximum drain current of over 1100 mA/mm was observed on the device which was not exposed to CHF_3 plasma at all after the first anneal step. All 3 devices show an improvement

in self-heating behaviour after the second anneal step along with more stable transfer characteristics. The highest maximum peak transconductance of over 250 mS/mm was observed on both device #3 (no exposure to plasma) and device #2 after the first anneal step. The measured threshold voltage values (V_{TH}) are also consistent and stable after performing the second anneal step. We found that avoiding exposure of plasma to the device active region benefits the device performance. We also found that further device improvement can be achieved by performing the two-step post gate annealing.

ACKNOWLEDGEMENTS

REFERENCES

[1]   Abid, I., Kabouche, R., Bougerol, C., Pernot, J., Masante, C., Micromachines, MDPI, vol. **10**, no. 10 (2019), pp. 690.

[2]   Abid, I., Mehta, J., Cordier, Y., Derluyn, J., Degroote, S., Miyake, H., Medjdoub, F., Electronics, vol. **10**, no. 6 (2021), pp. 635.

[3]   L. E. Velikovskiy, P. E. Sim, O. I. Demchenko, N. E. Kurbanova, I. A. Filippov, A. V. Sakharov, W. V. Lundin, E. E. Zavarin, D. A. Zakheim, D. S. Arteev, M. A. Yagovkina, A. F. Tsatsulnikov, "InAlN/GaN and AlGaN/GaN HEMT technologies comparison for microwave applications," in IOP Conf. Ser. Mater. Sci. Eng., vol. **1019**, no. 1 (2021).

[4]   Liu, W. et al., IEEE Microw. Wirel. Components Lett., vol. **31**, no. 6 (2021), pp. 748–751.

[5]   Arulkumaran, S., Egawa, T., Ishikawa, H., Jimbo, T., Sano, Y., Appl. Phys. Lett., vol. **84**, no. 4 (2004), pp. 613–615.

[6]   Liu, Z. H., Arulkumaran, S., Ng, G. I., IEEE Microw. Wirel. Components Lett., vol. **19**, no. 6 (2009), pp. 383–385.

[7]   Tadjer, M. J. et al., ECS J. Solid State Sci. Technol., vol. **6**, no. 1 (2017), pp. P58–P61.

[8]   Hashizume, T., Nishiguchi, K., Kaneki, S., Kuzmik, J., Yatabe. Z., Mater. Sci. Semicond. Process., vol. **78** (2018), pp. 85–95.

[9]   Kang, M-J., Kim, H-S., Cha, H-Y., Seo, K-S., Crystal 2020; vol. **10**, no. 9, (2020), pp. 842.

[10]   Guan, H., Shen, G., Gao, B., Zhang, H., Wang, Y., Wang, S., IEEE Access, vol. **9** (2021), pp. 9855–9863.

[11]   Rawal, D. S., Amit, Sharma, S., Kapoor, S., Laishram, R., Vinayak, S., Solid State Electron. Lett., vol. **1**, no. 1 (2019), pp. 30–37.

[12]   Tang, S. W., Huang, Z. H., Chen, Y-C., Wu, C-H., Lin, P-H., Chen, Z-C., Lu, M-H., Kao, K-H., Wu, T-L., Microelectron. Reliab., vol. **122** (2021), pp. 114150-114156,

[13]   Zaidi, Z., Lee, K., Guiney, I., Qian, H., Jiang, S., Wallis, D., Humphreys, C., Houston, P., Semicond. Sci. Technol., vol. **30**, no. 10 (2015), pp. 105007.

[14]   Q. Fan, S. Chevtchenko, Xianfeng Ni, S-J. Cho, H. Morko, "Recovery of GaN surface after reactive ion etching," in Proc. SPIE, Gallium Nitride Materials and Devices, vol. **612** (2006).

[15]   Cho, S.-J., Doğan, S., Sabuktagin, S., Reshchikov, M. A., Johnstone, D. K., Morkoç, H., Applied Physics Letters, vol. **84**, no. 16 (2004), pp. 3070-3072.

[16]   Niu, D. et al., Micromachines, vol. **12**, no. 2 (2021), pp. 1–9.

[17]   Cai, Y., Zhou, Y., Lau, K. M., Chen, K. J., IEEE Transactions on Electron Devices, vol. **53**, no. 9 (2006), pp. 2207-2215.

[18]   Z. Zaidi, "Applications of GaN HFETs in UV detection and Power electronics," (2014) pp. 1–169.