From Nanostructure to Nano Biosensor: Institute of Nano Electronic Engineering (INEE), UniMAP Experience

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Abstract

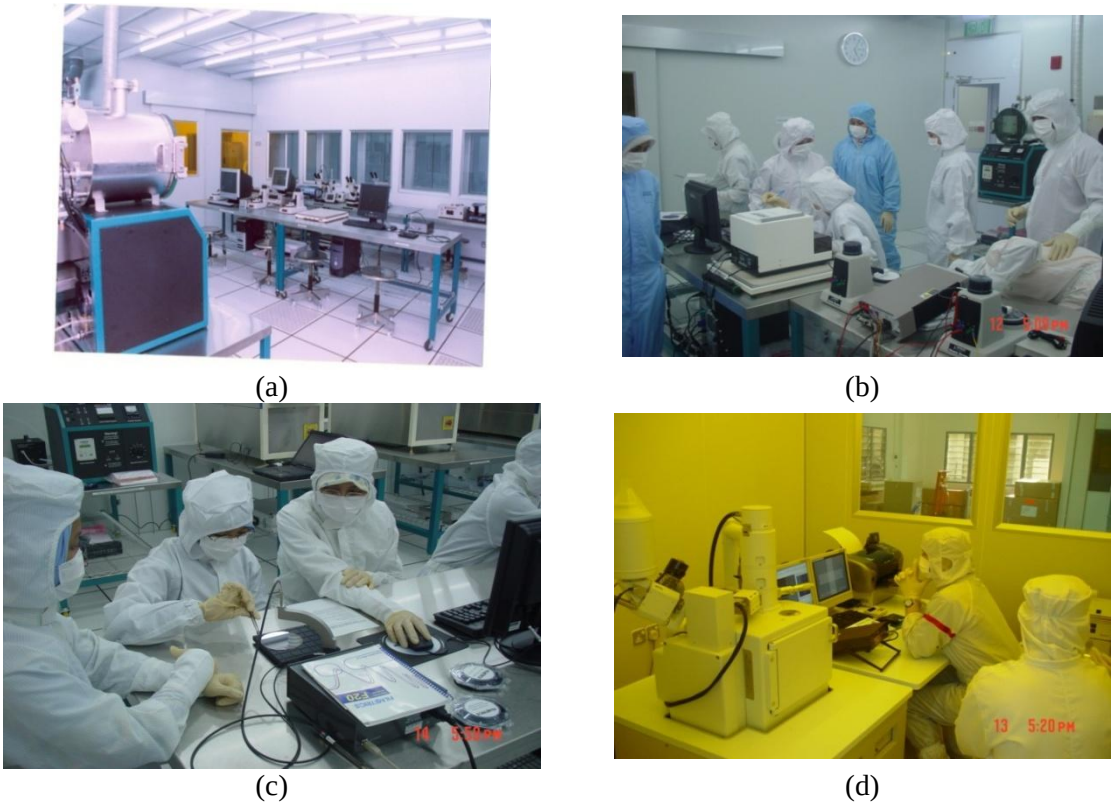
Nanostructure is defined as something that has a physical dimension smaller than 100 nanometers, ranging from clusters and/or to dimensional layers of atoms. There are three most important nanostructures that are extensively studied and researched in various organizations including Institute of Nano Electronic Engineering (INEE) in UniMAP. These include quantum dot, nanowire, and nanogap, which have been successfully designed and fabricated using in-house facilities available. These are subsequently used as a main sensing component in nanostructures based biosensor. This fabrication, characterization and testing job were done within four main interlinked laboratories namely microfabrication cleanroom, nanofabrication cleanroom, failure analysis laboratory and nano biochip laboratory. Currently, development of Nano Biosensor is the main research focus in INEE. In principle, biosensor is an analytical device which converts a biological response into an electrical signal.

Keywords: Nanostructure, INEE , nanowire , nanogap and Nano Biosensor

1. Research Facilities and Equipments

INEE comprises of 3 laboratories with state-of-the-art scientific equipment and facilities to accommodate researchers involve in device design, fabrication, characterization and testing**.** There are Micro Fabrication Cleanroom Laboratory, Nano Fabrication Cleanroom Laboratory and Nano Biochip Laboratory. The micro fabrication clean rooms (MFC) is the first and largest purpose build for research and teaching program by a university in Malaysia. The size of the cleanroom built is approximately 115m^2 with cleanliness class from ISO Class 5 to ISO Class 8. The cleanroom currently equipped with ten-process module comprising of oxidation, diffusion, photolithography, physical vapor deposition, wet etching, wet cleaning, wafer test and characterization, scanning electron microscope and E-beam lithography module.

The Nano Fabrication clean room (NFC) is housed in a combined cleanroom adjacent to the MFC. The NFC is facilitated with an Electron Beam Lithography (EBL) system for creating extreme fine nanopatterns for integrated circuits, Inductively Coupled Plasma – Reactive Ion Etching (Dry Etching) (ICP-RIE Etcher) for anisotropic etches of all type of thin films, and a Plasma Enhanced Chemical Vapour Deposition (PECVD) unit for deposition of high quality and stable interlayer dielectric film. The Nano BioChip laboratory focuses on testing and characterization of lab-scale silicon biosensor system. The laboratory holds two cleanbooth ISO class 10 known as yellow and white cleanbooth. Yellow cleanbooth is for testing and biology synthesizing under low light condition. The white cleanbooth is equipped with a high range frequency dielectric analyzer altogether with probe station integrated oscilloscope for electrical characterization and lab-on-chip package.



(a) (b)

(c) (d)

Figure 1: Micro fabrication cleanroom (a) cleanroom with equipment, (b) general views of the cleanroom in operation, (c) film thickness measurement, and (d) e-beam lithography

2. Research Road Map and Future Plan

Institute of Nano Electronic Engineering (INEE) was established in November 2008 as a converging hub for innovation, research and expertise in Malaysia, particularly for the Northern Corridor Economic Region (NCER). The objectives of the Institute are to continuously promote nano electronics expert within the Malaysian market, introducing the best in micro and nano fabrication practices from around the world to Malaysian society and building direct links between the technology and education sectors. INEE emphasizes on nano electronics engineering research activities that focus on nano biochip, novel devices, memory devices and nano photonic devices. After the passive nanostructure, such as quantum dots, nanowire, nanogap, nanotube and nanoporus had been successful developed in year 2008, INEE is currently work on functionalized the nanostructure for several type of sensor and transistor. In few years time later, various type of sensor will be successful produced by INEE Nano Biochip Research Group. At last, these sensors will be combined with the Computer-Aided Systems to produce a Nano Bio-System so called Lab-On-A-Chip. The INEE Road Map is shown in Figure 2.

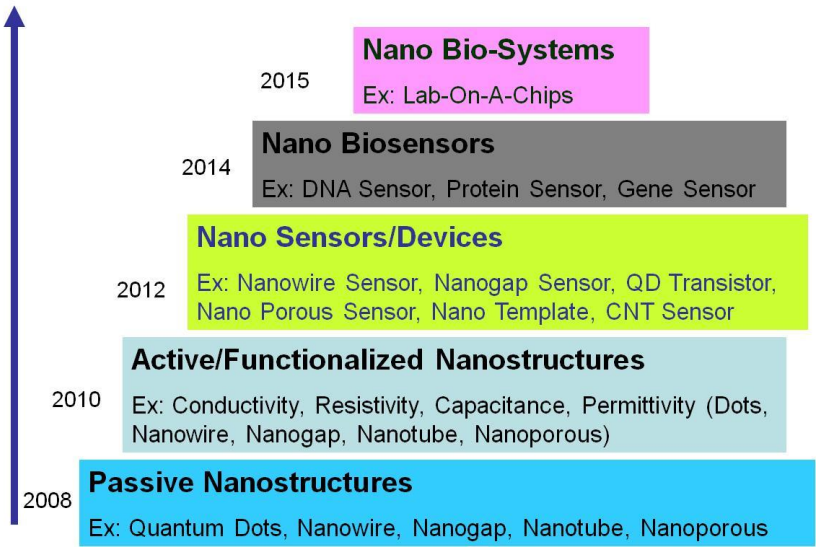


Figure 2: The INEE's Nanostructures to System Road Map

3. Microelectronic Based Research Output

3.1 ISFET

The basic structure of an ISFET is an n-channel enhancement mode FET. The source region is the electron supplier and the electrons drain from the drain region. It is the membrane covering the ISFET which provides the device its ionic sensitivity. Once the design of the layout is confirmed the masks from CAD designs were then transferred onto transparencies as actual mask using high resolution printer. All the masks were displayed in Figure 3.

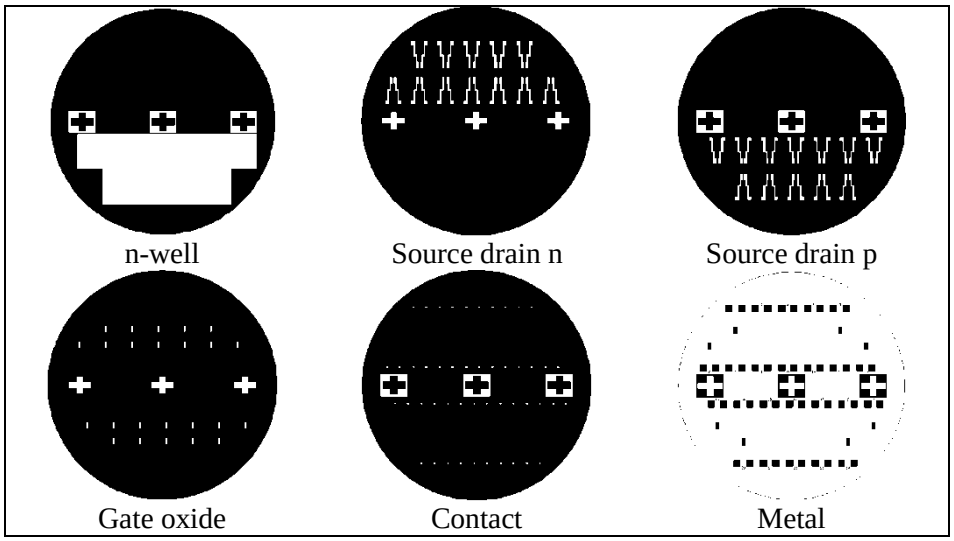


Figure 3: CAD design of ISFET masks.

The fabrication of the ISFET is a straightforward task as in principle the ISFET is a MOSFET with its gate region replaced by pH sensitive membrane exposed to solution under test. It is obviously advantageous to use standard CMOS

process as the resulting ISFETs can be easily and readily fabricated using existing CMOS foundries. In this research, the ISFET is fabricated on the basis of the MOSFET using standard N-Well CMOS technology with no extra or post processing steps. Figure 4 depicts the process flow of fabricating the ISFETs. By using CMOS technology, the starting material is chemically cleaned and oxidised p-type silicon wafer. N-well region, where PMOS transistors will be created are doped and diffused by phosphorus. Area with NMOS transistors and ISFETs are usually doped by boron to form p-well region. Active regions of all NMOS and PMOS transistors are then defined by photolithography. The wafer is then cleaned; the photoresist and the oxide are removed. Thin gate oxide of all active devices is created. The photoresist protecting the ISFET is removed and a special silicon nitride ion sensitive layer is PECVD deposited over the sensor gate region. In simple technologies, no inter level oxide is necessary and the deposition of the sensing membrane can be done at the end of the process fabrication if the temperature of deposition is not too high for the materials already deposited. The ISFET gate structure is now a bilayer consisting of a thermally grown silicon dioxide and a deposited silicon nitride layer. Contact openings are etched for accessing source and drain areas of ISFET, NMOS and PMOS transistors. The wafer is then coated with aluminium by thermal evaporation. A final photolithography step creates the metal contacts of the ISFETs. Figure 5 shows a completed wafer of ISFETs.

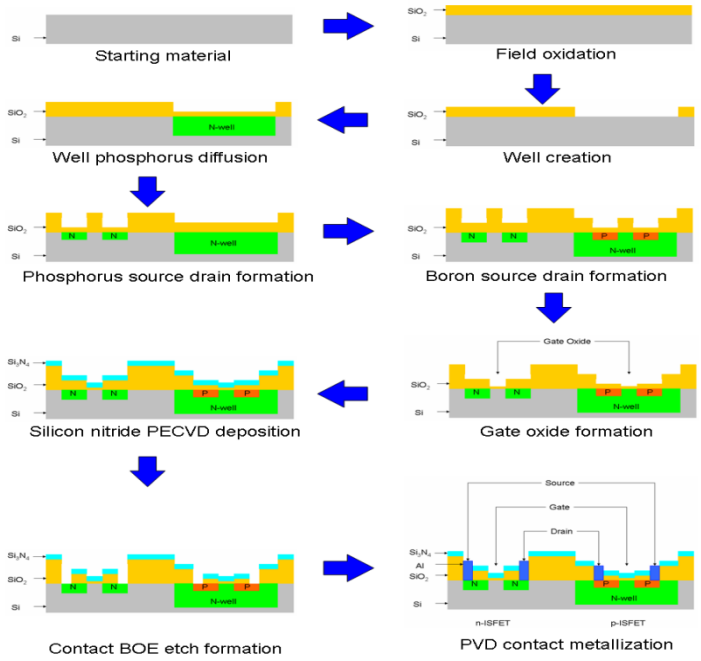


Figure 4: ISFET fabrication flow based on CMOS process

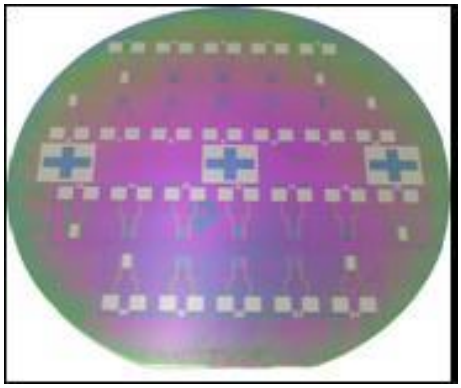


Figure 5: Completed ISFET on wafer

Before testing and measurements can be performed onto the ISFET, the device has to be prepared. This sort of preparation is called the encapsulation process of the ISFET. In order to use the ISFET with liquids, the ISFET must be covered with a protective layer to expose only the pH sensitive gate region. The ISFET die have to be mounted, wired and encapsulated before it could be used. Figure 6 illustrates the encapsulation process of the ISFET.

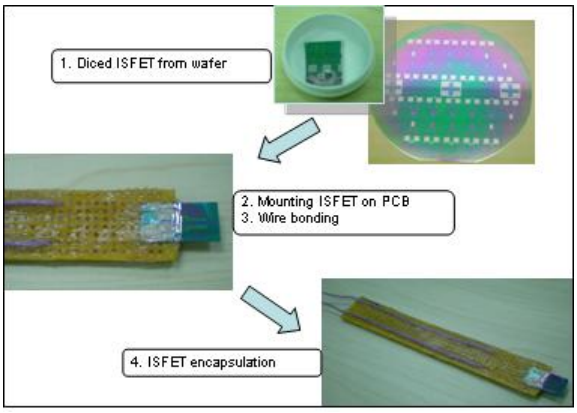


Figure 6: Encapsulation process of ISFET.

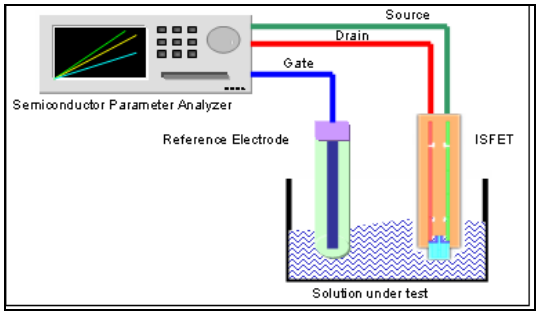
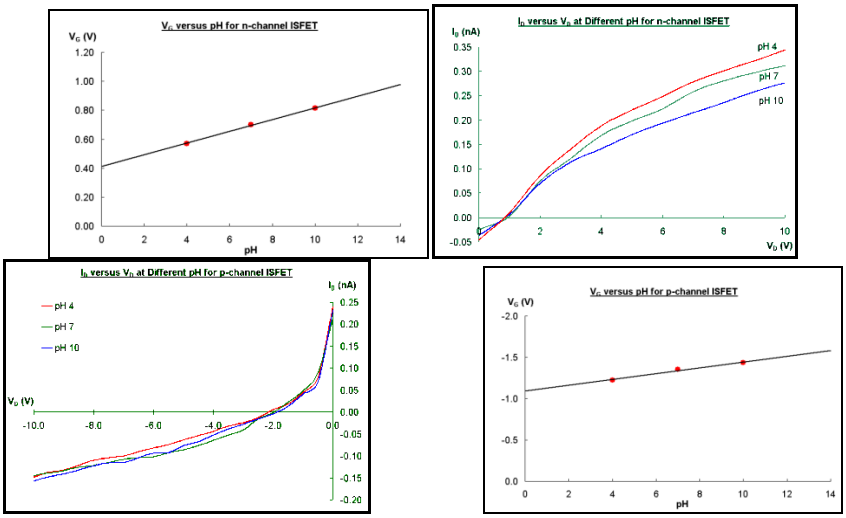


Figure 7: ISFET characterization set-up.

Once the CMOS ISFET has completed fabrication, it has to be tested and evaluated for its functionality. The measurement set-up and instruments are

shown in Figure 7 and all the test results are on display in Figure 8. The pH sensitivity of an ISFET was obtained through a shift in the measured threshold voltage, V_{TH}, of an ISFET. The V_{TH} was derived from the relationship curves between I_D and V_G. The transfer characteristics of the ISFET were recorded using the Keithley 4200 SPA. The change of V_{TH} of the ISFET is related to the change of electrolyte pH. A pH sensitivity of approximately 40.34mV/pH for Si_3N_4 gate n-channel ISFET and 34.83mV/pH for Si_3N_4 gate p-channel ISFET were calculated from the normalized curves plotted in Figure 8. These results agree with published values in the literature. The fabricated ISFETs present a satisfactory linear response with pH. In conclusion, the ISFETs in this research was successfully fabricated and characterized.



n-ISFET **p-ISFET**

Figure 8: The pH responses and device sensitivities of ISFETs

3.2 LISFET

The fabrication of LiSFET starts with a 4 inch p-doped silicon wafer. The fabrication involves four masking steps for NMOS process. The layout and dimension of each mask for LiSFET fabrication is shown in Figure 9. As shown in Figure 10, a new thick sacrificial layer is grown to serve as a diffusion mask in the next diffusion process. The first mask, N-type Diffusion Mask patterns the source and drain region of the n-channel MOSFET. After developing and etching, the wafer substrate is diffuse with the phosphorus by using the solid source wafer inside the n-doped diffusion furnace. The second mask, Gate Mask patterns the gate area of the MOSFETs. After developing and etching, a thin layer of gate oxide is grown under the presence of oxygen in the oxidation furnaces. A well mask is patterned onto the passivation layer to define the area which contains the sensing medium. The next process step is the deposition of Cadmium Sulphide by using PVD thermal evaporation. The CdS powder is evaporate from a Mo boat, with bored cap, connected between two coaxially cooled copper electrodes at 550°C, temperature where evaporation takes place. The annealing process for CdS layer can be done at 400°C in H_2 flow for 15 minutes. The next step is to spin coat photoresist on the CdS film, and it is exposing to UV light through a mask that makes the exposed layer soluble in basic developer solution. The exposed CdS layer can be etch either with wet etching or plasma etching by using HCI as a dissolving solution. The fourth masking step is uses Contact Mask to pattern the contact holes. The MOS device fabricated this far is ready for metallization process. An aluminium layer is deposited on top of

the MOS device by means of evaporation. The evaporation process is done inside the Physical Vapour Deposition Module (PVDM). The final masking step, Metal Mask defines the metal gate and contacts of the MOSFETs.

The images taken from the Low Power Microscope (10x magnification) were used to determine the proper line per area to come from the photolithography tool. Figure 11 shown the actual patterns of ISFET were fabricated with using photolithography equipment in UniMAP Cleanroom.

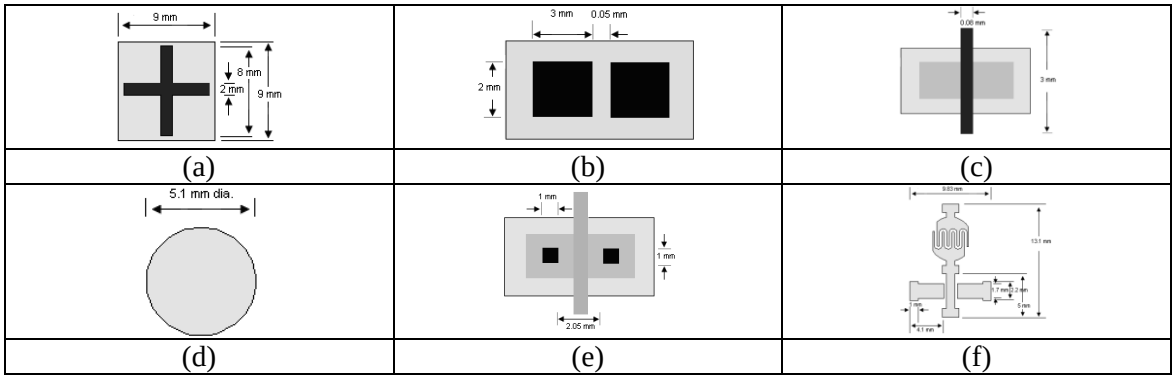


Figure 9: Masks Design and Specification for LISFET Fabrication (a) Align Mark Formation, (b) Source & Drain Formation, (c) Gate Oxide Formation, (d) CdS Sensor Formation, (e) Contact Formation and (f) Metallization Formation

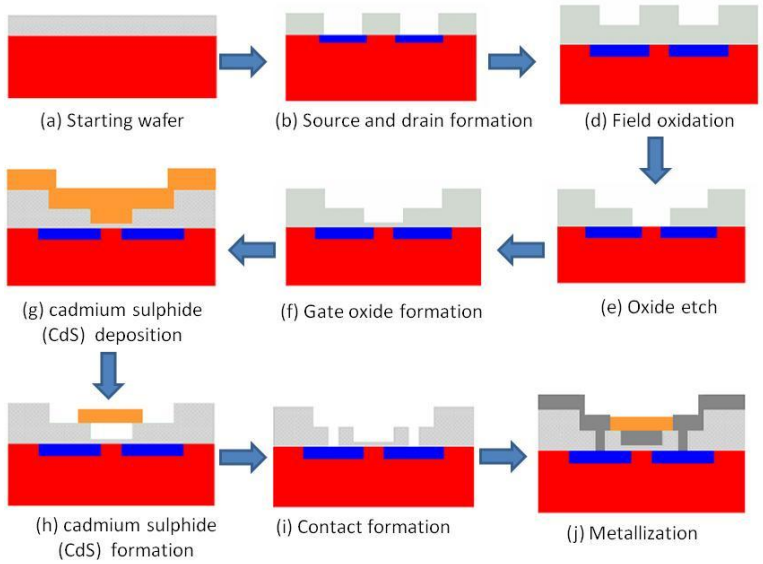


Figure 10: LiSFET fabrication process flow

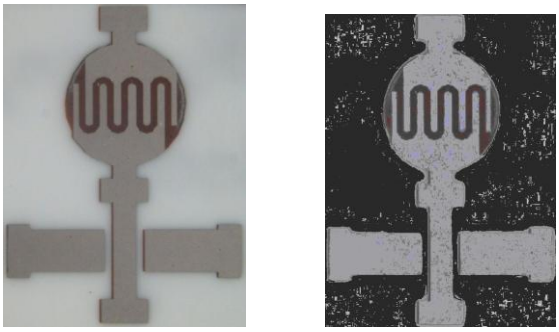


Figure 11: Actual pattern LiSFET were fabricated on different wafer

Once the LiSFET is completed fabrication, it is tested and evaluated for its functionality under the light. From the result shown in Figure 12, a CdS photoconductive sensor is a thick film semiconductor material whose electrical resistance decreases with increasing incident light. Photoconductive sensors based on cadmium sulfide (CdS) have sensitivity curves that closely match the sensitivity of the human eye.

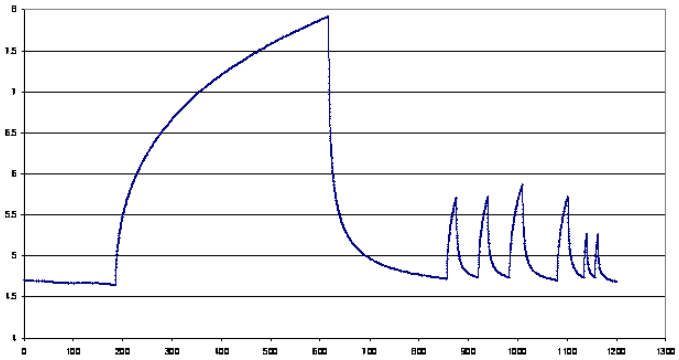


Figure 12: Switching testing result

4. Nanostructure Formation

4.1 Electronic Beam Lithography (EBL)

Scanning electron microscope (SEM) based electron beam lithography (EBL) is a method that used in this work. A Raith Elphy Quantum pattern generator was used to design the written pattern structures. This technique allows a large number of ohmically contacted nanoscale devices with controllable length to be placed on a single substrate. ELPHY Quantum is a universal lithography attachment which makes it possible to produce micro and nano structures by means of electron beam writing in connection with scanning electron microscope (SEM) system. The system has the control in three major areas of Scanning Electron Microscopes (SEM): Beam Blanker control, Scan & Signal control and Stage control. All required functions are fully integrated into one software, from pattern design, exposure parameter management, pattern overlay alignment to step and repeat exposures. Elphy Quantum is Windows-based operating software as shown in Figure 13 and its functionality is based upon a modular design. Editing and pattern design is made simple with a GDSII internal editor. This allows users to build hierarchy patterns on different levels and designs with any dose level within the shortest possible time. The fabrication step is shown in Figure 14. The following Figure 15 showed the successfully fabricated smaller size 70nm of silicon oxide nanowire and a 50nm of silicon nanowire.

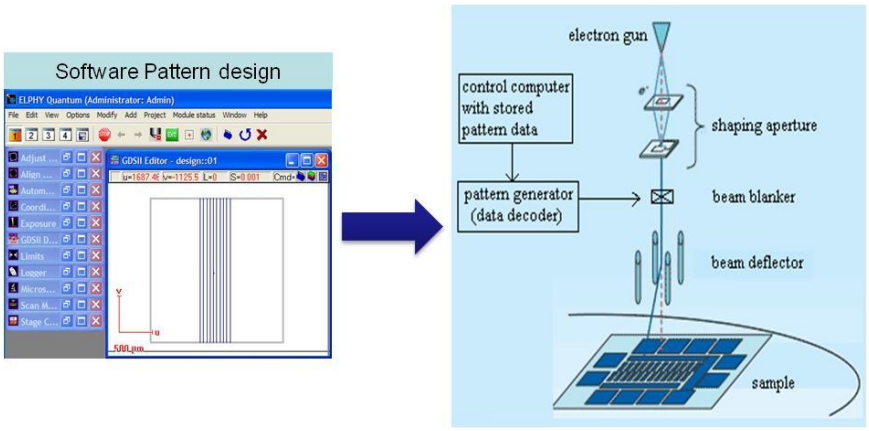


Figure 13: Electronic Beam Lithography (EBL) Technique

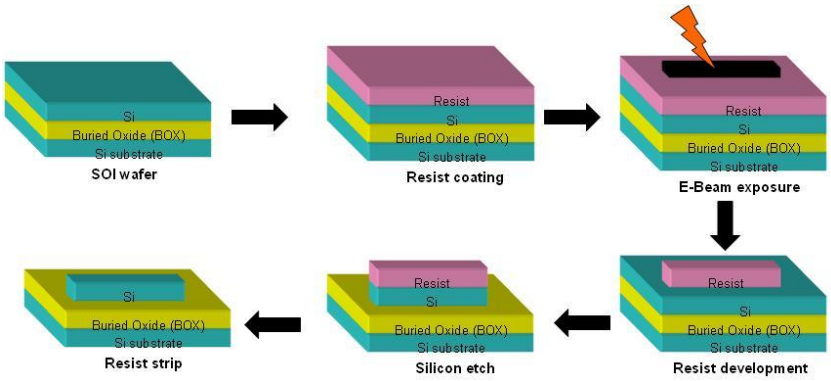


Figure 14: Electronic Beam Lithography (EBL) Process Flow

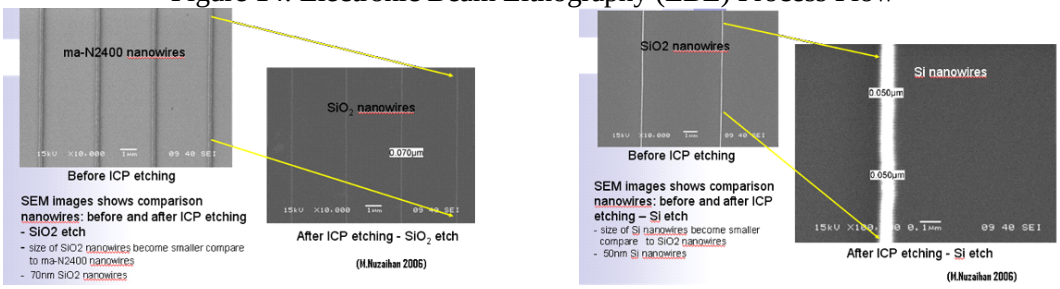


Figure 15: Silicon Oxide Nanowires and Silicon Nanowires

4.2 Spacer Patterning Lithography (SPL)

Spacer Patterning Lithography (SPL) is a low-cost and compatible to standard CMOS fabrication process. SPL, in general is a combination of conventional photolithography, anisotropic etchings and the excellent homogeneity and reproducibility of conformal chemical vapor deposition processes.

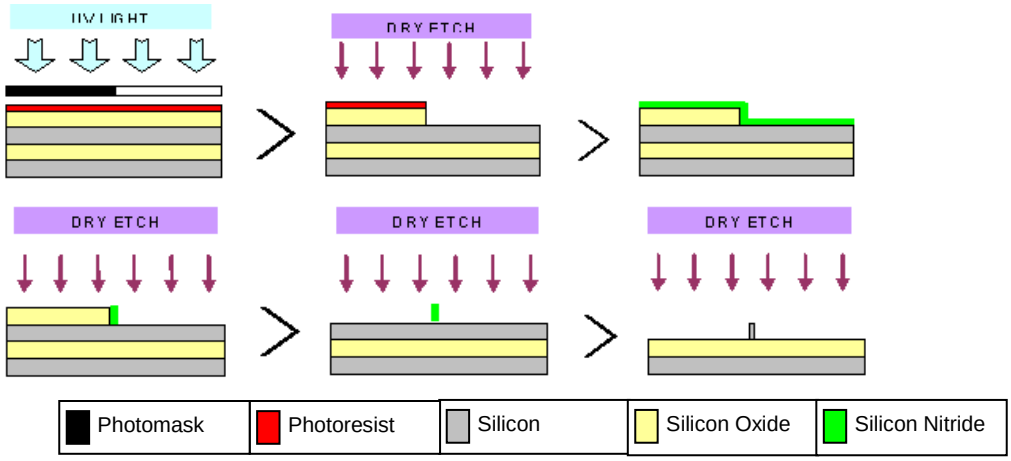


Figure 16: Layer by layer alignment and patterning method.

The process (shown in Figure 16) begins with deposition 200-500 nm layer of silicon oxide (SiO_2) as the sacrificial layer on a clean highly doped SOI wafer following by the mask pattern on top of it. This SiO_2 and Si_3N_4 are deposited by PECVD, plasma enhance will deposit the SiO_2 layer before making the proper mask alignment on top of it. After deposition, photo resist (PR) solution will be loaded onto the SiO_2 layer before making the proper mask alignment on top of the PR. By using MIDAS exposure system, pattern from the first mask is transferred on the PR. Prior to this, development and etching process using ICP-RIE inductive coupled plasma, the pattern layer is finally moved onto the SiO_2 layers. This etched recipe produced vertical sidewall profile with an angle 85°-88°. The residue PR is then removed using the Plasma-PreenII-862 system by Plasmatic Systems Inc. Then, a thin layer about 100nm-200nm of Silicon Nitride (Si_3N_4) is deposited on top of it. This thin layer of Silicon Nitride (Si_3N_4) is deposited uniformly onto the SOI to create the layer for spacer formation. The spacer is then defined using ICP-RIE etching by removing the silicon oxide. The spacer formed will be the next mask for the highly doped crystalline silicon substrate. The nanowire is then defined using ICP-RIE etching by removing the silicon. A series of SEM images are observed and shown in Figure 17 as an outcome of spacer patterning lithography process.

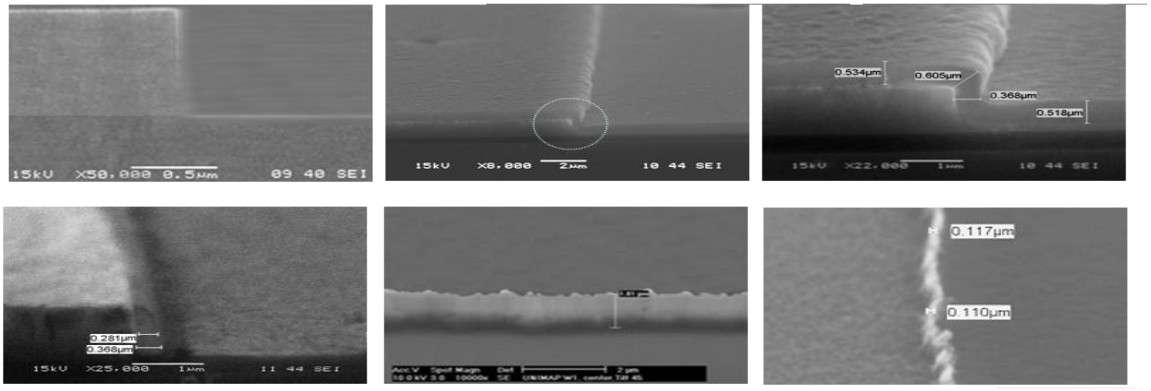


Figure 17: Image of sidewall and spacer formation under SEM

4.3 Size Reduction Lithography (SRL)

Size Reduction Lithography (SRL) method of pattern transfer is the selective

removal of material. The desired characteristics of such a process include selectively, anisotropy, a little damage to the electronic device. The consequence of isotropic etching is that the horizontal etch rate is comparable to the vertical etch rate. This fabrication method could potentially be used to fabricate specific nanometer-scale line and space structure with uniform surface morphology.

The process started with the cleaning process where the wafer is cleaned using the RCA/BOE. In the photolithography process, the samples were coated with the resist using the spinner. After that, the sample is exposed and aligned using the exposure equipment. Lastly, the ICP-RIE will be used to etch the trimmed resist. After the etching, the samples are inspected under the HPM to see whether the resist is still in good condition or not and observed by Profilometer to see the resist been reduced its size. The process repeated until get the desire size. The samples are inspected using the SEM tool which is shown in Figure 18, it shows that the rectangular shape is the resist that had been developed and its thickness.

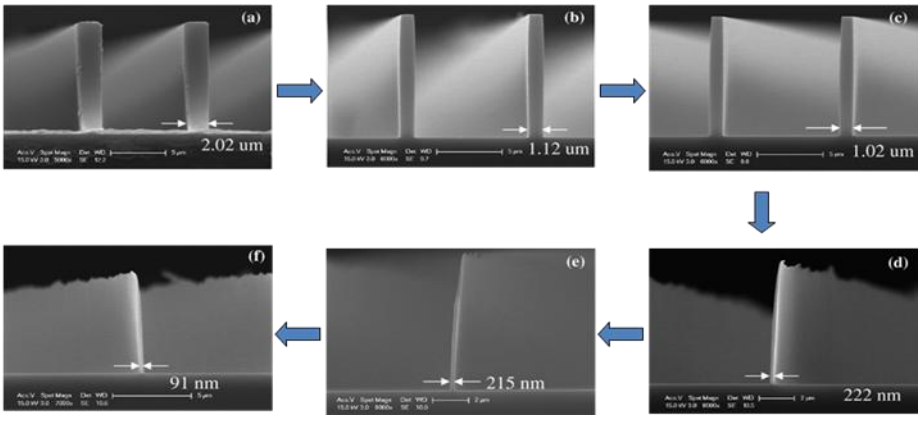
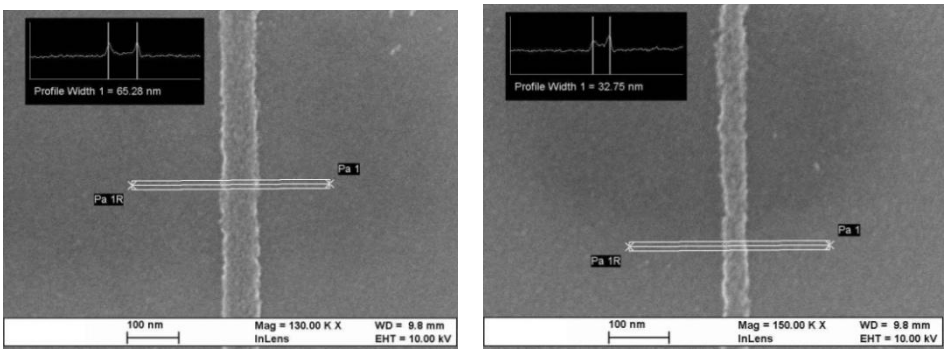


Figure 18: Process Flow for Size Reduction Lithography (SRL)

5. Type of Nanostructure

5.1 Nanowires

A very small nanowires can be produced by using a Top-Down Nanofabrication Method which involved Scanning Electron Microscope (SEM) based Electron Beam Lithography (EBL) method. Initially, the Top-Down Nanofabrication Method based on EBL was the design of the Nanowires Pattern Design (NPD). The NPD has been done by software called RAITH ELPHY Quantum GDSII Editor. The NPD is designed in various nanowires scale size from 100 nm down to 20 nm. Next, the nanofabrication process flow development which consists of the detailed parameters and recipes are developed for nanowires formation. Fabrication of Nanowires is main focus on the work which consists of SiO_2, Si, a-Si Nanowires. SiO_2 Nanowires is used as insulation and hard mask for silicon etching in order to form Si Nanowires. Si Nanowires and a-Si Nanowires are widely used as semiconducting nanowires and has great potential in nanoelectronic devices. In order to produce very small nanowires, the dimensions, developments, etch profiles of nanowires and size-reduction by thermal oxidation was investigated. Finally, the combination on Top-Down Nanofabrication Method and size-reduction has resulted in successful reduction of Si Nanowires reduced from 100 nm to approximately 20 nm which is shown by SEM image in Figure 19.

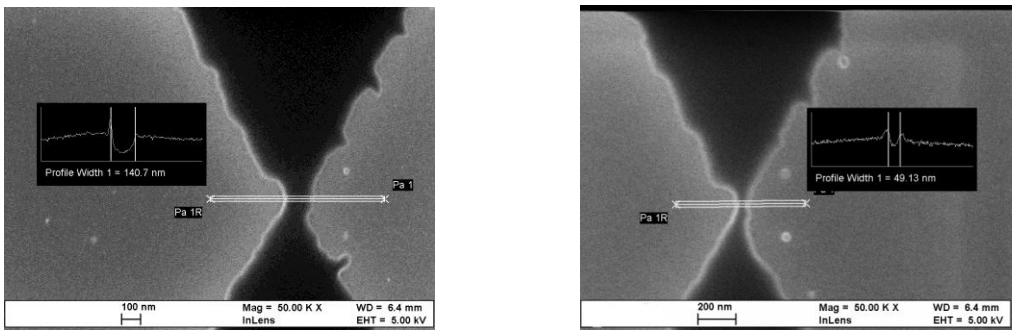


(a) (b)

Figure 19: Image of silicon nanowire under SEM (a) 65.28nm, and (b) 32.75nm

5.2 Nanogap

Nanogap electrodes are fundamental building blocks for the fabrication of nanometer-sized devices and circuits. There are simply two closely spaced electrodes, where the gap is of nanoscale dimension with sizes ranging from 10 to 60nm.The proposed process steps of Al electrode with polysilicon microgap fabrication are starting by cleaning the Si wafer before deposit 150nm SiO_2 substrate on Si wafer by using PECVD equipment. Then, use LPCVD equipment to deposit 600nm polysilicon layer to perform a layer of 135nm Al substrate as a hard mask to avoid damage of the polysilicon layer during the etching/ RIE process. Next, in the photolithography process, a layer of positive photoresist is first applied on to the Al surface, and then exposed to ultraviolet light through a mask. After development only the unexposed resist will remain, and then wet etching process of AL layer is performed before removing the resist. After that, applied dry etching process for polysilicon layer to fabricate the microgap for the micro structure, then a layer of 135nm Al substrate is deposited before the resist coating process. After exposing mask 2 the layer of the resist is developed, and then wet etching process of Al substrate is performed before removing the resist. Finally a structure of the Al electrode with a-silicon micro gap is obtained as in Figure 20.



(a) (b)

Figure 20: Image of lateral nanogap under SEM (a)) nanogap with 140.7nm, and (b) nanogap with 49.13nm

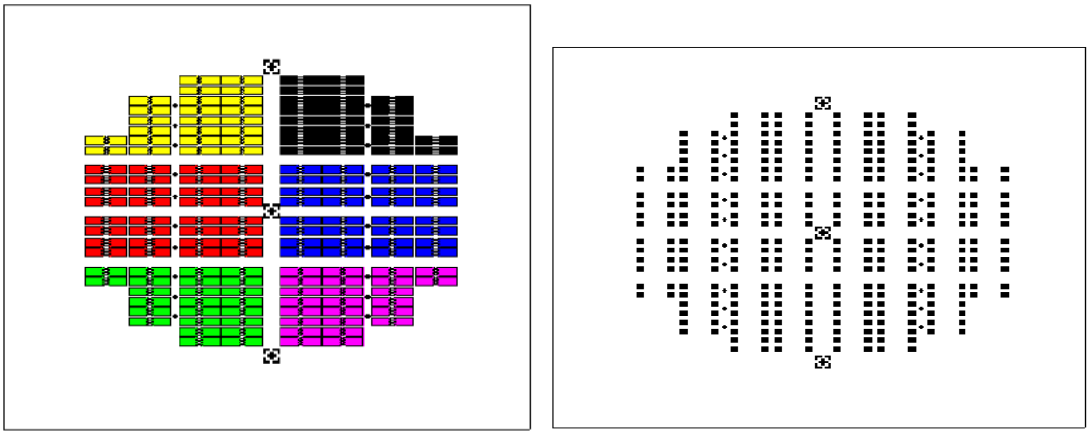
6. Development of Nano-Biosensor

In the past two decades, the biological and medical fields have seen great advances in the development of nano-biosensors and biochips capable of characterizing and quantifying biomoleculs. Nano-biosensor act like a biosensor where both of them convert the biological response to a processable and readable signal. But the advantages of Nano-biosensor over normal biosensor are label-free, ultrasensitive, smaller device and near real-time operation.

Biosensor is a device that can be widely used in several type of field such as food, agriculture and human cell. The concept of the bio-molecule detection is due to the idea of immobilization and hybridization of the cell or nucleic acid on the transducer. Nano-biosensor is mainly used in the detection of biological element such as nucleic acid, cancel cell and enzyme. With the ultrasensitive of the nanostructure to the biological element, cancel cell can be detected in the early stage, i.e. stage one or stage two.

6.1 Nanogap Biosensor For Halal Product Detection Kit

In this fabrication process, 2 masks designs are proposed which are shown in Figure 21. First mask is the lateral nanogap with gold electrode and the second mask is for pad gold electrode pattern.



(a) (b)

Figure 21: The actual mask (a) mask 1 is used to develop the lateral nanogap gold electrode and (b) mask 2 is used to develop the pad gold electrode pattern

The processes of gold electrode and gold nanogap fabrication are shown in Figure 22. First, Si_3N_4 layer is deposited onto the Silicon substrate as we can see in Figure 22(c). Then, before continuing with silicon oxide deposition, a layer of Ti/Au is deposited on the, Si_3N_4 surface layer. For photolithography process, positive photo resist is used to coat on the gold surface, and then exposed to ultraviolet light through mask1. After development, only unexposed resist will remain on the sample. Figure 22(k) shows the resist pattern after development process. An etching process is introduced to the Ti/Au layer before removing the resist layer. Then the wet etching for the SiO_2 layer and final structure of the gold electrode with gold nanogap fabrication which is obtained in Figure 22(m).

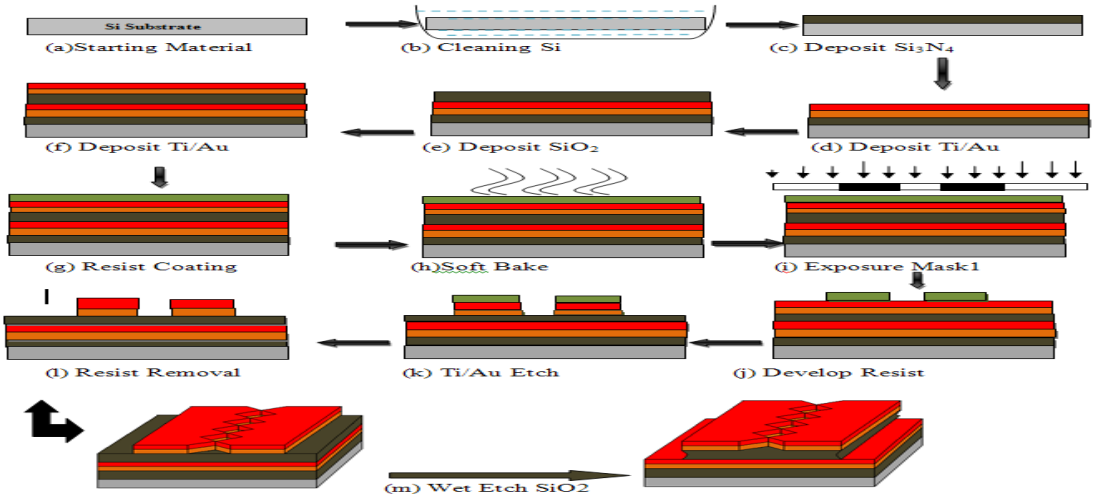
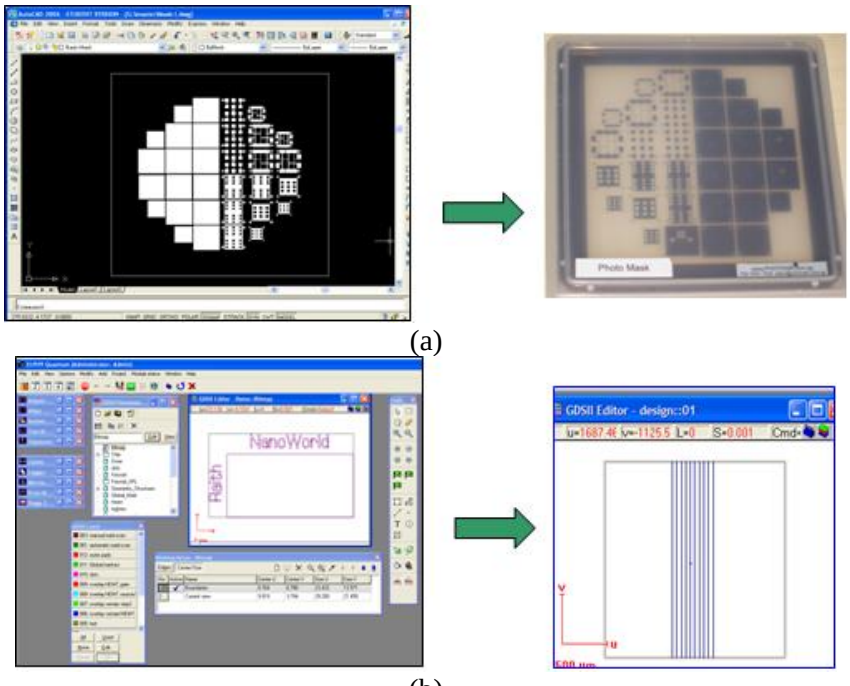


Figure 22: Gold Electrode with Gold Nanogap Fabrication

6.2 Nanowire Biosensor For Bio-molecule Detection

There are three masking steps that used in this fabrication process namely alignment mark for mask 1, silicon nanowire for mask 2 and metal pad for mask 3 (shown in Figure 23(a)). The alignment mark and metal pad were designed using AutoCAD. Nanowire pattern was designed using GDS II Editor Software (shown in Figure 23(b)).



(a)

(b)

Figure 23: (a) AutoCAD design fabricated on chrome mask (b) nanowire pattern design using GDS II Editor Software

In the first step of fabrication, standard cleaning procedure using RCA1, BOE, and RCA 2 is used to remove organic and inorganic contaminant on the samples surface. Then, the samples are baked using conduction hot plate at 200°C for 5 min to

remove residual water and cool down in room temperature in 60 min. Before patterning for the nanowire using electron beam lithography, the etch alignment marks are defined by optical lithography followed by reactive ion etch (RIE). Subsequent to alignment marks formation, negative tone ma-N 2403 resists are spun at 3000 rpm for 30 s. The coated sample is prebaked on the hot plate at 90°C for 60 s. After cool down to room temperature, the resist film is exposed using electron beam lithography system. After exposed, the sample is developed in ma-D 532 solution for 30s followed by rinse in DI water for 5 min. The exposure times to perform this nanometer scale features are short to due to the high electron sensitivity of ma-N 2403. Then, the micrometer size features are defined by optical lithography using positive photoresist. This method is used for fabricated electrode pad which is started with resist coating on the Au layer, follow by prebake on the hot plate at 90°C for 60 s, expose at Mask aligner and UV radiator for 8s and development in resist developer RD6. Lastly, the pattern creation and visual inspection take place for the patterned profile using High Power Microscope and SEM. The fabrication process of this work is shown in Figure 24.

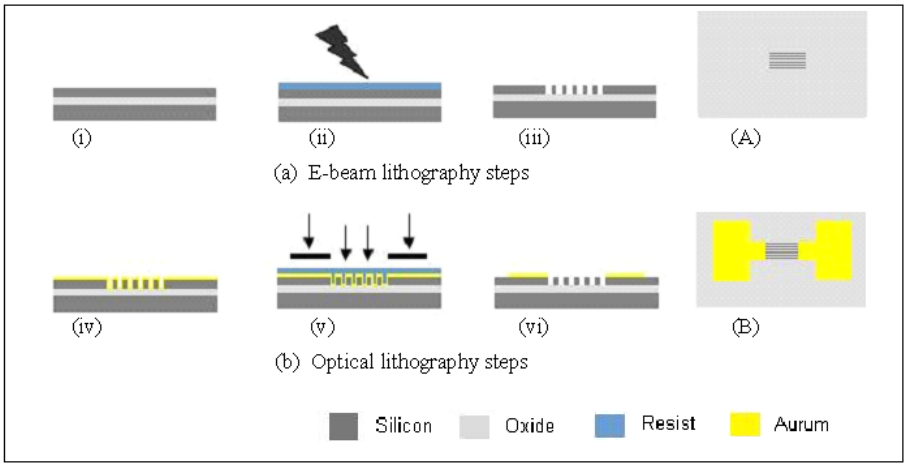
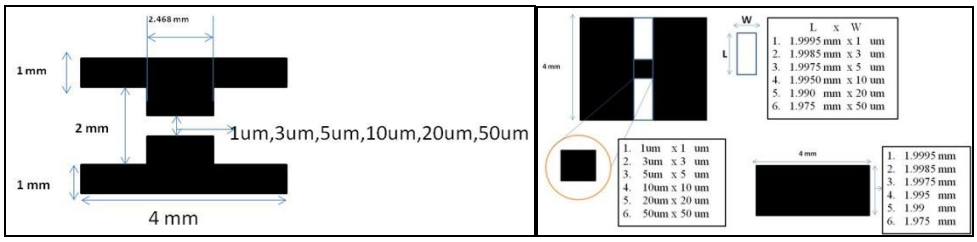


Figure 24: Experimental scheme of electron beam lithography coupled with optical lithography.

6.3 ZnO Nanowire For E-Nose Application

The purpose of this research is to explore the possibility to detect VOCs that are emitting from agarwood oil using ZnO nanowires by sol-gel process. The sensing properties of nanowires towards volatile organic compound present in agarwood oil will be studied using different I-V curves as well as different photo luminance spectrum. When air and volatile organic compounds are present they produce different curves and easy for chemical identification process. ZnO nanowires have smaller diameter therefore large surface area that increases the interaction of VOCs. As shown in Figure 25, 2 masks is designed in this research which are opening window for nanowire for mask 1 and gold electrode formation for mask 2.



(a) (b)

Figure 25: Masks for E-Nose Fabrication (a) opening window for nanowire, and (b) gold electrode formation

Starting with the Silicon in step 1, a gold layer will be deposited on silicon wafer as shown in step 2 and 10µm thickness of positive photoresist pattern layer is defined with photolithography method as shown in step 3 and 4. Step 6 is the etching of gold. In the next step ZnO will be deposited on the area from where the gold is etched away, after depositing the gold photoresist will be striped away and ZnO will left only on certain define areas. After striping the photoresist the next step will be the hydrothermal growth of nanowires. In the hydrothermal growth process zinc nitrate hydrate will be mixed with HMT solution. After preparing the solution the seeded substrate will be put in the solution so that the seeded solution face down, put that beaker or bottle in oven at certain temperature for few hours. After few hours nanowires will be grown on the selected area wash the wafer with deionized water (DI) for 2-3 times. The entire fabrication step is shown in Figure 26.

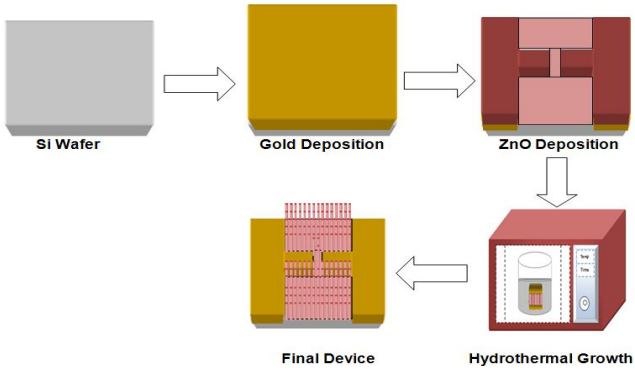
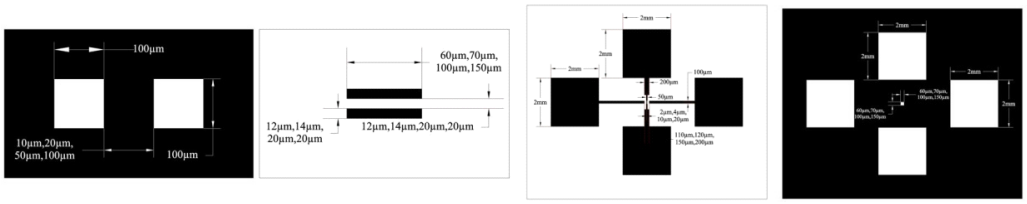


Figure 26: Process flow of gas sensor for E-Nose application

6.4 Nano BioFET For Early Detection of Cancel Cell

In this Nano BioFET fabrication process, it consists of four masks which were designed and printed on the chrome mask. With the nanowire as smaller as 40nm in width was fabricated with the spacer patterning lithography (SPL) technology, its surface-to-volume ratio is larger than the micronwire. Therefore, this novel design of this Nano BioFET has the advantage of label-free, ultrasensitive, smaller device and near real-time operation.



(a) (b) (c) (d)

Figure 27: Masks for BioFET Fabrication (a) Source and Drain Formation, (b) Nanowire Formation, (c) Gate and Contact Layer Formation and (d) Metallization and Testing Area Formation

In the fabrication process flow, the first mask will use to define the active area (source and drain) of the Nano BioFET. In this process, a controlled amount of dopant (boron) will introduce into the selected region using furnace for 30 minutes at 1100°C. This process is undergone with nitrogen and oxygen gas flow of 1L/min and 0.5L/min respectively. The second mask will define the nanowire for bio-molecule detection. The width of the nanowire is varied from 40nm to 200nm. In this research, the nanowire will fabricate using SPL method which has the advantages of low-cost and compatible to standard CMOS fabrication process. Prior to characterization and electrical testing, contact point will form by deposition of aurum (gold) material to the fabricated source, drain and nanowire. A thin layer of 1µm thick of aurum will deposit using E-beam evaporator onto the wafer surface. Then aqua regia will use to etch the aurum between the patterns. Finally, the gold pad will expose as contact point. The last mask will define an opening area for the DNA testing and also the contact area for source, drain and gate. This passivation layer will be formed by Si_3N_4 with the thickness of 1µm and it will use to isolate the testing area and the electrical contact point. This layer will be deposited using PECVD. Then ICP-RIE will use to etch the Si_3N_4 for creating the area for DNA sample drop and contact point. The entire fabrication process is shown in Figure 28.

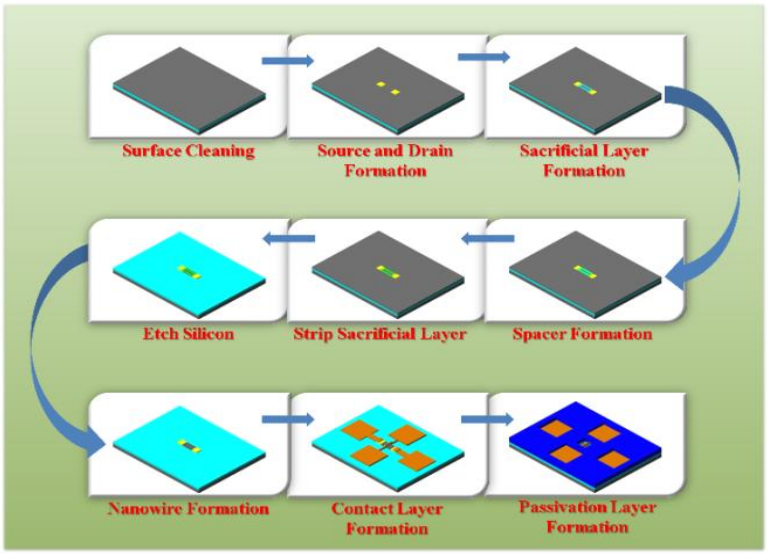


Figure 28. BioFET process flow

7. Conclusion

The ability to fabricate nanodevices and nanostructures with the smallest resolution and fidelity is fundamental to all future research activities. Nano Biochip Research Group from Institute of Nano Electronic Engineering (INEE) in UniMAP has demonstrated the application of e-beam is the core of today's nanofabrication technology. With the success of the current research in nanoelectronics field, it is believe that Nano Biochip Research Group will focus and lead their research towards nano-biosystem or Lab-On-Chip in the near future.

8. References

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