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Effect of alignment mark depth on alignment signal behavior in advanced lithography

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ABSTRACT

Finding a robust alignment strategy is one of the key evaluations in defining photolithography process. Alignment is a process to determine how the current pattern is placed on the wafer. Alignment is done by an optical system, which means that it is dependable on the quality of the alignment signal to determine the correct orientation. Alignment signal is generated by alignment mark, a diffraction grating structure (trench and line structure) printed on wafer. Hence, the processing steps can possibly affect the properties of alignment mark. The alignment mark depth (trench depth) can be varied due to the nature of processing. According optics, a light optical path variation may lead to a destructive interference, which is not good.

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Keywords: *Alignment signal, lithography, Alignment mark*

INTRODUCTION

The challenge in photolithography process is to print the desired feature size and to align the feature correctly to the subsequent layer [Rigorous Coupled wave analysis of FE of line wafer alignment marks]. It is important to ensure that the new pattern is overlaid the previous pattern correctly. Designing a robust alignment strategy is difficult and time consuming since the scanner alignment system is designed to work with an ideal profile of alignment mark. There have several factors can affect the alignment signal significantly which is size of alignment mark, polarity, processing steps, type of alignment system, refractive index, reflectivity, grain structure, and surface roughness [Laser Alignment Modeling Using Rigorous Numerical Solution]. This paper will concentrate on how processing steps affect the alignment signal behavior.

Previous work by [Experimental and simulation studies of alignment marks] stated that alignment signal is a strong function of trench depth. From [Segmented Alignment Mark Optimization and Signal Strength Enhancement for Deep Trench Process], for a rectangular grating profile, the intensity is given by;

$$I = \frac{4}{\pi^2} I_0 R \sin^2\left(\frac{\pi r}{r+1}\right) \sin^2\left(\frac{\alpha}{2}\right) \tag{1}$$

where I0: the incident radiation intensity

R: the reflection coefficient.

r: the ratio between area of the higher and lower lines of the phase grating.

α: optical phase difference between light reflected from the higher and lower lines of the grating.

Besides the perfection of alignment system, stray light can leak into the alignment system. If the mark depth is small, or the duty cycle is low, the relationship between the alignment signal intensity and the stray light intensity becomes critical. Too much stray light in the alignment system leads to unreliable alignment results. To small mark depth also makes the alignment mark visibility is lesser. Reducing the visibility weakens alignment signal strength, increases the probability of overlay error, alignment system failure, and rework [Optical Flatness and Alignment Mark Contrast in Highly Planar Technologies].

The behavior of alignment signal over a range of mark depth is depended on the laser wavelength. Theoretically, a reduction in signal strength occurred when the alignment mark depth value is in range of multiple lambda/2 [Experimental and Simulation Studies of alignment mark]. According physics theory; this is a point where a destructive interference occurred.

ALIGNMENT MARK FORMATION FOR CONTACT LAYER (CONTACT MARK)

Alignment mark is printed on the wafer. This means that it is going through exactly the same process as the rest of the circuit structure. The first step in order to produce a contact structure is to deposit oxide material at certain required thickness. Since the deposition process does not produce a flat surface, hence, planarization process is required. Then, the oxide material will go through a

patterning and etch process to produce the desired shape. Figure 1 illustrate the post lithography and etch process alignment mark.

Figure 1. Post lithography and etch contact alignment mark.

After that, tungsten material will be deposited. Tungsten material has to be completely removed from oxide upper surface. Tungsten is removed through chemical mechanical planarization (CMP) process. Contact hole will be completely filled by tungsten due to its small feature size. However, alignment mark trench won't be completely filled since its trench size is much larger than the tungsten deposition thickness (Figure 2). Figure 3 illustrates the alignment mark profile after tungsten planarization process.

Figure 2. Alignment Mark Profile after Tungsten Deposition.

Figure 3. Post Tungsten CMP Profile.

Finally, metal/aluminum layer will be deposited on the existing structure through physical deposition process (PVD). Usually, the asymmetric profile becomes significant after this process. Figure 4 shows the possible profile after metal layer is deposited. This is final profile of contact alignment mark. The reflected signal behavior during metal1 layer alignment depends on this profile

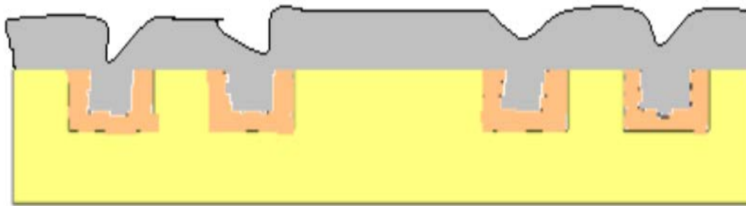


Figure 4. Post Aluminum/Metal Layer Deposition Profile

From description above, alignment mark depth variation is influenced by final oxide thickness, tungsten deposition thickness, and tungsten planarization time.

RESEARCH METHODOLOGY

Based from the conclusion of the previous section, an experiment was designed in order to investigate how various processing steps affect the alignment mark depth and eventually alignment signal performance. Each of the alignment mark will be evaluated for each particular condition.

Table 1. Process Split based from DOE

Split	Final ILD CMP Thickness	Tungsten Deposition Thickness	Tungsten Planarization Time
A	9200	3200	60
B	7800	2800	0
C	8500	3000	30
D	7800	3200	60
E	7800	2800	60
F	7800	3200	0
G	9200	3200	0
H	9200	2800	0
I	9200	2800	60

Oxide measurement will be measured right after ILD planarization and after tungsten planarization process. This measurement is important so that the theoretical alignment mark depth can be calculated. In this experiment, three main types of alignment mark were used which are AH32, AH53, and AH74. Please refer to table 2 for the details of alignment mark used in this experiment. Alignment signal strength behavior is represented by Wafer Quality (WQ) parameters.

Table 2. Alignment Mark Type and their optimized light order recipe

Mark Type	Subtype	Architecture Type	Optimized light Recipe
AH32	AH32-CON-PRI	No Poly Block	Third Order Light
	AH32-CONPLB-PRI	Poly Block	
AH53	AH53-CON-PRI	No Poly Block	Fifth order Light
	AH53-CONPLB-PRI	Poly Block	
	AH53-CV2V4-NPLB	No Poly Block	
	AH53-CV2V4-SCR	Poly Block	
	AH53S-CV2V4-SCR	Poly Block	
AH74	AH74-CON-PRI	No Poly Block	Seventh Order Light
	AH74-CONPLB-PRI	Poly Block	
	AH74-CV2V4-SCR	Poly Block	
	AH74DC60-CV2V4	Poly Block	

RESULT AND DISCUSSION

Alignment mark is a reflected diffraction grating structure. Hence, the signal behavior generated by alignment mark follows the diffraction rules. Equation 1 suggest that there have four factors may affect the reflected light intensity from alignment mark, which is incident radiation intensity, the reflection coefficient, the ratio between area of the higher and lower lines of the phase grating, and optical phase difference between light reflected from the higher and lower lines of the grating. The optical phase is interpreted as alignment mark depth (Figure 5).

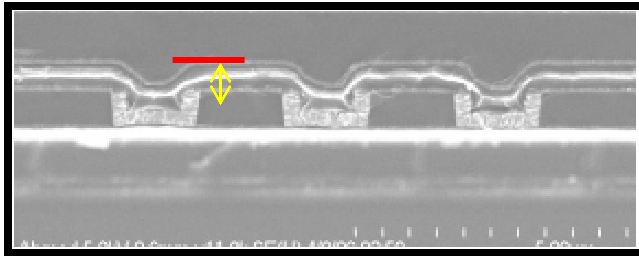


Figure 5. Cross sectional view of alignment mark. Yellow mark shows an alignment mark depth.

In this work, alignment mark depth is calculated based from oxide/metal stacking.

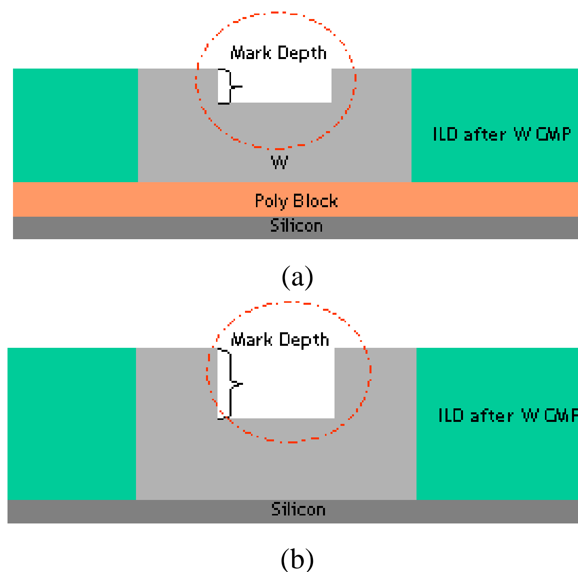
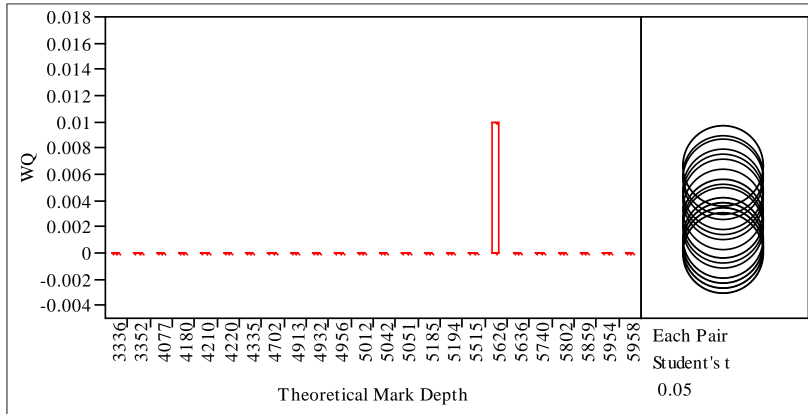


Figure 6. Alignment Mark Structure (a) Poly Block Alignment Mark Structure (b) No Poly Block Alignment Mark Structure.

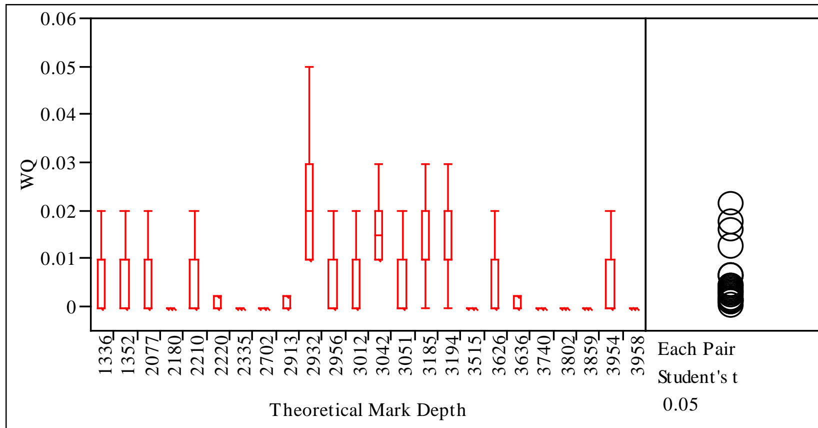
Depending on whether the alignment mark structure consists of poly block or not (refer to Figure 7 for stacking details), the alignment mark depth is calculated based from equation 2 and equation 3.

Theoretical Alignment Mark Depth = Final Oxide Thickness (post CMP Inter Layer Dielectric (ILD)/Inter Layer Metal (IMD) –
Tungsten Deposition – Oxide Loss during Tungsten
CMP – Poly Block Thickness (if exist) (2)

Oxide Loss during Tungsten CMP = Final Oxide Thickness (post CMP Inter Layer Dielectric (ILD/Inter Layer Metal (IMD) –
Final Oxide Thickness after Tungsten CMP (3)

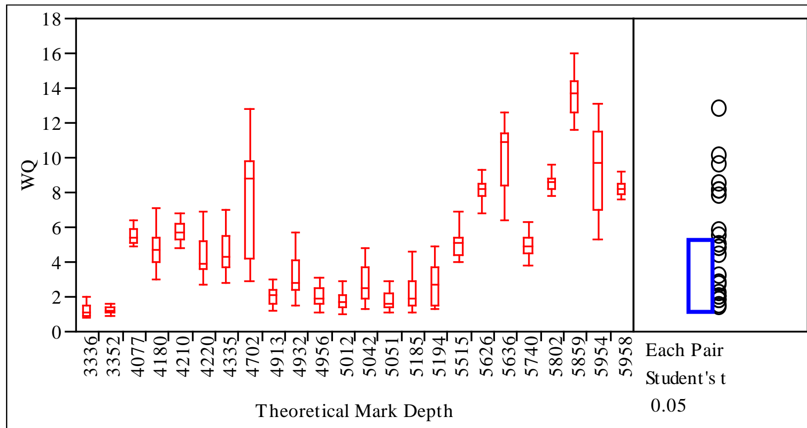


(a)

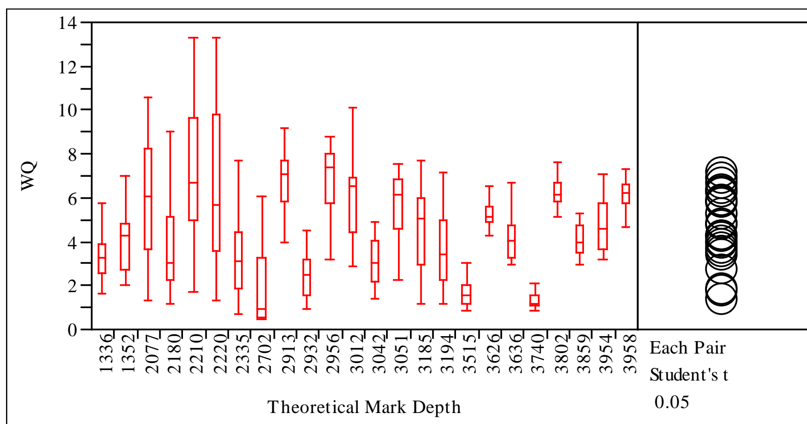


(b)

Figure 7. AH32 Alignment Mark Type vs. Mark Depth. (a) AH32-CON-PRI (b) AH32 CONPLB-PRI.



(a)



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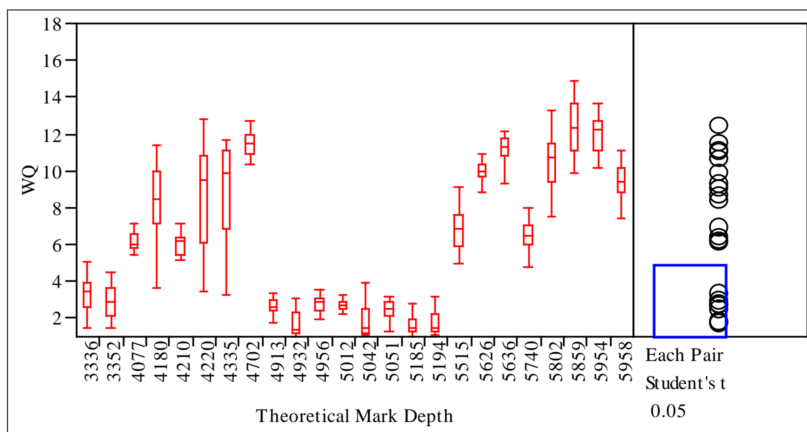

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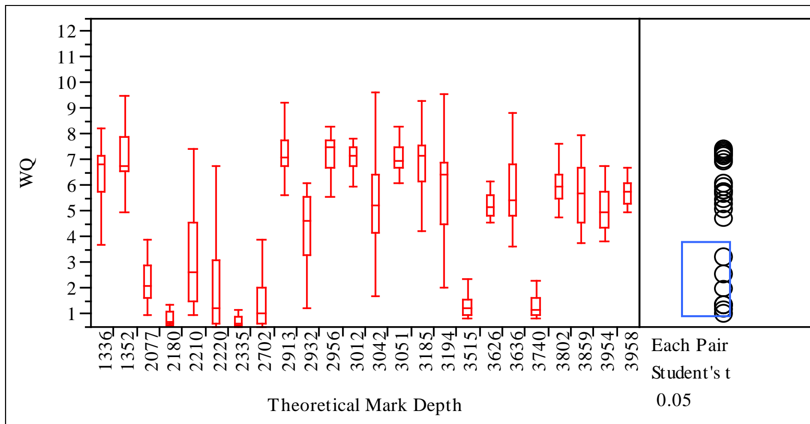

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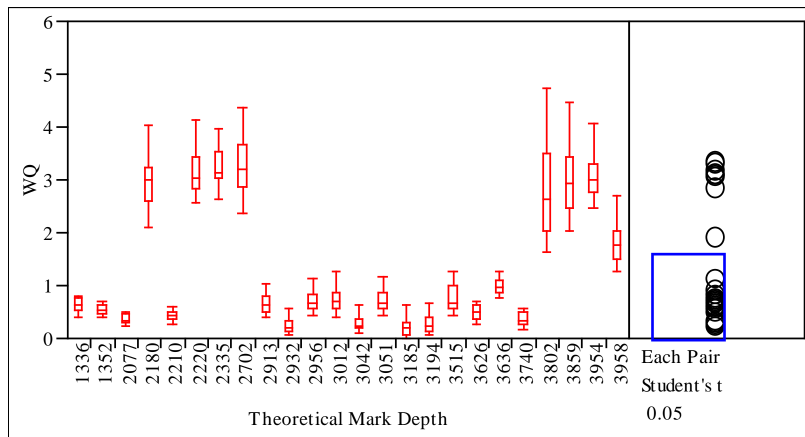
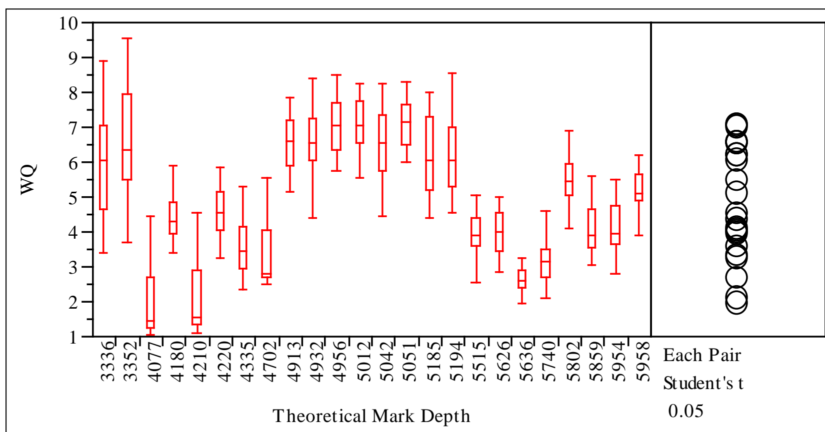
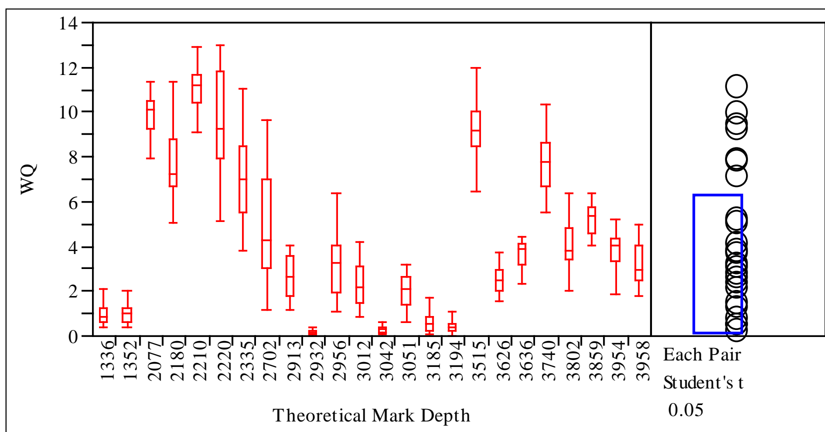


(e)

Figure 8. AH53 Alignment Mark Type vs. Alignment Mark Depth (a) AH53-CON-PRI (b) AH53-CONPLB-PRI (c) AH53-CV2V4-NPLB (d) AH53-CV2V4-SCR (e) AH53S-CV2V4-SCR



(a)



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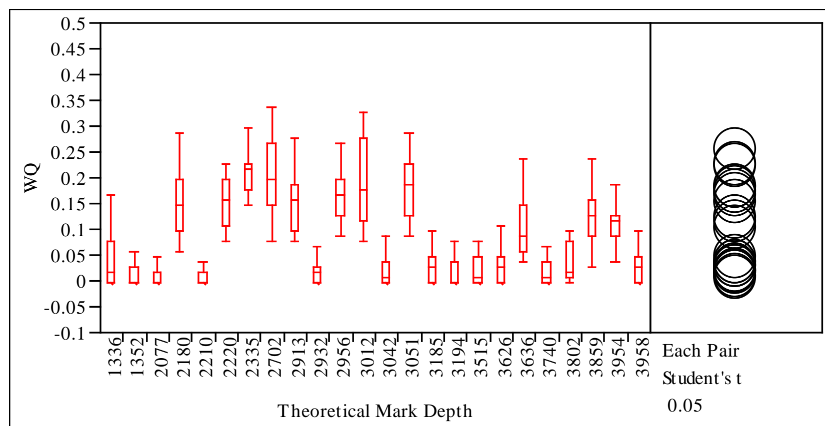

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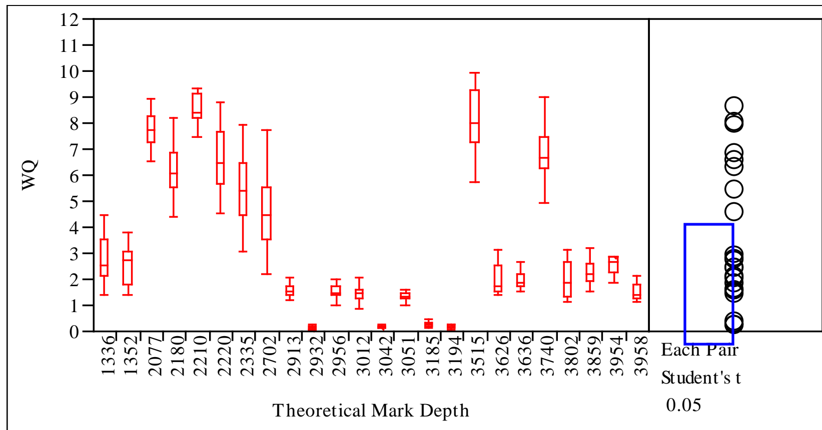

(d)

Figure 9. AH74 Alignment Mark Type vs. Alignment Mark Depth (a) AH74-CON-PRI (b) AH74-CONPLB-PRI (c) AH74-CV2V4-SCR (d) AH74DC60-CV2V4

Figure 7 shows the signal strength trend for AH32 mark plotted with respect to theoretical alignment mark depth. Basically, there is no trend over the alignment mark depth variation for both AH32 mark since the signal strength is almost zero. Excluding AH53-CONPLB-PRI and AH53-CV2V4-SCR mark, the rest of the AH53 alignment mark shows a signal variation trend as the alignment mark depth also varied (Figure 8). From t-test, their signal variations are significant. Even though there is a significant difference signal variation for AH53-CV2V4-SCR as shown in Figure 7d, there is no physical trend observed on the Figure 7d graph. From Figure 8, all AH74 mark type except AH74-CV2V4-SCR shows a significant signal variation (From t-test) with respect to the alignment mark depth variation. AH74-CV2V4-SCR mark have an overall zero signal strength throughout the mark depth variation.

Table 3.Theoretical Alignment Mark Depth where the signal starts to degraded/increasing compared to signals at other mark depth.

Alignment Mark Type	**Theoretical Mark Depth at point where alignment signal degraded/increasing**
AH32-CON-PRI	-
AH32 CONPLB-PRI	-
AH53-CON-PRI	4913-5194
AH53-CONPLB-PRI	-
AH53-CV2V4-NPLB	4913-5194
AH53-CV2V4-SCR	-
AH53S-CV2V4-SCR	2913-3740
AH74-CON-PRI	4913-5194
AH74-CONPLB-PRI	2913-3194
AH74-CV2V4-SCR	-
AH74DC60-CV2V4	2913-3194

Generally, the alignment signals starts to degrade at 4913Å to 5194Å range and 2913Å – 3740 Å (Table 3). All mark given in Table 3 is only theoretical values calculated based from process stacking. More or less, this behavior are truly reflected the actual situation during alignment.

CONCLUSION

From the results, there is a degradation of signal strength over a range of alignment mark depth. Unfortunately, alignment mark depth could not be controlled since it is dependent on process characteristics such as oxide thickness and over polish time. This parameter cannot be simply changed since it may impact the overall production yield. The best that can be done is to find a selection of alignment mark, which is less sensitive to the alignment mark depth variation.

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