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Fabrication and characterization of p-type double gate and single gate junctionless silicon nanowire transistor by atomic force microscopy nanolithography

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Abstract

The fabrication of Double gate (DG) and Single gate (SG) Junctionless silicon nanowire transistor (JLSNWT) was investigated in this research. The transistors used silicon nanowire patterned on lightly doped (10^5 cm^{-3}) p-type silicon-on-insulator (SOI) wafer fabricated with an atomic force microscope (AFM) nanolithography technique. The top Si layer has a thickness of 90 nm and a resistivity (ρ) of 13.5-22.5 Ω cm. The modified RCA method implemented for sample preparation. The local anodic oxidation (LAO) followed by two wet etching steps, KOH etching for Si removal and HF etching for oxide removal, have implemented to reach the structures. The writing speed and applied tip voltage were held in 0.6 μm/s and 8.5 volt respectively. Scan speed was held in 1.0 μm/s. The etching processes were elaborately optimized by 30% wt. KOH + 10% vol. IPA in appropriate time, temperature and humidity. The structure is a gated resistor turned off based on a pinch-off effect principle, when essential positive gate voltage is applied and made a sufficiently large barrier in the gating region. Negative gate voltage is unable to make significant effect on drain current to drive the device into accumulation mode.

Keywords: Local anodic oxidation (LAO), silicon-on-insulator (SOI), atomic force microscope (AFM), double gate (DG) and single gate (SG) junction-less silicon nanowire transistor (JLSNWT).

1. Introduction

Departing from microelectronic to nano-electronics is one of the crucial areas in nanotechnology. Relevant obstacles rise up from this departing process could summarize in two main problems; fabricating the structure and understanding the transport phenomena. Among the several types of nanotransistors, scaling down the size of transistors and the gate length of MOSFETs created some issues such as short channel effect (SCE), leakage current

or very low current. Several methods suggested to conquer these problems, such as high κ dielectrics [1-2], metal gate electrodes [3], and new transistor architectures based on silicon-on-insulator (SOI), such as FinFETs [4], multigate FETs [5] or gate-all-around FETs [6]. Junction less transistors (JLTs) can be a reliable alternative for the conventional scaled MOSFETs. The JLTs have a constant doping concentration through the source, channel and drain. From the first JLT [7] until recent alternatives for SOI-JLT [8-9], high doping concentration have always been recommended, in order to compensate the low number of charge carriers in the channel. But high doping always gives rise to strong unavoidable scattering effect and also increases subthreshold swing (SS) fluctuation. JLTs appeared to be the new and promising alternative for new generation of transistors [7, 10]. In the last two years, the research in JLTs focused to design and property [9, 11-12], simulation [13-14], high temperature performance [15], new fabrication method of the device with higher mobility and better performance [16-17].

The principle of AFM nanolithography, using Local anodic oxidation (LAO) on SOI, has been described for the first time by Snow and Campbell *et al*. [18-19]. Ionica *et al*. [20] have remarkably reported the electrical characteristics of the devices made by AFM nanolithography. Also some recent works were performed to improve the method of AFM nanolithography [21-22]. However, the lack of sufficient explanation for the behaviour of these structures is still an interesting issue. It was already reported that the fabrication of the p-type side gate JLT device with simple structure, low doping concentration and no gate oxide layer [23-24]. The conventional MOSFETs functions are strongly dependent on the oxide layer and capacitance of the gate oxide layer, but for JLSNWTs, capacitance dependence does not have a strong effect [25-26]. Therefore, in our JLTs devices, lacking of the gate oxide layer could be acceptable. Moreover, it can eliminate the difficulty of the gate oxide layer stacking into the structure. In this work, the experimental method and investigation of the experimental of the side gate JLT device was improved with optimized geometry. The pinch-off effect for positive gate voltage and the effect of negative gate voltage on channel will be investigated as well. The numerical origin of double gate (DG) and single gate (SG) JLSNWT structure's characteristic in on state at low and high drain voltages were explored according to JLT principles.

2. Methodology

The process of fabrication of double gate (DG) and single gate (SG) JLSNWT by means of AFM-LAO nanolithography on SOI substrate will be elaborately expressed. The fabrication process is divided into three separate and major steps which are shown in Fig. 1. The important contributing parameters or factors in fabrication process can be mentioned as the cleaning and preparation procedures, AFM instrument parameters, relative humidity, KOH etching parameters, etching optimization.

2.1 Cleaning and Preparation

The first step of fabrication is the cleaning process, which was applied by modifying the standard RCA method. During optimization of the cleaning process, the ratio of chemical concentration, temperature and time are the major parameters. The standard method and other researchers suggested that the ratio of chemical 1:50 for HF:DIW. However, in our case this ratio caused some roughness on the surface of the samples. The best ratio found for our condition was 1:100 for HF:DIW. The temperature and temperature interval are also important. Any change more than 3^{o}C in temperature interval, exceeding

the temperature of 80°C or lowering below 77°C during the cleaning process would give rise to inequality or even twisting the sample surface. By applying sulfuric acid/hydrogen peroxide/deionized water ($H_2SO_4/H_2O_2/H_2O$) at 110-130°C in Piranha clean method, it was found that it did not go well with the SOI surface due to high temperature. The use of ultrasonic cleaning before applying the RCA method was very useful. Using the acetone/methanol washing before the RCA cleaning also did not produce good results.

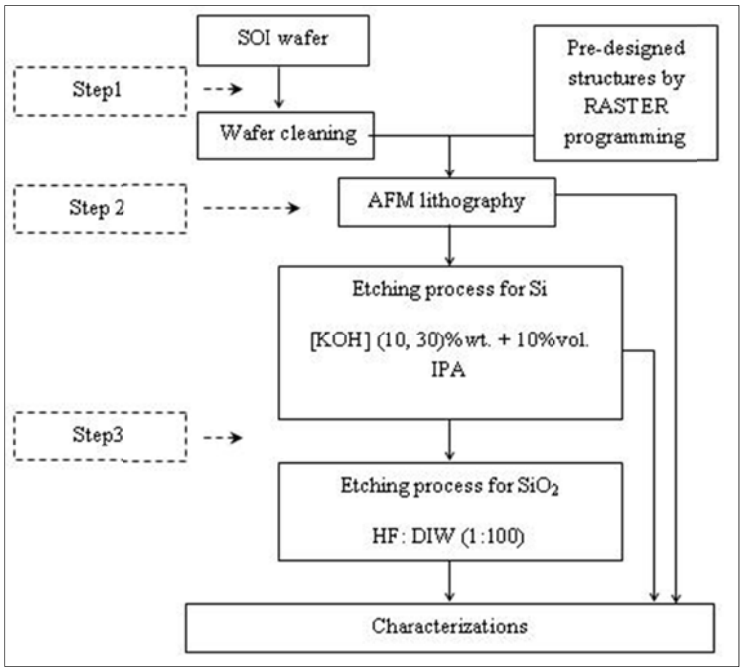

Fig. 1: Flow chart of methodology and steps of fabrication the device by AFM-LAO nanolithography.

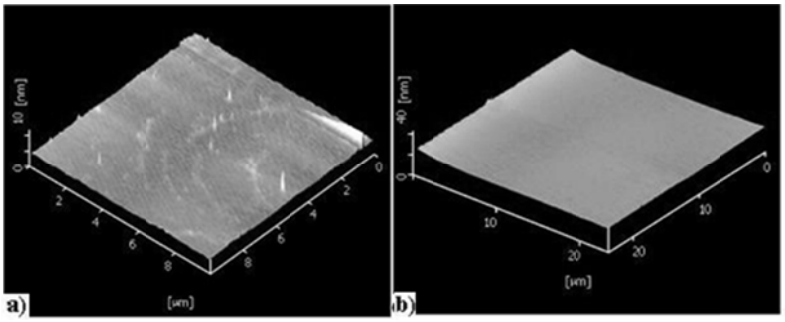

Fig. 2: AFM image of the SOI substrate (a) before, and b) after optimized RCA cleaning process, native oxide and other contamination removal is recognizable after cleaning.

The timing of immersing or even rinsing is also very important factor. For examples after each step, the sample was immediately put into the beaker containing DIW to prevent it from long time air exposure which will caused the native oxide appearing on the surface of the sample. In addition, it was also found that the type and brand name of SOI wafer can be important in each step of the cleaning. Fig. 2 shows the AFM images of the SOI sample before and after cleaning process.

2.2 Contribution of Applying Voltage on the AFM Tip and Exposure Time

The oxide growth mechanism can be described as the following [27]. After cleaning process Si-H bonds are formed on the surface and native oxide could be removed. When the surface was de-passivated, the first layer of Si-Si bonds became polarized due to high electron negativity of the OH^-. Then, the Si-Si bonds reacted to the polar H_2O molecules from humidity to form monolayer of silicon oxide, SiO_2. The oxide film thickness increased, when the OH^- drifted through the oxide film. It happened when the electric fields are created between the first silicon oxide layer and the substrate when applying a voltage on AFM tip. Not only the electrical fields enhanced the OH^- formation, but also provide the correct direction to cause the OH^- diffusion through the oxide film.

Writing speed and AFM tip voltage are two parameters to optimize the fabrication process. Fig. 3 shows the effect of applied voltage on the AFM tip at a constant writing speed of 0.6 μm/s and for different writing speeds with the same applied voltage of 8 V. High voltage (Fig. 3(a), (b)) provides thicker oxidation and more uniformity on the substrate surface. The best result was derived from the applied voltage of 8 V. On the other hand, low writing speeds can make wider oxidation effect on the substrate, whereas faster writing speed did not provide any oxidation effect on the substrate in 8V (Fig. 3(c)). For writing speeds of 1.0 and 1.5 μm/s the oxidation tracks were not recognizable. In our case, the speed of 0.6 μm/s and the voltage of 8.5 V are the optimized parameters.

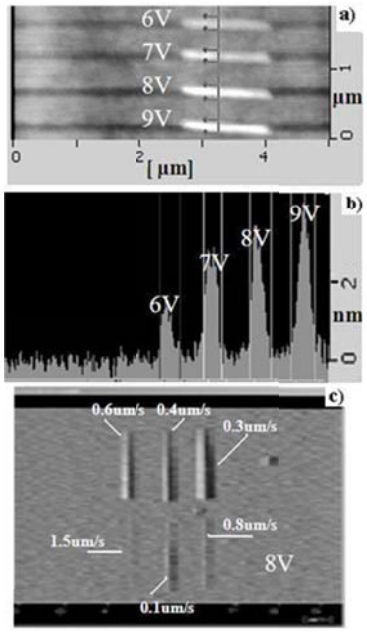

Fig. 3: Effective parameters during LAO process on different arbitrary samples a) and b) effect of different applied voltage on AFM tip and c) effect of different writing speed.

Another parameter plays an important role in LAO is the relative humidity (RH), due to water molecules in the ambient air for oxidation process. When RH% increased, the thickness of oxide increased simultaneously. The oxidation rate is very sensitive to the field strength at high RH%. The oxide thickness extremely depends on the humidity and AFM tip voltage. In Fig. 4, the relation between oxide thickness and RH% at room temperature with constant applied voltage of 8.5 V is shown.

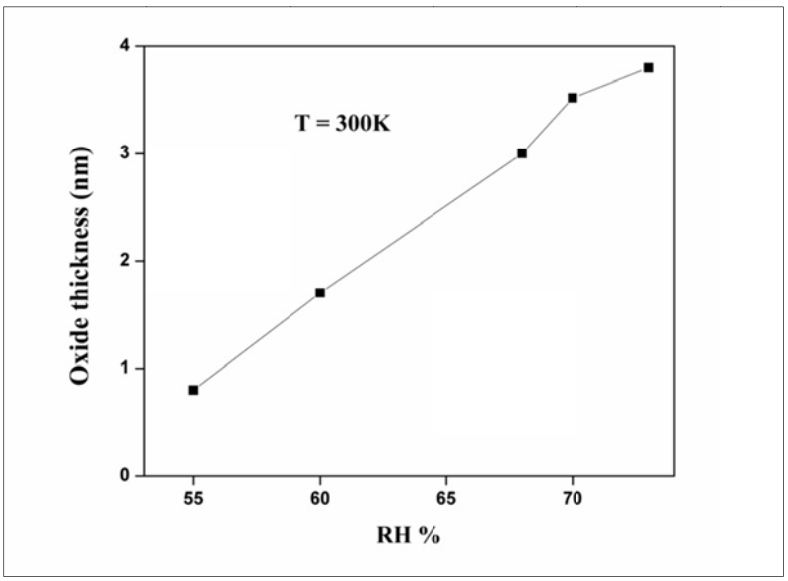

Fig. 4: Relation between oxide thickness and RH %, at room temperature with constant applying voltage (8.5 V).

Humidity and temperature are affecting the device structure during patterning. Normally to get a good pattern, the range of temperature must be $\leq 4^{o}C$ and the range of humidity must be $\leq 4\%$. From the observation during patterning, the best results were found in the range of $22 – 26^{o}C$ for the temperature and between 65-68% for the relative humidity for the Cr/Pt coated tip. In fact, after RH% increases beyond 70% the rate of increasing oxide thickness will be reduced, instead, the shadow effect was observed. These results support the previous studies on AFM nano-oxidation about the influences of room humidity in oxide growth on silicon surface when the others parameters are constant [27-29]. Fig. 5 shows the AFM topography for the pads prepared by LAO technique. The presence of the shadow around the pad can be seen, which deformed the shape. This phenomenon has been reported in several works [30] and our observation has confirmed this.

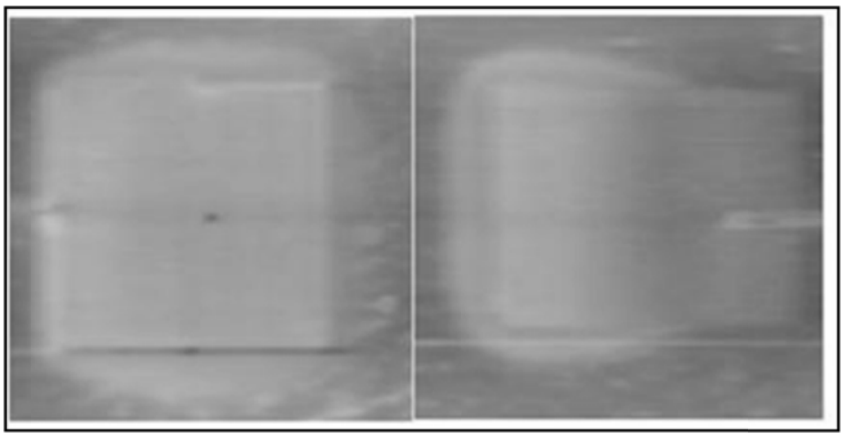

Fig. 5: AFM topography images of the pads with the shadow effect due to LAO in high RH %.

2.3 Effect of KOH Etching Process on Device Fabrication

KOH wet etching is a very significant part in the fabrication of JLSNWT. In fact, having contamination, ill-etched or over etching structure was hardly avoidable in wet etching, accordingly, the accuracy and precaution are important. To remove the undesired Si area, KOH was used as etchant. Referring to the previous reports in KOH wet etching [31-33], it can be clearly seen that the surface roughness improved as the concentration of KOH increased. At low KOH concentration, the surface was rough and the formation of insoluble precipitates can be seen. Isopropanol (IPA) was used in this work as initiator to improve the cleaning process. IPA reduced the etch rate, hence improving the surface roughness and making the etching process more controllable [32]. Moreover, the uniformity of surface roughness increased drastically when added the IPA [31, 34]. Base on this work and the literatures for optimization, the best percentage of IPA added to the solution was 10% vol. in the KOH etchant. Apart from the concentration of the etchant, the immersing time and temperature are also playing important role in obtaining the most optimum result for nanostructure formation. In Fig. 6, SEM images under the effect of etching for different KOH concentration are shown. With the solution of 30% wt. KOH+ 10% vol. IPA and immersing time of 20s (Fig. 6(a)), structure shows proper sharpness compare to the others in Fig. 6(b), (c). In Fig 6(a), (b) also can be seen for longer immersing time at the same concentration, the sharpness will be decreased. In Fig. 7, AFM topography images of the complete structure before etching and after etching (over etched) are shown. It can be seen that for the over etched sample (Fig. 7(b)) the gap between the gate and the nanowire/channel has disappeared and the gate contact expanded toward the channel and fill the gap area. In fact, it would have anisotropic etching to the structure etched with KOH + IPA [33, 35-36]. In anisotropic etching for (100) Si, the rectangular hole will be ended up in a pyramid shaped etch pit and the wall will be flat and angled. Fig. 8 shows SEM images for the different concentartion of KOH for two complete structures and over etching effect (Fig. 8(b)) on the structure for 40% wt. KOH + 10% IPA at 65^{o}C, after 30 seconds immersing time. Some parts of the structure are clearly gone due to re-etching with high concentration of KOH. It can be said that for higher concentration, over etching would be more sever compare to higher immersing time or temperature.

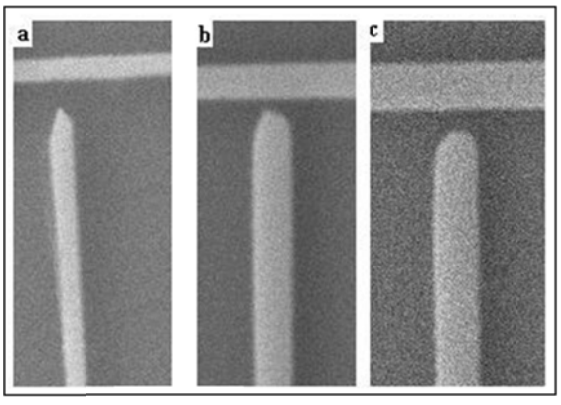

Fig. 6: SEM images of the nanowire and the lateral gate gap at room temperature, a) etched with 30% wt. KOH + 10% vol. IPA for 20 seconds, b) etched with 30% wt. KOH + 10% vol. IPA for 28 seconds, and c) etched with 40% wt. KOH + 10% vol. IPA for 20 seconds.

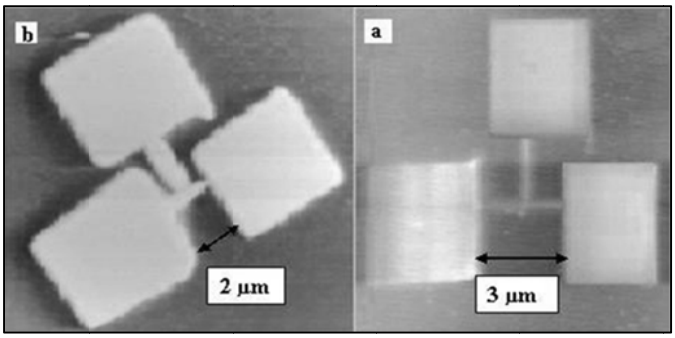

Fig. 7: AFM topography images of the structure a) before, and b) after the etching process (over etched) with the solution of 30% wt. KOH + 10% IPA at 68°C, after 30 seconds immersing time.

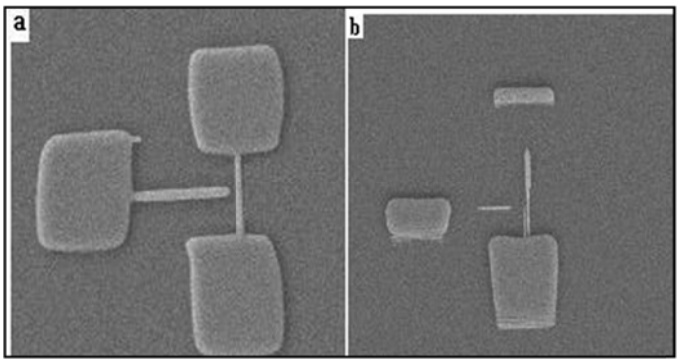

Fig. 8: SEM images for the complete structure after etching process a) etched by the solution of 30% wt. KOH + 10% IPA at 63°C, after 23 seconds immersing time, b) etched by the solution of 40% wt. KOH + 10% IPA at 63°C, after 23 seconds immersing time.

2.4 Optimum Condition for KOH Etching

In this study, previous works for optimum condition for KOH etching are considered and adopted [23, 33, 37-41]. The best condition according to the fabrication environment, clean room and other parameters is the solution of 30% wt. KOH with 10% vol. IPA for wet etching at 63°C, 20 seconds for immersing time and stirred at 600 rpm. Stirring the solution is to ensure the uniformity of the etching process.

2.5 Effect of Oxide Removal on Device Fabrication

The oxide reoval is the last step in our fabrication method. The etchant is hydrofluoric acid (HF) in aqueous solution with well-known ability to dissolve SiO_2. After etching by KOH admixture with IPA solution, the Si layer should be removed. The sample was etched with diluted HF at room temperature for 12-14 seconds and stirred at 600 rpm to remove the SiO_2 mask. During HF etching oxide removal, the oxide layer including the native oxide and the mask were removed.

2.6 Other Parameters Issues

In fabrication process, in addition of major factors like RH% or applying voltage and exposure time or cleaning and preparation process, there are some minor factors which are able to make significant effect in details. The type of the AFM tip is very important. The tip must be specified for contact mode (tapping mode and non-contact mode tips are

nonfunctional). For this case three types of contact mode tips were test, which were Au coated, Cr/Pt coated conductive probe and Al reflex coating. Regarding to the particular condition of the experiment, the best result extracted by Cr/Pt coated conductive probe. The coating layer also enhances the laser reflectivity of the cantilever. In fact gold (Au) coated probe also showed the acceptable result [23, 33, 42], but with Cr/Pt coated conductive probe tip got is more reliable result.

Another issue is the order of oxidation. By experiment, it was learnt that the whole pattern structure cannot be made in one time unless, proper humidity in ambient air already been provided. Fig. 9 shows that the second pad (right side) is ill-shaped due to the lack of proper humidity in ambient air to make the perfect LAO.

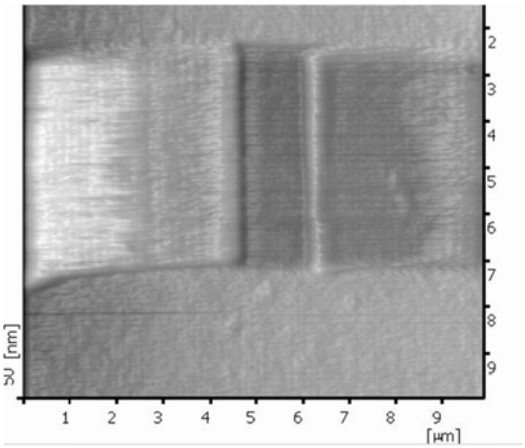

Fig. 9: AFM image of successive LAO for two pads the right pad is ill-shaped due to the lack of proper humidity in ambient for LAO.

The unwanted native oxide layer on the top of the sample a while after the fabrication should be considered, even though the sample was keep at dryer cabinet. The native oxide could be probably the important reason for Hysteresis effect reported for work [24]. The one of the important issue faced during the fabrication was in KOH etching for uncovered Si layer removal. It could be very tricky and sometimes it depends in the surface property. For example, the immersing time or temperature for KOH etching for Si removal and HF etching of (001) Si wafer is different with another orientation [43]. In Fig. 10, SEM images for the over etching effect of high concentration of KOH+IPA are shown. It can be recognized that some parts of the structure were removed.

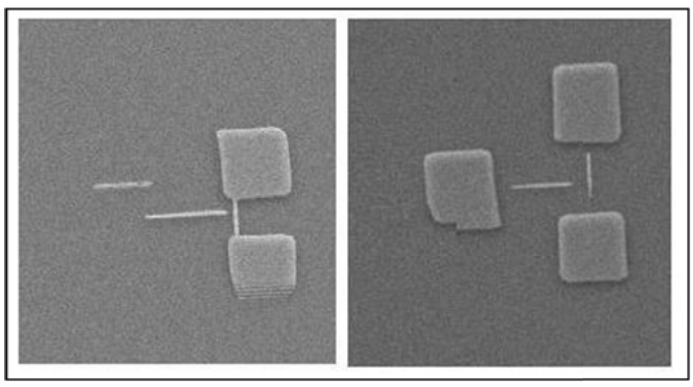

Fig. 10: SEM images for over etched sample after KOH and HF etching.

3. Results and Discussion

Fig. 11 shows the AFM and SEM images of profile analysis and topographic picture of DG and SG JLSNWT. In Fig.11(a), the whole structure of the source, channel and the drain are uniformly doped and made of p-type SOI with 90 nm thickness of the Si layer. Accordingly, the source, drain and channel would have the same thickness. Both devices have 100 nm for the channel width, the gate gap of 100 nm, 200 nm for the channel length and 4 μm for the distance between the source and drain. The sample shown in Fig 11(c), (d), with the channel intentionally located closer to the gate and not in middle of the source/drain side, displayed better performance and less leakage current compared to our previous works for SG structure [23-24, 33].

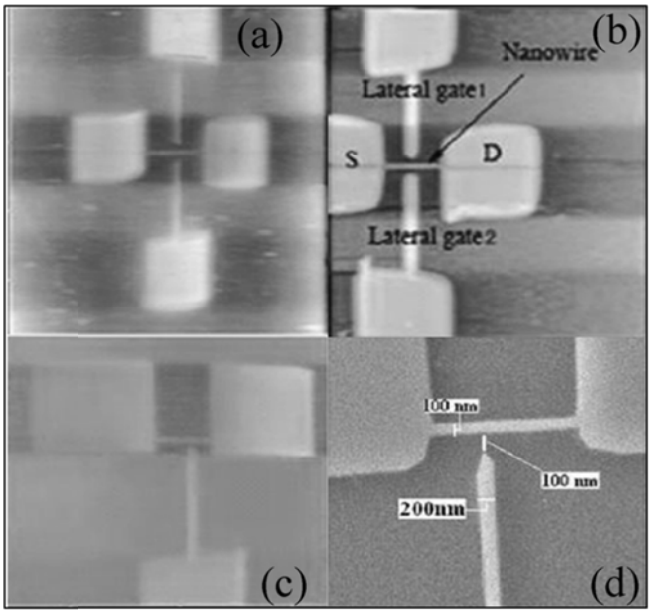

Fig. 11: AFM and SEM images of DG a),b) and SG c),d) JLSNWTs.

For the characterization of the device Agilent HP4156C SPA device or semiconductor parametric analyzer were used to monitor current-voltage relationship in different configurations. This analyzer has four medium power source monitor units (SMU), each of which can supply upto 50 V with maximum current of 100 mA and the current resolution of 1 pA. If proper cares are taken, such as the cable are kept in a dark and vacuumed environment (the SPA equipped with the vacuum facility), it can measure down to 10 fA of current.

For the side(s) gated measurement, first the side gate (V_G) was swept from -3 V to +3 V while keeping the drain to source voltage (V_{DS}) constant and negative because the channel is p-type. I_D-V_G graphs are shown for SGJLSNWT for V_{DS}= -1, -0.05 in Fig. 12(a). The figure shows the pinch-off effect due to positive lateral gate applying on the channel. It shows that the device is in on state for zero gate voltage, and by increasing the positive gate voltage, the current will be dropped. This indicates the pinch-off effect due to positive lateral gate applying on the channel. The field effect also can be observed under the lateral positive gate voltage regarding to the p-type channel. When the device is in the on state and a positive gate voltage is applied to the lateral gate, the current value will be dropped and the channel starts to deplete at a sufficient positive gate voltage and the device reaches to the pinch off state.

In JLTs, the gate voltage controls the channel resistivity. Unlike the conventional MOSFETs where it is necessity of reverse bias for off state condition, but in JLT, the channel is depleted by the gate electrostatic potential, producing high resistivity in the channel. For p-type channel, increasing negative voltage applied on the gate will force the major carriers in the channel to accumulate, producing low resistivity [44].

The On/Off ratio and subthreshold swing (SS) for DGJLSNWT were 106 and 100 mV/decade respectively (not shown) and for SGJLSNWT were 10^5 and 167 mV/decade respectively (Fig. 12(b)). High SS for the SG structure can be explained by asymmetry of the gate regarding to the channel, which as expected for DG structure, the SS is decreased compare to SG structure. The pinch off effect occurred in +1.5 V and +2.5 V in DG and SG structure respectively. As it is shown in Fig. 12(a) for SG structure, the output characteristic shows that the drain current (ID) does not significantly increase with the negative increase of gate voltage, unlike the conventional p-type channel MOSFETs. Also, high and positive threshold voltage (+ 1.2 V for SG and +0.8V for DG), indicates that the transistor is in On state with zero gate voltage.

Low current is due to the low doping concentration profile (10^{15} cm^{-3}) for the channel, which is lower than reported current value of the high doping concentration profile ($5x10^{19}$ cm^{-3}) JLTs. The MOSFETs or JLTs with high doping concentration mostly suffered with high scattering effect or threshold voltage variation. Low channel doping can improve field-effect mobility and drive current. It also can be helpful to have low off current, decrease the scattering effect and threshold-voltage variations [45]. Electrical characteristics of the devices have the same trend compared to the reported cases fabricated by AFM nanolithography with nearly similar structure [18, 46-47]. However, in none of the reported cases, the devices were used as the pinch off device.

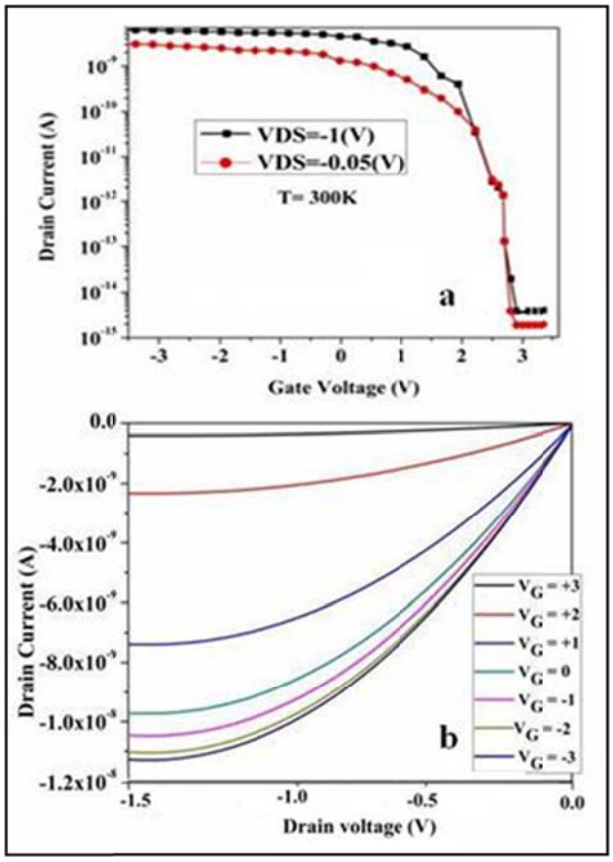

Fig. 12: Transfer (a) and output (b) characteristics graph for the SGJLSNWT at T= 300K.

4. Conclusion

Simple structures as the side gate Junctionless Si transistor fabricated on low-doped SOI by improved AFM nanolithography. Sample preparation and cleaning process were modified RCA method. The AFM-LAO parameters were optimized to achieve the devices. Two wet etching process implemented to extract the structure after LAO process. First, the KOH etching to remove the uncovered Silicon and then, the HF etching for Silicon oxide removal were used. The output and transfer characteristic of the device investigated showing the device is in on state for zero gate voltage. The pinch off effect observed for positive gate voltage

Acknowledgements

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References

[1] J. P. Han, *et al.*, Japanese Journal of Applied Physics **50** (2011)
[2] H. G. Virani, *et al.*, Japanese Journal of Applied Physics **50** (2011) 04DC04
[3] R. Chau, *et al.*, Electron Device Letters, IEEE **25** (2004) 408
[4] G. Lansbergen, *et al.*, Nature Physics **4** (2008) 656
[5] A. Veloso, *et al.*, Japanese Journal of Applied Physics **50** (2011)
[6] B. Yang, *et al.*, Electron Device Letters, IEEE **29** (2008) 791
[7] J. P. Colinge, *et al.*, Nature Nanotechnology **5** (2010) 225
[8] A. Afzalian, *et al.*, *MultiGate SOI MOSFETs: accumulation-mode vs. enhancement-mode*, (2008) 1
[9] S. Gundapaneni, *et al.*, Electron Device Letters, IEEE, **32** (2011) 261
[10] J. Colinge, *et al.*, *SOI gated resistor: CMOS without junctions* (2009) 1
[11] A. Kranti, *et al.*, *Junctionless nanowire transistor (JNT): Properties and design guidelines* (2010) 357
[12] D. D. Zhao, *et al.*, Applied Physics Express **4** (2011) 031302
[13] E. Gnani, *et al.*, IEEE Transactions on Electron Devices 58 (2011) 2903
[14] C. W. Lee, *et al.*, Applied Physics Letters **94** (2009) 053511
[15] C. W. Lee, *et al.*, Electron Devices, IEEE Transactions on **57** (2010) 620
[16] J. P. Raskin, *et al.*, Applied Physics Letters **97** (2010) 042114
[17] S. J. Choi, *et al.*, Electron Device Letters, IEEE (2011) 1
[18] P. Campbell, *et al.*, Applied Physics Letters **66** (1995) 1388
[19] E. Snow, *et al.*, Applied Physics Letters **63** (1993) 749
[20] I. Ionica, *et al.*, Solid-State Electronics **49** (2005) 1497
[21] G. Pennelli, Microelectronic engineering **86** (2009) 2139
[22] J. Martinez, *et al.*, Nano Letters **8** (2008) 3636

[23] S. D. Hutagalung and K. C. Lew, *Electrical characteristics of silicon nanowire transistor fabricated by AFM lithography* (2010) 358
[24] A. Dehzangi, *et al.*, *Field effect in silicon nanostructure fabricated by Atomic Force Microscopy nano lithography* (2011) 104
[25] A. Nazarov, *et al.*, *Semiconductor-On-Insulator Materials for Nanoelectronics Applications*: Springer Verlag (2011)
[26] S. J. Fonash, *et al.*, Applied Physics Letters **91** (2007) 193508
[27] T. H. Fang, Microelectronics journal **35** (2004) 701
[28] K. Morimoto, *et al.*, Applied surface science **158** (2000) 205
[29] H. Kuramochi, *et al.*, Surface science **542** (2003) 56
[30] D. Ricci and P. C. Braga, Methods In Molecular Biology-Clifton Then Totowa **242** (2004) 25
[31] S. Youn and C. Kang, Wear **261** (2006) 328
[32] G. Pennelli, *et al.*, Microelectronic engineering **83** (2006) 1710
[33] A. M. Abdullah, *et al.*, *Etching Effect On The Formation Of Silicon Nanowire Transistor Patterned By AFM Lithography* (2010)
[34] H. G. G. Philipsen and J. J. Kelly, Electrochimica acta **54** (2009) 3526
[35] M. Yun, Journal-Korean Physical Society **37** (2000) 605
[36] I. Zubel and M. Kramkowska, Sensors and Actuators A: Physical **93** (2001) 38
[37] C. R. Yang, *et al.*, Sensors and Actuators A: Physical **119** (2005) 271
[38] H. Camon and Z. Moktadir, Microelectronics journal **28** (1997) 509
[39] W. Haiss, *et al.*, Journal of Electroanalytical Chemistry **597** (2006) 1
[40] K. Biswas, *et al.*, Microelectronics journal 37 (2006) 765
[41] A. Dehzangi, *et al.*, American Journal of Applied Science **8** (2011) 872
[42] S. D. Hutagalung, *et al.*, Journal of Scanning Probe Microscopy, 2 **1** (2007) 28
[43] M. Yun, *et al.*, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures **16** (1998) 2844
[44] E. Hsieh and S. S. Chung, *A new type of inverter with Juctionless (J-Less) transistors* (2010) 1
[45] Y. K. Choi, *et al.*, Japanese Journal Of Applied Physics Part 1 Regular Papers Short Notes And Review Papers **42** (2003) 2073
[46] V. Bouchiat, *et al.*, Microelectronic engineering **61** (2002) 517
[47] I. Ionica, *et al.*, Solid-State Electronics **49** (2005) 1497