

CHAPTER 4

RESULTS & DISCUSSION

3.2 Introduction

This project aims to prove that Modified Baugh-Wooley Two's Complement Signed Multiplier is one of the high speed multipliers. The schematic of the multiplier is designed and analyzed using Block Design Editor that is provided in Altera's Quartus II Software. In order to check the speed performance, the schematic is analyze using Timing Analyzer Tool. The multiplier consists of AND gate, NAND gate, Half Adder, Carry Save Adder and D flip-flop. This chapter will discuss about the design that has been made for 8-bits x 8-bits Modified Baugh-Wooley Two's Complement Signed Multiplier and the results achieved.

4.2 Half Adder

Half Adder is an arithmetic circuit that generates the sum of two binary digits. It has two inputs and outputs. The Half Adder is implemented with one exclusive OR gate and one AND gate as shown in Figure 4.1.

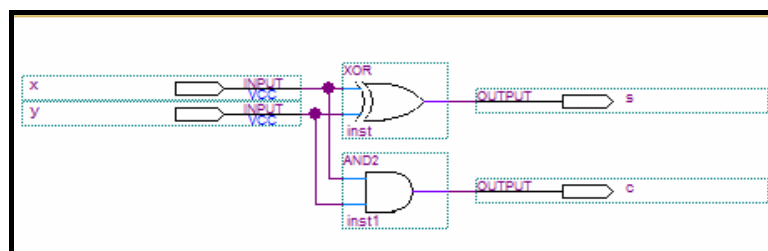


Figure 4.1 : Logic Diagram of Half Adder

The result for this Half Adder is shown in Figure 4.2. The result of this Half Adder is exactly the same as in Table 3.3 that has been explained in Section 3.3.3.

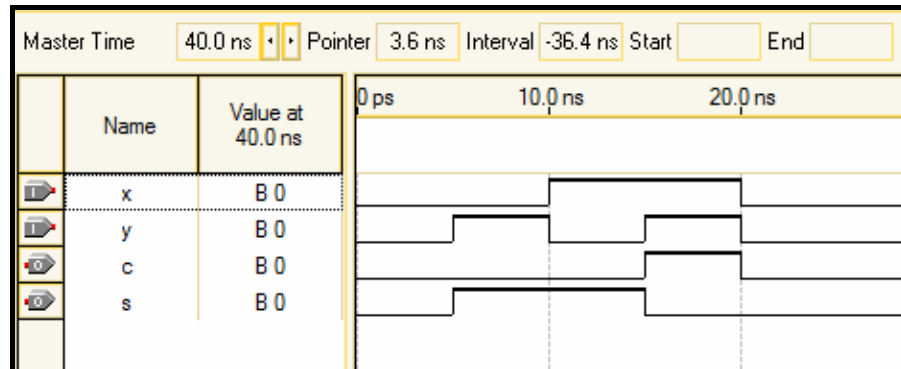


Figure 4.2 : Simulation Waveform of Half Adder

4.3 Carry Save Adder

Carry Save Adder accepts three n-bit operands and generates two n-bit results, an n bit partial sum, and n-bit carry. As shown in Figure 4.3, the logic diagram for Carry Save Adder consists of two Half Adder blocks and an OR gate. Half Adder block is created from Half Adder.bdf file using Create Symbol Tool.

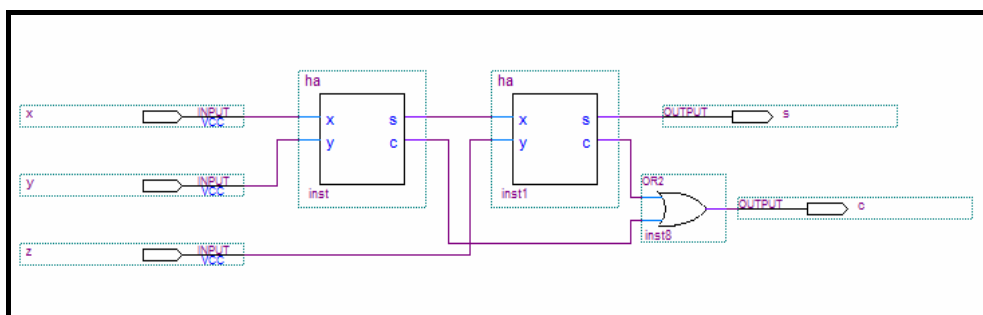


Figure 4.3 : Logic Diagram of Carry Save Adder

The result of Carry Save Adder is shown in Figure 4.4. It shows that the result is exactly the same with Table 3.4 in Section 3.3.4.

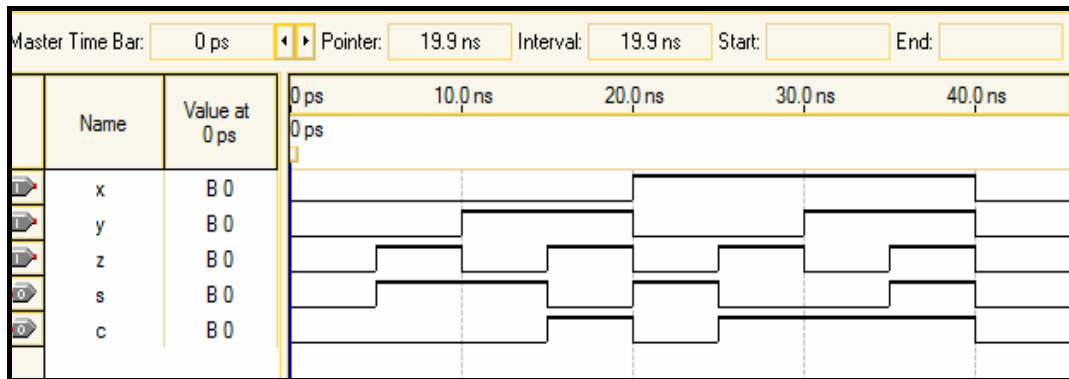


Figure 4.4 : Simulation Waveform of Carry Save Adder

4.4 Modified Baugh-Wooley Two's Complement Signed Multiplier

The design of 8-bits x 8-bits Modified Baugh-Wooley Two's Complement Signed Multiplier is done by referring to the tabular form of bit-level Modified Baugh-Wooley multiplication. The implementation of this circuit needed AND gates, NOT gates, Half Adders and Carry Save Adders to form the partial product bits as shown in Figure 4.5 in next page.

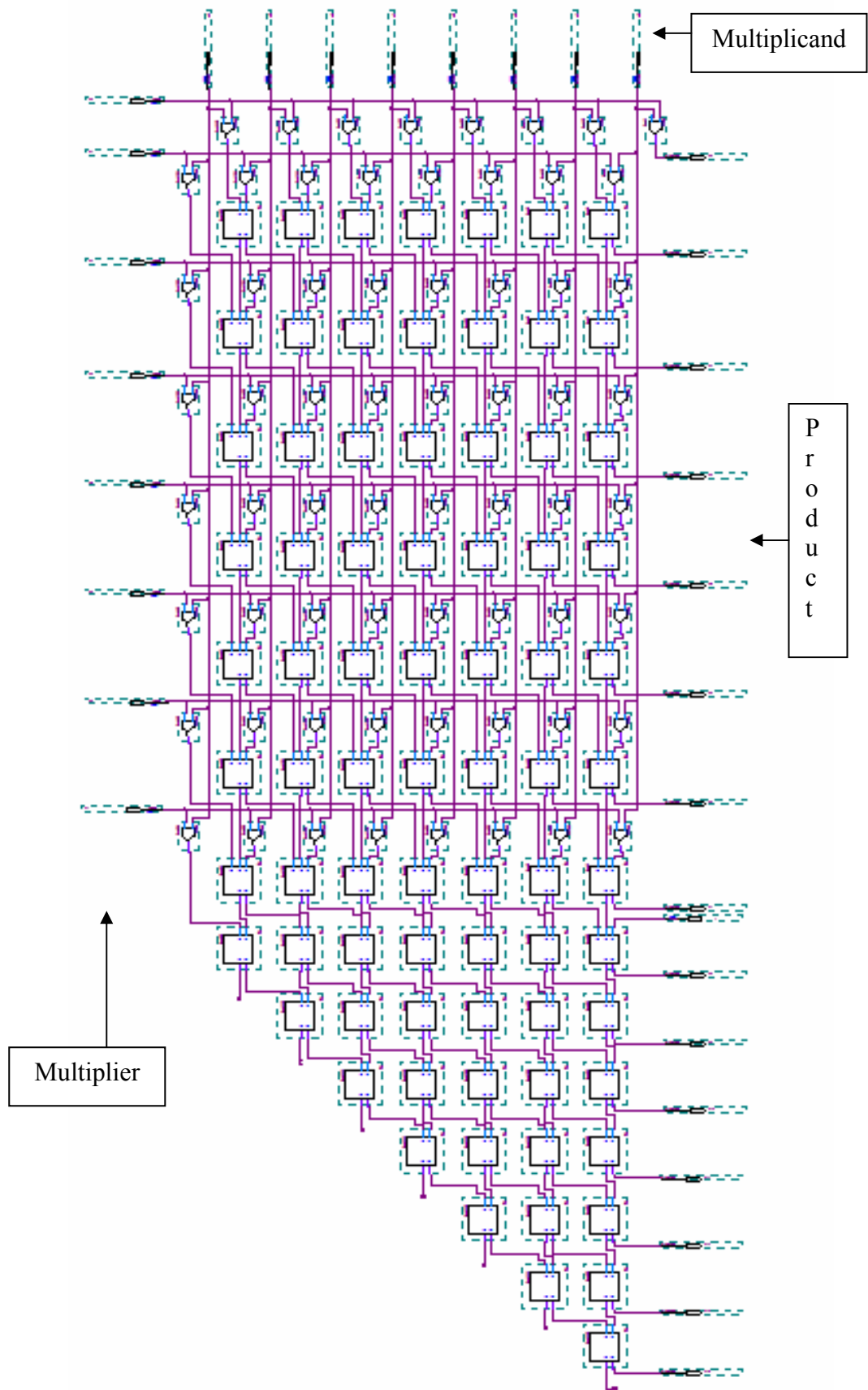


Figure 4.5: 8-bits x 8-bits Modified Baugh-Wooley Two's Complement Signed Multiplier

Modified Baugh-Wooley Two's Complement Signed Multiplier is a two's complement parallel array multiplier. Since it uses two's complement representation, the multiplicand and the multiplier are put in true binary form to perform multiplication. If the two numbers to be multiplied are positive, both are already in true binary form and are multiplied as they are. The resulting product is positive and is given a sign bit of 0.

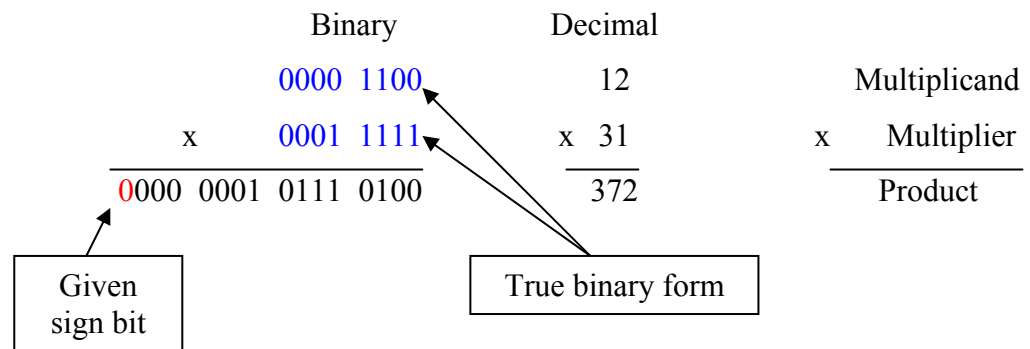


Figure 4.6 shows the correct answer of multiplication for the two positive numbers. The result is represented in binary and decimal numbering system verification. Since the range of positive numbers in an 8-bit system is 0000 0000 to 0111 1111 (0 to 127), only selected number are displayed.

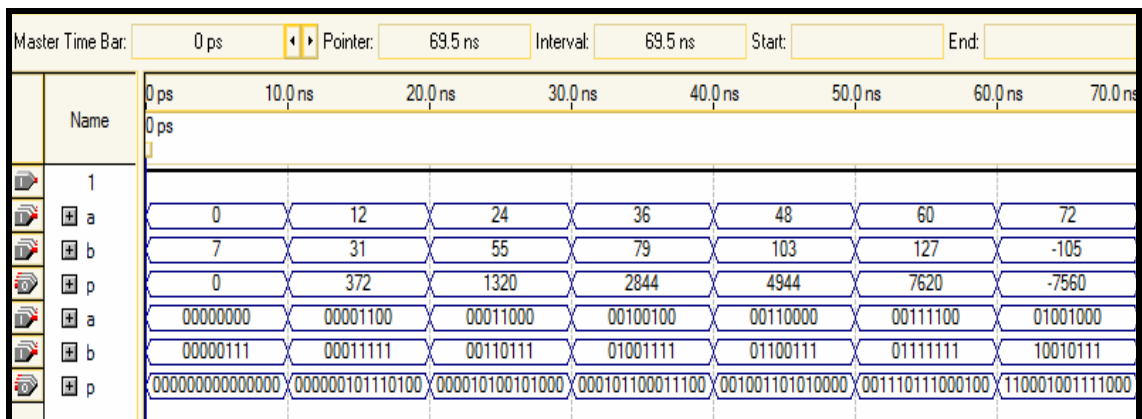


Figure 4.6 : Simulation Waveform of Both Positive Numbers Multiplication

When two numbers are negative, it will be in two's complement form. The two's complement of each is taken to convert it to a positive number, and then the two numbers are multiplied. The product is kept as a positive number and is given a sign bit of 0.

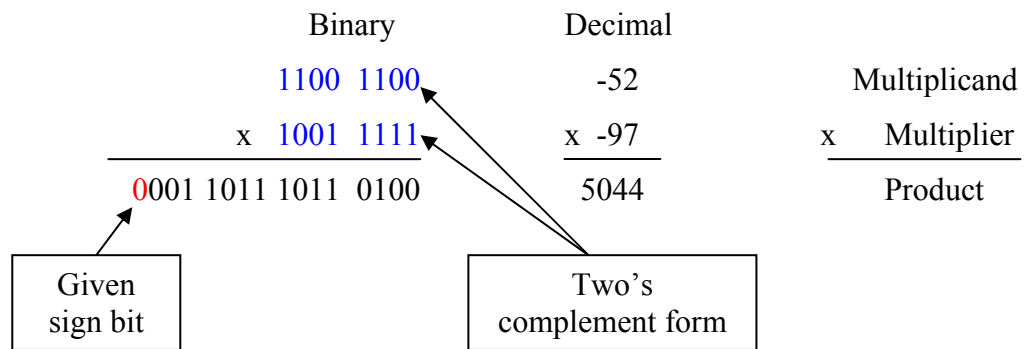


Figure 4.7 shows the correct answer of multiplication for the two negative numbers. The result is represented in binary and decimal numbering system verification. The range of negative numbers is 1111 1111 to 1000 0000 (-1 to -128), only selected number are displayed.

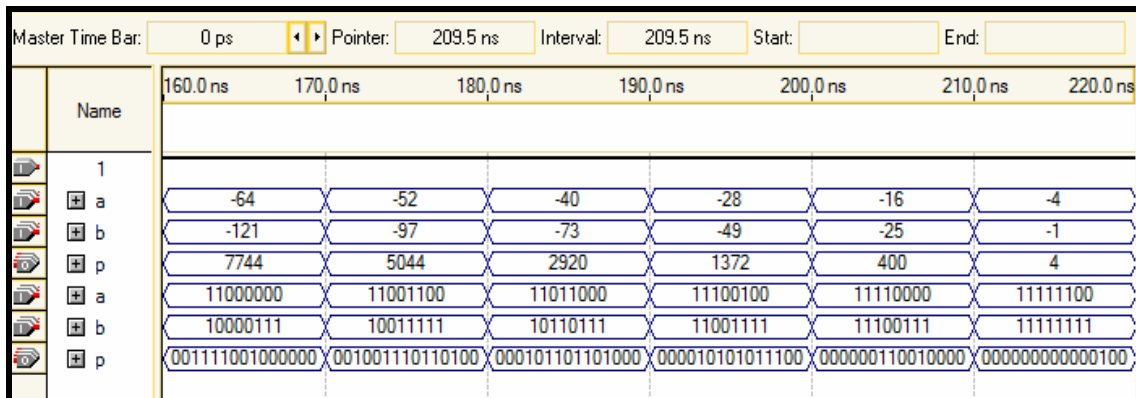


Figure 4.7 : Simulation Waveform of Both Negative Numbers Multiplication

When one of the numbers is positive and the other is negative, the negative number is first converted to a positive magnitude by taking its two's complement. The product will be in true magnitude form. However, the product must be negative, since the original numbers are of opposite sign. Thus, the product is then changed to two's complement form and is given a sign bit of 1.

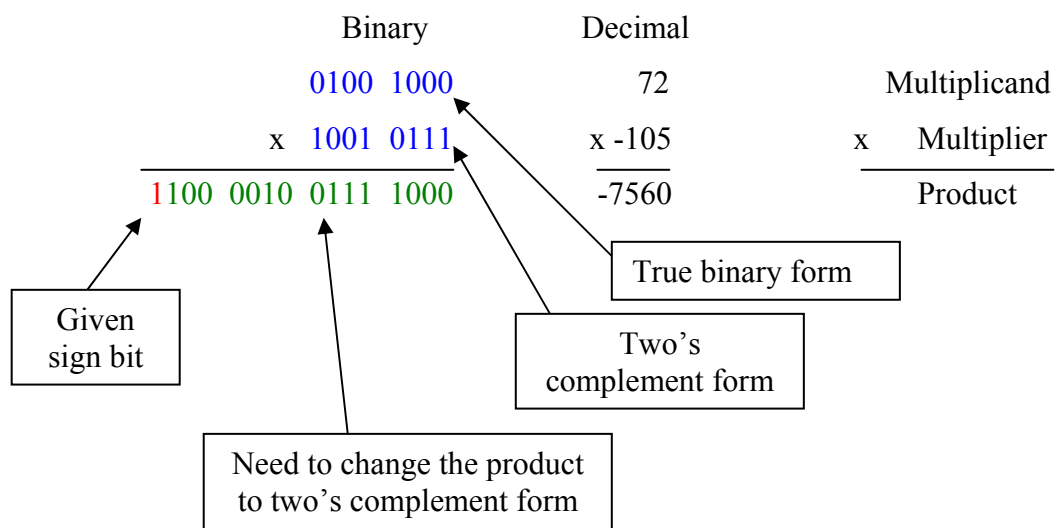


Figure 4.8 shows the result for positive and negative numbers multiplication. The results of multiplications for both numbers are correct. Only selected numbers are displayed, due to the wide range of numbers that can be multiplied together.

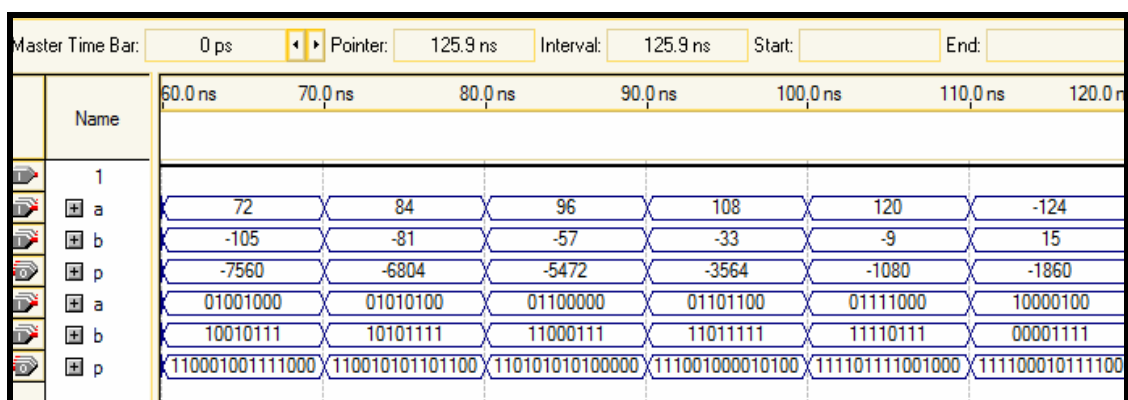


Figure 4.8 : Simulation Waveform of Positive and Negative Numbers Multiplication

The main objective for this project is to prove that Modified Baugh-Wooley Two's Complement Signed Multiplier is a high speed multiplier. In order to check the speed performance, D Flip-flop must be connected first to each inputs and outputs to provide a clock signal as shown in Figure 4.9.

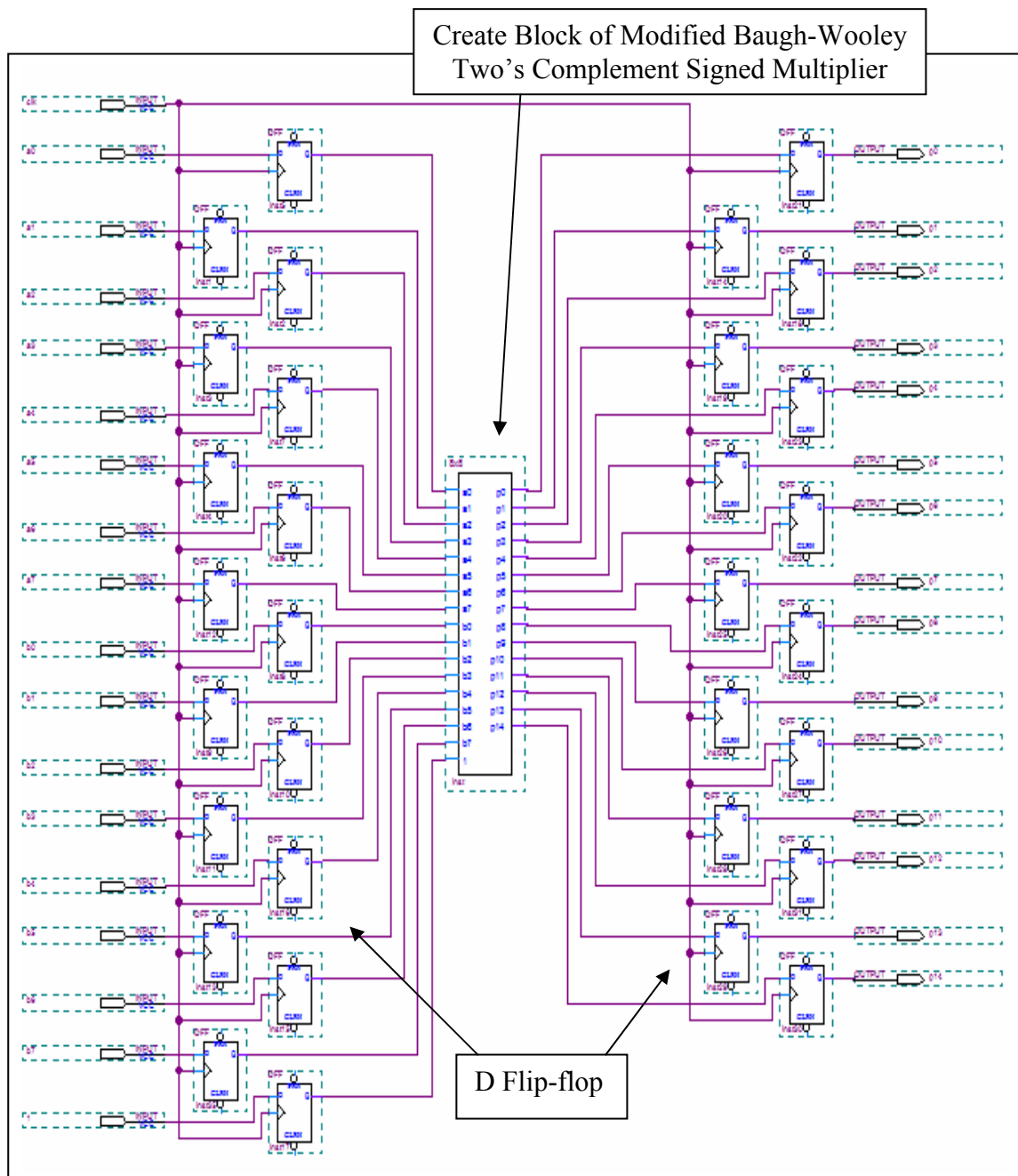


Figure 4.9 : 8-bit x 8-bit Modified Baugh-Wooley Multiplier with D Flip-flop at inputs and outputs

The speed value for this multiplier is 20.33MHz as shown in Figure 4.10.

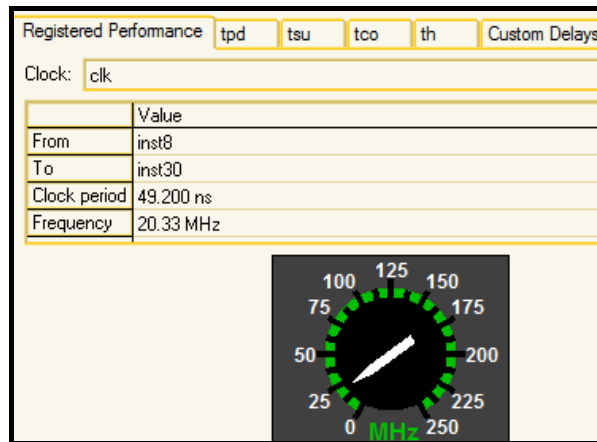


Figure 4.10 : Speed Performance for Modified Baugh-Wooley Multiplier

The output from this multiplier is shown in Figure 4.11. The multiplication results for this multiplier are correct. It should be noted that, there is delay for first output that been introduced by D Flip-flop registers.

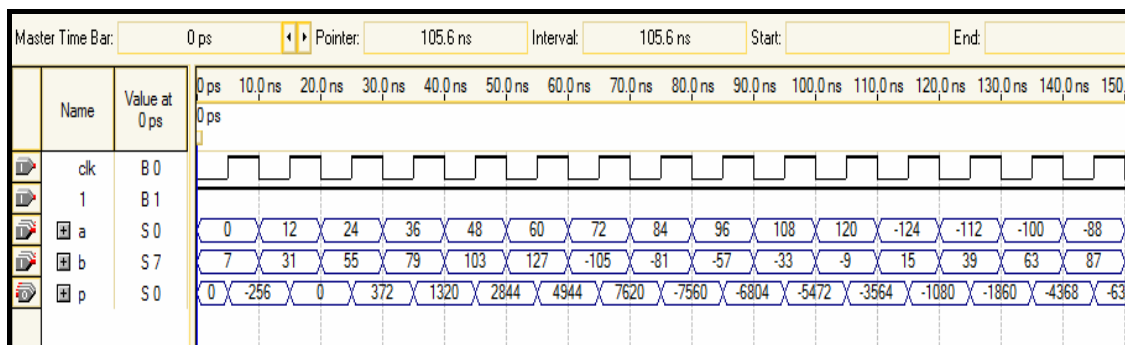


Figure 4.11 : Simulation Waveform for Modified Baugh-Wooley Multiplier

From results that have been discussed, it shows that the schematic design of Modified Baugh-Wooley Two's Complement Signed Multiplier is functioning correctly. D Flip-flop must be connected first to each inputs and outputs to provide a clock signal in order to check the speed performance. Pipelining approach applied to Modified Baugh-Wooley Two's Complement Signed Multiplier has not been able to produce the expected result yet, might be due to improper of placing pipeline

register (D Flip-flop) in the schematic. This is because, some of the D Flip-flops must even be placed in data paths in which no work has been done.