

FABRICATION OF SILICON NANOWIRES USING
SCANNING ELECTRON MICROSCOPE BASED
ELECTRON BEAM LITHOGRAPHY METHOD

MOHAMMAD NUZAIHAN BIN MD NOR

UNIVERSITI MALAYSIA PERLIS

MALAYSIA

2007

© This item is protected by original copyright



**Fabrication of Silicon Nanowires Using Scanning
Electron Microscope Based Electron Beam
Lithography Method**

By

**MOHAMMAD NUZAIHAN BIN MD NOR
0430110011**

A thesis submitted

In fulfillment of the requirements for the degree of
Master of Science (Microelectronic Engineering)

**School of Microelectronic Engineering
UNIVERSITI MALAYSIA PERLIS
MALAYSIA**

2007

**GRADUATE SCHOOL
UNIVERSITI MALAYSIA PERLIS**

PERMISSION TO USE

In presenting this thesis in fulfillment of a post graduate degree from Universiti Malaysia Perlis, I agree that permission for copying of this thesis in any manner, in whole or in part, for scholarly purposes may be granted by my supervisor or, in their absence, by Dean of the Graduate School. It is understood that any copying or publication or use of this thesis or parts thereof for financial gain shall not be allowed without my written permission. It is also understood that due recognition shall be given to me and to Universiti Malaysia Perlis for any scholarly use which may be made of any material from my thesis.

Requests for permission to copy or make other use of material in whole or in part of this thesis to be addressed to:

**Dean of Graduate School
Universiti Malaysia Perlis
Jalan Bukit Lagi
01000 Kangar
Perlis Indera Kayangan
Malaysia**

APPROVAL AND DECLARATION SHEET

This thesis titled Fabrication of Silicon Nanowires Using Scanning Electron Microscope Based Electron Beam Lithography Method was prepared and submitted by Mohammad Nuzaihan Bin Md Nor (Matrix Number: 0430110011) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the award of degree of Master of Science (Microelectronic Engineering) in Universiti Malaysia Perlis (UniMAP).

Check and Approved by

.....
(Associate Professor Dr Uda Bin Hashim)

School of Microelectronic Engineering
Universiti Malaysia Perlis

(Date :.....)

School of Microelectronic Engineering
Universiti Malaysia Perlis

DEDICATION

Al- Fatihah to my mum, Allahyarhammah Jamiah Binti Hashim, may Allah S.W.T bless you. Special dedication to my dad, Md Nor Bin Awang and my siblings, thanks for all the support and understanding. May Allah S.W.T bless all of us, Amin.

Thank you!

© This item is protected by original copyright

ACKNOWLEDGEMENT

First of all my deepest thanks and humble supplication are due to Almighty Allah (SWT), the Omnipotent, the Merciful, the Compassionate, always help, support and strengthened me during my lifetime. I beg Him to continue His blessings on me forever. Alhamdulillah, finally I have fulfilled my thesis in this year, 2007. The journey towards the completion of this thesis was full of unexpected challenges and it is almost impossible to complete this thesis single-handedly without the help and support of others. I would like to give my heartfelt thanks to everyone who has provided me with such support.

I would like to acknowledge and express the greatest gratitude to my supervisor Assoc. Prof. Dr. Uda Hashim, not only for giving me the opportunity to work in his group but also for his encouragement, supervision and guiding me throughout this whole research work. His invaluable knowledge and suggestion had develop and grown up my experience and my skills in this nanotechnology. It has been great experience in the IRPA Single Electron Transistor (SET) Group. I wish to express my gratitude for the benefits that I have gained from conversations with the other member in this group.

Many colleagues have worked closely with me on this research work. First, I would like to thank Miss S Niza for helping me to start at the lab. I am lucky to have Miss Nurhamidah, Miss Amiza and Miss Nik Hazura in pursuing the functional SEM, EBL system, AFM and Modu Lab Equipments. I do appreciate the constant help from lab technicians who always understand and their great help during the process of completing this research work. I also want to thank Mr Mohd Hafiz, Mr Mohd Sukri and Miss Suraya for helping me a lot to improve the written English.

A special thank to all staff members of the School of Microelectronic Engineering, Universiti Malaysia Perlis such as Mrs. Hasnizah, Miss Sanna, Mrs. Aznira, Mr. Khairuddin, Miss Nurjuliana and Mr. Razaidi for their technical advice and contributions either directly or indirectly. I'm also very grateful to Universiti Malaysia Perlis and the IRPA Single - Electron Transistor (SET) for their financial support throughout my postgraduate study. These special thanks also go to Miss Sharifah Husna and Miss Norzaililah for their support in managing the postgraduate and scholarship program.

Last but no least, I would like to thank my father, sisters and brothers for their love, confidence and support throughout my study. Not to forgot my housemate Mr. Amir who has always given encouragement and advise during my thesis preparation. To my friends whose names are not included here, may ALLAH bless you all.

Thanks to Almighty ALLAH.

MOHAMMAD NUZAIHAN BIN MD NOR
UNIVERSITI MALAYSIA PERLIS
m.nuzaihan@unimap.edu.my

**FABRIKASI “*SILICON NANOWIRES*” MENGGUNAKAN KAEDAH
MIKROSKOP IMBASAN ELEKTRON BERDASARKAN LITHOGRAFI ALUR
ELEKTRON**

ABSTRAK

Nanowires merupakan kelas baru dalam bahan yang telah menarik perhatian dan menjadi tumpuan penyelidikan sejak akhir-akhir ini kerana penggunaannya berpotensi di dalam nanoteknologi seperti kejuruteraan '*nanoelectronic*', '*nanomechanical*', '*biomedical*'. Fabrikasi '*Nanowires*' merupakan sesuatu yang sangat mencabar pada hari ini. Kaedah konvensional lithografi tidak mampu lagi untuk menghasilkan '*Nanowires*' dan walaupun dengan menggunakan lithografi nano yang maju adalah bukan mudah untuk mencapai ukuran yang kurang daripada 100 nm. Tujuan kerja penyelidikan ini adalah untuk membentuk dan menghasilkan '*Nanowires*' terkecil menggunakan kaedah fabrikasi nano '*Top-Down*' yang melibatkan Mikroskop Imbasan Elektron berdasarkan Lithografi Alur Elektron. Kaedah fabrikasi nano '*Top-Down*' berdasarkan Lithografi Alur Elektron dimulakan dengan menghasilkan Rekaan Corak '*Nanowires*' (NPD). Rekaan Corak '*Nanowires*' direka menggunakan perisian yang dipanggil '*RAITH ELPHY Quantum GDSII Editor*'. Pakej perisian ini menawarkan semua ciri-ciri yang diperlukan untuk menghasilkan struktur mikro dan nano bermula dengan reka struktur, proses selanjutnya dan kerja-kerja modifikasi. Rekaan Corak '*Nanowires*' ini direka dalam pelbagai skala daripada 100 nm dikesilkan sehingga 20 nm. Seterusnya, pembangunan proses aliran fabrikasi nano yang mengandungi parameter-parameter yang terperinci dan resepi-resepi telah dibangunkan untuk membentuk '*Nanowires*'. Dua (2) jenis topeng kerintangan dan tiga (3) jenis '*Nanowires*' yang terlibat dalam pembangunan proses aliran ini. Topeng kerintangan terdiri daripada Topeng Kerintangan PMMA dan Topeng Kerintangan Siri ma- N2400. Ianya digunakan sebagai bahan topeng atau topeng punaran semasa proses memunarkan lapisan oxida. Fabrikasi '*Nanowires*' merupakan fokus utama dalam kerja penyelidikan ini yang terdiri daripada '*SiO₂*', '*Si*', '*a-Si Nanowires*'. '*SiO₂ Nanowires*' berfungsi sebagai penebat dan topeng keras untuk punaran silica dalam usaha membentuk '*Si Nanowires*'. '*Si Nanowires*' dan '*a-Si Nanowires*' adalah sangat meluas digunakan sebagai '*Nanowires*' semikonduktor dan mempunyai nilai potensi dalam peranti '*nanoelectronic*'. Dalam usaha menghasilkan '*Nanowires*' terkecil ini, dimensi, profil pembentukan, profil punaran dan pengecilan saiz melalui pengoksidaan secara pemanasan telah diselidik. Akhir sekali, penggabungan kaedah fabrikasi nano '*Top-Down*' dengan pengecilan saiz telah menghasilkan kejayaan pengecilan '*Si Nanowires*' daripada 100 nm hinggalah menghampiri 20 nm.

FABRICATION OF SILICON NANOWIRES USING SCANNING ELECTRON MICROSCOPE BASED ELECTRON BEAM LITHOGRAPHY METHOD

ABSTRACT

Nanowires is a new class of materials that have attracted attention and great research interest in the last few years because of their potential applications in nanotechnology such as nanoelectronic, nanomechanical and biomedical engineering. Fabrication of Nanowires is one of the great challenges today. Conventional lithography methods are not capable to produce Nanowires and even with advance nanolithography sizes below 100 nm may not easily be achieved. The goal of this research work is to form and produce very small nanowires using a Top-Down Nanofabrication Method which involved Scanning Electron Microscope (SEM) based Electron Beam Lithography (EBL) method. Initially, the Top-Down Nanofabrication Method based on EBL was the design of the Nanowires Pattern Design (NPD). The NPD has been done by software called RAITH ELPHY Quantum GDSII Editor. The software package provides all the features needed to produce micro and nano scale structures starting from a structure design, post processing and design modification. The NPD is designed in various nanowires scale size from 100 nm down to 20 nm. Next, the nanofabrication process flow development which consists of the detailed parameters and recipes are developed for nanowires formation. Two (2) types of resist masks and three (3) types of nanowires are involved in the process flow development. The Resist Masks consist of PMMA Resist Mask and ma-N 2400 Series Resist Mask. It is used as a mask material or etches mask during Silicon Dioxide etching process. Fabrication of Nanowires is the main focus in this research work which consists of SiO₂, Si, a-Si Nanowires. SiO₂ Nanowires is used as insulation and hard mask for silicon etching in order to form Si Nanowires. Si Nanowires and a-Si Nanowires are widely used as semiconducting nanowires and has great potential in nanoelectronic devices. In order to produce very small nanowires, the dimensions, developments, etch profiles of nanowires and size-reduction by thermal oxidation was investigated. Finally, the combination on Top-Down Nanofabrication Method and size-reduction has resulted in successful reduction of Si Nanowires reduced from 100 nm to approximately 20 nm.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGES
	PERMISSION TO USE	i
	APPROVAL AND DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENTS	iv
	ABSTRAK	vi
	ABSTRACT	viii
	TABLE OF CONTENTS	ix
	LIST OF TABLES	xiii
	LIST OF FIGURES	xiv
	GLOSSARY OF ABBREAVATION	xix
	LIST OF APPENDIXES	xxi
	LIST OF PUBLICATIONS	xxii
	LIST OF AWARDS	xxv
1.0	INTRODUCTION	
1.1	Overview of Nanotechnology	1
1.2	Problem Statement	4
1.3	Research Objective	6
1.4	Research Scopes	6
1.5	Organization of this research work	7

2.0

LITERATURE REVIEW

2.1	Introduction	8
2.2	Nanowires	10
2.3	Materials of Nanowires	11
2.3.1	Insulator	11
2.3.2	Semiconductor	12
2.4	Properties of Nanowires	14
2.5	Existing Fabrication of Nanowires	15
2.5.1	Vapor-Liquid-Solid Method	15
2.5.2	Template-Based Method	17
2.5.3	Vapor Phase Method	18
2.5.4	Solvothermal Method	19
2.5.5	Oxide Assisted Growth Method	20
2.5.6	E-Beam Lithography Method	21
2.6	Application of Nanowires	24

3.0

TOP-DOWN NANOFABRICATION METHOD

3.1	Introduction	27
3.2	Sample Preparation	29
3.2.1	Starting Material	29
3.2.2	Wafer Cleaning Process	30
3.2.3	Oxidation Process	32
3.2.4	Deposition Process	33
3.2.5	E-beam Resist Spin Coating	34
3.2.6	E-Beam Resist Thickness Measurement	38
3.2.7	PMMA Resist Thickness	39
3.2.8	ma-N 2400 Series Resist Thickness	40
3.3	Software Description and Pattern Design	41
3.3.1	ELPHY Quantum GDSII Editor	42
3.3.2	Pattern Design	44

3.4	Electron Beam Lithography (EBL) System	45
3.4.1	Direct Writing EBL Approach	46
3.4.2	Beam Current and Focusing	47
3.4.3	Coordinate Systems	49
3.4.4	EBL Exposure	49
3.5	Development Process	53
3.5.1	Developer	53
3.6	Inductively Coupled Plasma – Reactive Ion Etching (ICP-RIE)	54
3.7	High Power Microscope (HPM) Inspection	54
3.8	Scanning Electron Microscope (SEM) Imaging	55
3.9	Atomic Force Microscopy (AFM) Characterization	56
3.10	Chapter Summary	57

4.0

RESIST MASKS AND NANOWIRES FORMATION

4.1	Introduction	58
4.2	The Process Flow Development	58
4.3	Resist Masks Formation	59
4.3.1	Process Flow of the Resist Masks	59
4.3.2	Results and Discussion	64
4.4	Nanowires Formation	78
4.4.1	Process Flow of the SiO ₂ Nanowires	79
4.4.2	Results and Discussion	80
4.4.3	Process Flow of the Si Nanowires	84
4.4.4	Results and Discussion	85
4.4.5	Amorphous Silicon (a-Si) Nanowires Formation	90
4.4.6	Results and Discussion	92
4.5	Chapter Summary	93

5.0

CONCLUSION

5.1	Introduction	95
5.2	Conclusion	95
5.3	Recommendations	98

REFERENCES

101

APPENDICES

© This item is protected by original copyright

LIST OF TABLES

TABLES	TITLE	PAGES
Table 1.1	Past and Future Technology Nodes for Feature CD	4
Table 2.1	The properties of Si and SiO ₂	14
Table 2.2:	The successful works on EBL Method	21
Table 3.1:	The silicon wafer specifications	29
Table 3.2:	The suitable exposure parameters	51
Table 4.1:	The Resist Masks and Nanowires involved in the process flow development	59
Table 4.2:	The develop troubleshooting problems	74
Table 4.3:	The smallest CD of Nanowires	94
Table 5.1:	The achievements of this research work	97

LIST OF FIGURES

FIGURES	TITLE	PAGES
Figure 1.1	The growth of U.S. government funding for nanotechnology	1
Figure 1.2	One nanometer is approximately the length to 5 silicon atoms aligned in a line	2
Figure 1.3	Schematic representations of the top-down and bottom-up approach and their relationship to biological and structures	3
Figure 1.4	The development of the feature size of IC, the limit of MOS Transistor was predicted as 1995	5
Figure 2.1	An illustration of Moore's Law shows the number of the transistor decreases every year	8
Figure 2.2	The transistor physical gate length of MOSFETs predicted in International Technology Roadmap for Semiconductors	9
Figure 2.3	The unique geometry of nanowires	10
Figure 2.4	The atomic structures of Silicon Dioxide	11
Figure 2.5	The covalent bonding of pure Si	12
Figure 2.6	The atomic order of crystal structure	13
Figure 2.7	The amorphous atomic structure	13
Figure 2.8	The schematic diagram of VLS for nanowires growth	16
Figure 2.9	The GaN Nanowires by VLS method	16
Figure 2.10	The ZnO Nanowires by VLS method	16
Figure 2.11	The alumina templates on the silicon wafer	17
Figure 2.12	The production of nanowires by vapor phase method	18

Figure 2.13	The TEM image of the sample prepared in the solvothermal method	19
Figure 2.14	The schematic diagram of OAG	20
Figure 2.15	The SEM image of sub-100 nm single layer patterns produced on Si substrate by EBL method	24
Figure 2.16	The nanowires MOSFET	24
Figure 2.17	The connections between nano and micro structures	25
Figure 2.18	The schematic diagram (top) and SEM image of Si SET (bottom)	26
Figure 3.1	The Top-Down Nanofabrication Method	28
Figure 3.2	P-type silicon wafer	30
Figure 3.3	The Wet Cleaning Bench	30
Figure 3.4	The RCA and BOE solution	31
Figure 3.5	The Modu-Lab Oxidation Furnace Module	33
Figure 3.6	The Plasmalab 80 Plus PECVD	33
Figure 3.7	The PMMA (left) and ma-N2403 (right)	35
Figure 3.8	Schematic of the chemical reaction of a positive resist (top) and negative resist (bottom) used in EBL	36
Figure 3.9	Positive and negative resist transfer process	36
Figure 3.10	Steps for resist coating process	37
Figure 3.11	The WS-400B-GNPP/UTE Spinner	38
Figure 3.12	The Filmetrics F-20 Spectrometer	39
Figure 3.13	Overview of graphic user interface (GUI) RAITH ELPHY Quantum GDSII Editor	42
Figure 3.14	The Nanowires Pattern Design (NPD)	44
Figure 3.15	The Nanowires Pattern Design with dimensions	45
Figure 3.16	The EBL System	46
Figure 3.17	The comparison of scanning methodologies: raster scan and vector scan	47
Figure 3.18	The schematic of an electron-beam exposure system	47
Figure 3.19	The beam current measurement window	48
Figure 3.20	SEM images shows (a) The contamination dot at 10K X magnification (b) The contamination	48

	dot at 70K X magnification	
Figure 3.21	The coordinate system by on the sample	49
Figure 3.22	The exposure window	50
Figure 3.23	The exposure parameter calculation	50
Figure 3.24	Block diagram of optimized exposure parameters	52
Figure 3.25	The SAMCO ICP-RIE 10iP	54
Figure 3.26	The Olympus BX51M HPM	55
Figure 3.27	The JOEL JSM 6460LA SEM	56
Figure 3.28	The SPA 400 AFM	57
Figure 4.1	The process flow of Resist Masks	59
Figure 4.2	The p-type <100> silicon wafer after cleaning process	60
Figure 4.3	Growth of 200 nm SiO ₂ layer	60
Figure 4.4	The PMMA resist coating on the SiO ₂ layer	61
Figure 4.5	The ma- N 2403 resist coating on the SiO ₂ layer	61
Figure 4.6	Soft bake of PMMA resist coated sample	62
Figure 4.7	Soft bake of ma- N2400 resist coated sample	62
Figure 4.8	The coated sample is exposed using EBL exposure	63
Figure 4.9	The final remaining resist for both Resist Mask	64
Figure 4.10	HPM images of the PMMA Resist Mask shows	65
	(a) the whole of the NPD with DF, (b) BF at 625 X,	
	(c) row 1 and (d) row 4 of the NPD	
	at 27000 X magnification, respectively	
Figure 4.11	HPM images of the ma-N2403 Resist Mask shows	66
	(a) the whole of the NPD with DF image,	
	(b) BF image at 625 X, (c) row 2 and	
	(d) row 3 of the NPD at 2700 X magnification, respectively	
Figure 4.12	HPM images of resist profile shows	67
	(a) incomplete development,	
	(b) under development, (c) over development and	
	(d) surface contaminants	
Figure 4.13	The SEM images of the PMMA Resist Mask	69
	shows the (a) (b) row 1, (c) (d) row 2, (e)	
	(f) row 3 at 5K and 15K, (g) row 4 of the NPD at 5K	
	and (h) 30K and (i) 50K X magnification, respectively	

Figure 4.14	The SEM images of the ma-N 2403 Resist Mask shows the (a) (b) row 1, (c) (d) row 2, (e) (f) row 3 at 5K and 15K, (g) row 4 of the NPD at 5K and (h) 30K magnification and (i) 50K X magnification, respectively	71
Figure 4.15	The SEM image of the Nano-Songket structure of the ma-N 2403 Resist Moks	72
Figure 4.16	The SEM images show the resist profile problems (a) Residue resist on the developed sample, (b) Incomplete development and (c) Underdevelopment and Overdevelopment	73
Figure 4.17	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of PMMA Resist Mask	75
Figure 4.18	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of ma-N2403 Resist Mask	76
Figure 4.19	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of ma- N 2403 Resist Mask after rework	77
Figure 4.20	The process flow of Nanowires	78
Figure 4.21	The etching process of SiO ₂	79
Figure 4.22	The SiO ₂ Nanowires	80
Figure 4.23	The SEM images of the 70 nm SiO ₂ Nanowires at (a) 5K X and (b) 15K X magnification	80
Figure 4.24	The SEM images of the 70 nm SiO ₂ Nanowires at (a) 30K X and (b) 50K X magnification	81
Figure 4.25	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of the SiO ₂ Nanowires	82
Figure 4.26	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of the SiO ₂ Nanowires after the etch improving by BOE	83
Figure 4.27	The etching process of Si	84
Figure 4.28	The Si Nanowires	85

Figure 4.29	The SEM images of the 70 nm Si Nanowires at (a) 5K X and (b) 15K X magnification	85
Figure 4.30	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of the Si Nanowires	86
Figure 4.31	The principle of size-reduction of Si Nanowires by thermal oxidation	87
Figure 4.32	The SEM images of the 50 nm Si Nanowires at (a) 5K X and (b) 30K X magnification	88
Figure 4.33	The SEM images of the 50 nm Si Nanowires at 100K X magnification	88
Figure 4.34	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of the size-reduction of Si Nanowires	89
Figure 4.35	The process flow of Nanowires based on a-Si material	90
Figure 4.36	The a-Si deposited sample	91
Figure 4.37	The ma-N 2403 developed sample	91
Figure 4.38	The a-Si Nanowires	91
Figure 4.39	The AFM images show (a) surface topography, (b) 3-D and (c) profile measurement of the a-Si Nanowires	92
Figure 4.40	The process flow development of the Resist Masks and Nanowires Formation	93
Figure 5.1	The schematic of EBL lift-off process (a) EBL in the PMMA, (b) exposed PMMA is developing, (c) metal deposition and (d) liftoff of metal on unexposed PMMA by removing PMMA underneath	99
Figure 5.2	The SEM images of 4 point Si Nanowires resistivity measurement structure	99
Figure 5.3	The schematic diagram of Si-SET	100

© This item is protected by original copyright

GLOSSARY OF ABBREVIATION

SET	=	Single Electron Transistor
EBL	=	Electron Beam Lithography
AFM	=	Atomic Force Microscopy
SPM	=	Scanning Probe Microscopy
SEM	=	Scanning Electron Microscopy
STM	=	Scanning Tunneling Microscopy
CD	=	Critical Dimension
IC	=	Integrated Circuit
PMMA	=	Polymethyl Methacrylate
SiO ₂	=	Silicon Dioxide
Si	=	Silicon
a-Si	=	Amorphous Silicon
VLS	=	Vapor-Liquid-Solid
OAG	=	Oxide Assisted Growth
GaN	=	Gallium Nitride
ZnO	=	Zinc Oxide
TEM	=	Transmission Electron Microscopy
FET	=	Field-Effect Transistor
CMOS	=	Complementary Metal Oxide Semiconductor
DNA	=	Deoxyribonucleic Acid
ICP-RIE	=	Inductively Coupled Plasma- Reactive Ion Etching
HPM	=	High Power Microscopy
SC	=	Standard Cleaning
BOE	=	Buffered Oxide Etch
WCM	=	Wet Cleaning Module
OFM	=	Oxidation Furnace Module
PECVD	=	Plasma Enhanced Chemical Vapor Deposition

PAC	=	photoactive Compound
MV	=	Molecular Weight
CAD	=	Computer Aided Design
GUI	=	Graphic User Interface
NPD	=	Nanowires Pattern Design
WA	=	Working Area
SPL	=	Single Pixel Line
MIBK	=	Methyl IsoBethyl Ketone
IPA	=	Isopropanol
DI	=	Deionized
DF	=	Darkfield
BF	=	Brightfield

© This item is protected by original copyright

LIST OF APPENDIXS

APPENDIX	TITLE	PAGES
A	Publications	110
B	Colloquiums	113
C	Awards	114
D	Posters	115
E	Newspaper Cutting	116
F	The Various Results Of The Resist Masks and Nanowires Formation (From 1 μ M Down To 30 nm Widths) During Optimization Exposure Parameters Steps	117

© This item is protected by original copyright

LIST OF PUBLICATIONS

1. **Mohammad Nuzaihan Md Nor, S Niza Mohammad Bajuri, Uda Hashim.** Pattern Design for Nanowire Formation Using Raith Elphy Quantum GDSII Editor. Proceeding of Annual Fundamental Science Seminar 2005, AFSS 2005. P. 110-116. ISBN 983-43098-0-5.
2. **Mohammad Nuzaihan Md Nor, S Niza Mohammad Bajuri, Nur Hamidah Abdul Halim, Uda Hashim.** Positive Pattern Scheme and Negative Pattern Scheme For Nanowire Formation Using Scanning Electron Microscope Based Electron Beam Lithography Technique, Journal Solid State Science & Technology Letters. Volume 12, RCSST 2005. P. 62. ISSN 0128-8393.
3. **Mohammad Nuzaihan Md Nor, U.Hashim, N.H.A. Halim, S.N. M. Bajuri.** Nanowire formation for Single Electron Transistor using SEM Based Electron Beam Lithography (EBL) Technique: Positive Tone Vs Negative Tone E-beam Resist. Technical Proceeding of NSTI Nanotech 2006, HCC Boston USA, NSTI 2006. P. 266-269. ISBN 0-9767985-8-1 Vol.3.
4. **Mohammad Nuzaihan Md Nor, U.Hashim, N.H.A. Halim.** Nanowires. Extended abstract of One-Day Seminar on Nanotechnology, Nanomig 2006, USM. P 67-70.
5. **Mohammad Nuzaihan Md Nor, Nur Hamidah Abdul Halim, Uda Hashim, Hasnizah Aris, Sanna Taking, Zaliman Sauli , KC Phang** "KUKUM Nano Fabrication Cleanroom: Efforts Towards Nanotechnology", Seminar Penyelidikan Kejuruteraan KUKUM 2006.

6. **Mohammad Nuzaihan Md Nor**, U.Hashim, Armiza Rasmi, N.H.A. Halim. Nanowire Formation Using SEM Based Electron Beam Lithography (EBL) Technique: Developments Profile of Negative Tone E-Beam Resist. The Second International Conference on Solid State Science and Technology 2006, ICSSST 2006 KUSTEM. P 282-284. ISSN 0128-839.
7. **Mohammad Nuzaihan Md Nor**, Uda Hashim, Nur Nazihah Halemi, Nur Hamidah Abdul Halim. Nanostructure Formation Using Scanning Electron Microscope (SEM) Based E-Beam Lithography (EBL) Technique: Wet Etch Profile. 15th Scientific Conference of Electron Microscopy Society of Malaysia, EMSM 2006 KUSTEM, P 43-44.
8. **Mohammad Nuzaihan Md Nor**, Uda Hashim, Nur Hamidah Abdul Halim. Top Down Approach: Fabrication of Si Nanowires Using Scanning Electron Microscope (SEM) Based E-Beam Lithography (EBL) Technique and Inductively Coupled Plasma-Reactive Ion Etching. Submitted and accepted for International Conference on Advancement of Materials and Nanotechnology 2007, ICAMN 2007 SIRIM & UITM.
9. S Niza Mohammad Bajuri, Nur Hamidah Abdul Halim, **Mohammad Nuzaihan Md Nor** and Uda Hashim. PMMA Characterization and Optimization for Nano Structure Formation. Proceeding of 1st national Conference on Electronic design (NCED) 2005. P 81-83. ISBN 983-42724-0-5
10. Armiza Rasmi, **Mohammad Nuzaihan Md Nor**, Uda Hashim. SOI Single Electron Transistors (SET) Set Design and Process Development. 1st National Conference on Electronic Design 2005, NCED2005, P 85-90. ISBN 983-42724-0-5.
11. S Niza Mohammad Bajuri, Nur Hamidah Abdul Halim, **Mohammad Nuzaihan Md Nor** and Uda Hashim. 495K & 950K PMMA Thickness Characterizations and Optimization. Proceeding of Annual Fundamental Science Seminar 2005, AFSS 2005. P.140-144. ISBN 983-43098-0-5.