SIMULATION ON EFFECTS OF DIFFERENT TYPES OF CHANNEL/DRAIN ENGINEERING STRUCTURE ON MOS DEVICE PERFORMANCE

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by

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APPROVAL AND DECLARATION SHEET

This project report titled Simulation on Effects of Different Types of Channel/Drain Engineering Structure on MOS Device Performance was prepared and submitted by Norazlina Binti Mohd Amin (Matrix Number: 031010367) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Microelectronic Engineering) in Universiti Malaysia Perlis (UniMAP).

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ABSTRAK

Projek tahun akhir ini merupakan satu analysis terhadap kesan penggunaan tiga jenis sturuktur kejuruteraan ‘channel/drain’ terhadap persembahan ‘MOS transistor’. Sebagai asas projek, proses resipi untuk 0.35µm daripada UC Berkeley telah digunakan sebagai rujukan. Projek ini dihasilkan dengan mengekalkan parameter yang lain dan hanya mengubah struktur ‘channel/drain’. Struktur MOS ini dihasilkan dengan menggunakan TSUPREM4. Struktur kejuruteraan ‘channel/drain’ yang dihasilkan adalah LDD, MDD dan Halo-Implantation. Ini diikuti dengan analisis mengenai sifat elektrik dengan menggunakan MEDICI. Parameter yang dikaji ialah voltan ambang, ‘slope’ yang linear, arus tertutup dan ‘slope’ sub-ambang. Daripada keputusan, didapati bahawa NMOS Transistor dengan struktur ‘Halo Implantation’ memberi persembahan yang terbaik. Voltan ambang untuk ‘Halo Implantation’ adalah 0.2613 V dengan arus tertutup sebanyak 9.1553 x 10^{-3} A/um. Voltan ambang yang rendah menunjukkan bahawa hanya voltan pada gate yang rendah diperlukan untuk membuatkan transistor berfungsi. Manakala, arus tertutup yang rendah memberikan nilai yang kecil terhadap kebocoran arus yang mengalir didalam transistor pada keadaan tertutup. Parameter lain yang dikaji adalah ‘slope’ yang linear dengan nilai 27.16 µA/µm-V dan 85.28 mV/dec untuk ‘slope’ sub-ambang.

ABSTRACT

This final year project is aimed to analyze the effects of three different types of channel/drain engineering structure on MOS transistor performance. As a project basis, a 0.35μm process recipe from UC Berkeley is used as reference. To proceed it, the other parameters need to be retained and only the channel/drain structure is altered. The MOS structure is first designed using TSUPREM4. The channel/drain engineering structures to be designed are Lightly Doped Drain (LDD), Moderately Doped Drain (MDD) and Halo-Implantation structure. This is followed by extraction of the electrical characteristic in MEDICI. Parameters that have been extracted are threshold voltage, linear slope, off-current and the subthreshold slope. From the results, it is found that NMOS transistor with Halo Implant structure gives the best performance. The threshold voltage (Vth) extracted for the halo implant structure is of 0.2613 V with off-current of 9.1553 x 10^{-3} A/um. The low Vth obtained shows that only a small amount of Vg is needed to turn-on the transistor. Meanwhile, low value of off-current means that only a small amount of leakage current flows when the transistor is in the 'off' condition. Other parameters extracted are linear slope with value of 27.16 μA/μm-V and subthreshold slope with value of 85.28 mV/dec.

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