THE OPTIMIZATION OF P-i-N POWER SWITCHING DIODE IN TERM OF REVERSE BREAKDOWN VOLTAGE AND ELECTROSTATIC DISCHARGE PERFORMANCE

By

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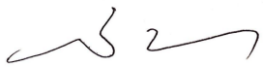

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LIST OF ABBREVIATIONS

I_R	Reverse Leakage Current
V_{BR}	Reverse Breakdown Voltage
V_F	Forward Voltage
ESD	Electrostatic Discharge
HBM	Human Body Mode
MM	Machine Mode
CDM	Charge Device Mode
TCAD	Technology Computer-aided Design
DOE	Design of Experiment
TRR	Reverse Recovery Lifetime
RSM	Response Surface Model
TEOS	Tetraethylorthosilicate
CVD	Chemical Vapor Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
LTO	Low Thermal Oxide
CMP	Chemical Mechanical Planarization
DUT	Device Under Test
IC	Integrated Circuit
SEM	Scanning Electron Microscope
GUI	Graphical User Interface
SWB	Sentaurus Work Bench

1D	One dimensions
2D	Two dimensions
3D	Three dimensions
HMDS	Hexamethyldisilazane
OVAT	One Variable at a Time
BOE	Buffered oxide wet etching

LIST OF SYMBOLS

I_R	Reverse Leakage Current
V_{BR}	Reverse Breakdown Voltage
V_F	Forward Voltage
I_F	Forward Current
P	Positive Dopant
N	Negative Dopant
ESD	Electrostatic Discharge
^oC	Celsius
Å	Ångström
Si	Silicon
O_2	Oxygen Gas
SiO_2	Silicon Oxide
H_2O	Water
H_2	Hydrogen Gas
AlSi	Silicon Aloy
N_D	Dopant Concentration
W_D	Depletion Width
µ	Micron
m	Mili

Pengoptimasi P-i-N Kuasa Pensuisan dalam Voltan Pincang Balikan dan Prestasi Nyahcas Elektrostatik

ABSTRAK

Kuasa pensuisan penerus (P-i-N penerus) merupakan salah satu penerus yang digunakan secara meluas dalam tinggi peranti semikonduktor kuasa sebagai perlindungan litar. Populariti ini terhasil daripada kecemerlangan untuk menyekat voltan terbalik dan prestasi nyahcas elektrostatik yang tinggi. Oleh itu, penerokaan penerus kuasa untuk membuat peranti yang lebih mantap dan berdaya saing dalam pasaran adalah tidak terbatas, yang bertujuan untuk penambahbaikan yang berterusan ke atas ciri-ciri elektrik. Dalam tesis ini, struktur rekabentuk kuasa pensuisan penerus P-i-N telah digunakan terdiri daripada bentuk anod persimpangan yang berbentuk lingkaran, substrat jenis N dengan lapisan epitaksi substrat silikon yang mewakili kawasan intrinsik. Terdapat dua jenis kuasa pensuisan penerus P-i-N dibincangkan dalam tesis ini, iaitu 250 V dan 300 V semasa pincang balikan. Kajian peningkatan prestasi voltan puncang balikan dan prestasi pembaikan nyahcas elektrostatik (ESD) yang berbeza telah dilancarkan masing masing. Perubahan tersebut telah dilakukan melalui proses simulasi serta rekabentuk disahkan melalui eksperimen proses wafer fabrikasi secara DOE. Untuk analisa ESD, peranti telah melalui pengujian tanpa musnah (non-destructive test) dan pengujian musnah (destructive test) untuk peranti yang telah difabrikasi. Pada mulanya, tesis membincangkan kajian-kajian penyelidikan untuk memperluaskan julat operasi kuasa pensuisan daripada 250 V kepada lebih daripada 300 V semasa pincang balikan berdasarkan perubahan ketebalan dan kerintangan lapisan epitaxi semasa pincangan arus hadapan dan balikan. Tujuan memperluaskan julat operasi kuasa pensuisan adalah digunakan dalam aplikasi kuasa pengagihan kuasa dan bukan dalam aplikasi telekomunikasi sahaja. Hasil kajian menunjukkan bahawa, perubahan tersebut dapat meningkatkan prestasi voltan kepada tahap ~500 V, iaitu melebihi 300 V semasa arus balikan. Peningkatan prestasi voltan pincang balikan adalah lebih daripada 65% dari 250 V. Selain daripada kajian meningkat ciri-ciri elektrik dalam tesis, kajian pembaikan ESD penerus P-i-N juga telah ditunjukkan dengan diod 300 V semasa arus balikan. Penambahbaikan ESD penerus P-i-N boleh dicapai dengan mengubah profil ciri-ciri persimpangan anod P+ dalam penerus P-i-N. Ciri-ciri profil juga boleh diubah dengan merendahkan kepekatan pendopan dan meningkatkan kedalaman persimpangan anod penerus P-i-N. Ianya didapati, untuk 300 K penerus P-i-N dapat bertahan lonjatan voltan lebih daripada 1 kV semasa ESD ragam badan manusia (HBM) (400% tinggi daripada asal) dan lebih daripada 400 V semasa ESD ragam mesin (MM) (100% tinggi daripada asal).

The Optimization of P-i-N Power Switching Diode in Term of Reverse Breakdown Voltage and Electrostatic Discharge Performance

ABSTRACT

The Power switching diode (P-i-N diode) is one of the widely used diode in high power semiconductor devices as circuit protection. This popularity comes from excellent reverse voltage blocking and better electrostatic discharge (ESD) performance. As a result, the exploration on the P-i-N power switching diode to make the device more robust and competitive in the market is boundless, which aims for continuous improvement on the electrical characteristics. In this thesis, the design structure of P-i-N power switching diode consist of a circular shape anode junction, an n-type bulk substrate and the epitaxial layer of silicon substrate that represent the intrinsic region is used. Two different type of reverse breakdown voltage range P-i-N power switching diode are discussed in this thesis which is 250 V and 300 V. Independently, the optimization of reverse breakdown voltage and ESD respectively is conducted using 250 V and 300 V respectively as both diode have different good and poor electrical performance. The improvement of both diodes are performed by process simulation and as well as the confirmation by the design of experiment (DOE) of physical wafers fabrication process. For the ESD analysis, the devices are then subjected to non-destructive and destructive test of the fabricated diodes. Initially, this thesis describes the research work to widen the operating range of the 250 V P-i-N power switching avalanche diodes that can be operated more than 300 V by exploring the effects of the thickness and resistivity of epitaxial layer during forward and reverse biasing. Purpose of widen the operating range is to be used in power distribution application instead of telecommunication application. The result shows that, the changes on a P-i-N type structure of the power switching avalanche diode can increase the reverse breakdown voltage performance to ~500 V, which is beyond 300 V during reverse bias. The improvement of reverse breakdown voltage is more than 65% from 250 V. In addition to the electrical characteristics operating range improvement in the thesis, the study of ESD improvement of 300 V reverse breakdown voltage P-i-N diode is demonstrated. A better ESD performance of the P-i-N diode is also achieved by changing the characteristic profile of the P+ anode junction of P-i-N diode. The characteristics profiles are altered by lightening the dopant concentration and increasing the depth of the P-i-N diode junction. It is found that, the 300V P-i-N power switching diode can sustain more than 1 kV during ESD Human Body Modal (HBM) surge test (400% higher from initial surge) and more than 400 V during ESD Machine Modal (MM) surge test (100% higher from initial surge).

CHAPTER 1

INTRODUCTION

1.1 Background

A semiconductor material has a small energy gap (i.e., 1.11 eV for silicon), that is a value between an insulator (>2 eV) and a conductor (0 eV) (M. Quirk & J. Serda , 2001). Thus, a semiconductor material can function as either conductor or insulator. For a formation of diode, a P-N junction is created with p-type and n-type semiconductor materials in intimate contact on an atomic scale. The formation of P-N junction is to diffuse acceptor impurities (p-type dopant) into an n-type silicon crystal or vice versa. The depletion region formed instantaneously across a P-N junction when junction is in thermal equilibrium or in a steady state. During the steady state, the properties of the system does not vary in time; thus it has been called dynamic equilibrium (J. E. Ayers , 2003) (S.M. Kang and Y. Leblebici, 2003).

A P-N junction diode is a device which only allows unidirectional of current flow when operating within a rated specified voltage level, and it is also known as a rectifier. In high power applications, an ideal power diode should be able of conducting high forward bias current (I_F) and supporting high reverse breakdown voltage (V_{BR}) (B. J. Baliga, 1996). For a vertical structure of P-N junction diode, a very thick wafer substrate bulk can be used to fulfill the requirement of a power diode. However, thicker substrate exhibits several drawbacks, which are greater weight and higher production cost. One of the methods for having a higher reverse breakdown voltage and higher forward current performance is by using the P-i-N diode's structure. The P-i-N diode was one of the very first semiconductor

devices developed for the power circuit application. (B. J. Baliga ,1996) This evolution came from a conventional P-N junction diode with the addition of an extra intrinsic layer deposited between p-type and n-type regions. Figure 1.1 illustrates the P-i-N diode structure in 2D structure.

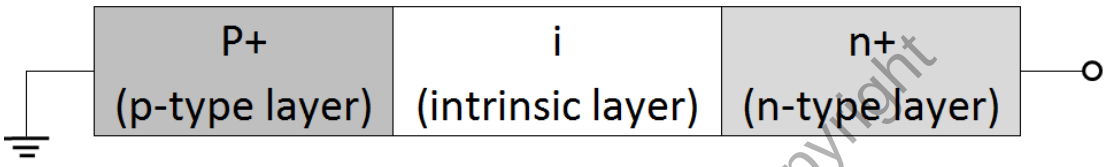

Figure 1.1: 2D structure layer P-i-N diode

The P-i-N diode has an intrinsic layer known as the i-region, which can be depleted at zero bias. Hence, an ideal P-i-N diode is also called a zero punch through diode (J. F. White , 2012) However, in practical cases, not all diodes are zero punch through. The i-region (sandwiched between the heavily doped p and n regions) is being substituted by a substantially higher resistivity p- or n-type layer (J. F. White , 2012).

In semiconductor power device theory, the reverse breakdown voltage of P-i-N is controlled by the intrinsic layer which represented by the n- epitaxial layer of the diode structure. Figure 1.2 illustrates the cross section design of the power switching diode.

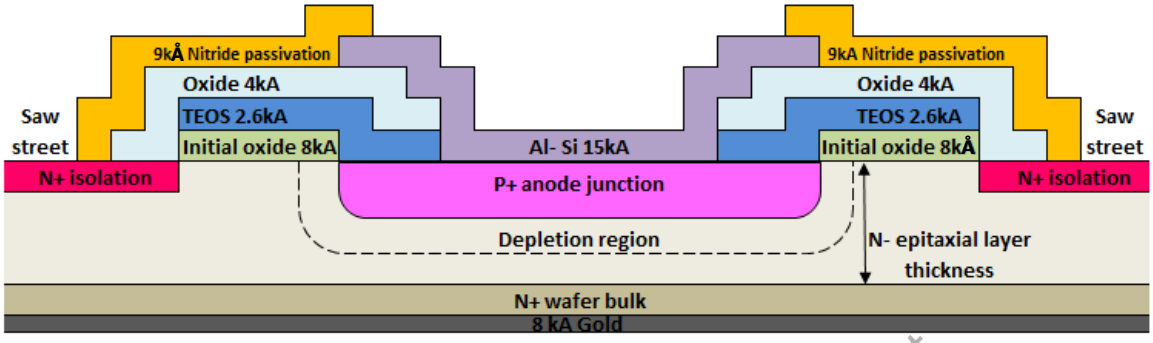

Figure 1.2: Cross-Section structure of Power Switching Diode

Compared to a normal P-N junction diode, the structure of P-i-N diode supports a higher reverse breakdown voltage with a much thinner n-type substrate. The heavily doped boron, p+ region is closest to the top of the diode. The doping level changes abruptly at the heavily doped boron p+ junction to a flat n- region; again abruptly to the flat n+ doping in the diode's another side (A. A.Sweet , 2007)

With the better reverse breakdown voltage performance (V_{BR}) of P-i-N diode compared with P-N junction diode, the usage of the P-i-N diode is still limited in power switching performance. P-i-N power switching diode is widely used in power industry. There are three main performance criteria that need to be achieved for the power switching diode which are huge reverse breakdown voltage, switching performance and the ESD performance. The ESD performance must be substantially high in power switching industry as ESD can create spectacular electric sparks under a huge surge which can cause damage to sensitive electronic devices. To improve reverse breakdown voltage and ESD performance, the design of the device must be studied and modified.

This research is greatly motivated by the comprehension of the function of power switching diode with vertical P-i-N diode structure. Two commercially available P-i-N

power switching diode devices, 250 V and 300 V are the interest in this work. The design of both 250 V and 300 V are similar except the die size. 250 V power switching diode has die size of 468 µm x 468 µm while 300 V power switching diode has a smaller die size of 400 µm x 400 µm.

1.2 Problem statements

In this work, two main performance criteria will be focused on which are the studies of increase reverse breakdown voltage and the ESD performance improvement. The device failure for these two types of diode encourages us to explore and to understand the problem. The failures are low breakdown voltage for 250 V power switching diode and poor ESD performance for 300 V power switching diode. The device optimization of both 250 V and 300 V P-i-N power switching diode are done independently, as both limitation are different.

Limitation of the operating range less than 300 V is found on the 250 V P-i-N power switching diode which unable to use in the motor control, robotics and power distribution application. In this thesis, we propose to increase the reverse breakdown voltage from 250 V to 450 V. The reason of increasing reverse breakdown voltage of 250 V power switching diode is to widen the application operating range from only used in the application of computer and telecommunications.

To increase the reverse breakdown voltage, this work will discuss the power switching diode reverse breakdown improvement through N- epitaxial layer optimization approach.

The alteration of the N- epitaxial layer thickness and resistivity profile not only increase the reverse breakdown voltage but may unpredictable significant increase other

electrical performance such as forward voltage, V_F and reverse leakage current, I_R. So, for this 250 V power switching diode research approach, the key analysis and investigation of exploring a good working window is assisted by Technology computer-aided design (TCAD) simulation and wafer fabrication Design of Experiment (DOE) method.

As for 300 V power switching diode, the focus is on the ESD improvement. This power switching diode has the same cross section structure design as the 250 V which is shown in Figure 1.2, except the smaller die size of 400 µm x 400 µm. Typically, as the feature chip size is smaller and complexity of semiconductor fabrication technology is more, resolving ESD-induced reliability issues have become more challenging.(Z. Qiang Cui, Juin J. Liou, Jean-Jacques Hajjar, Javier Salcedo, 2015). Therefore, by comparing the ESD performance of 250 V and 300 V power switching diode units, the 250 V P-i-N power switching diode can sustain more than 1 kV surge during ESD HBM and more than 400 V surge during ESD MM due to the larger die size. But for 350 V P-i-N power switching diode with a smaller die size, it can only sustain less than 500 V surge during ESD HBM and less than 400 V surge during ESD MM.

In this work, failure analysis on poor ESD performance units from 300 V P-i-N power switching diode is performed too observe the detail magnification image of the failure spot. After de-processing and decorative etch on the sample, the metal spike damage observed under the Scanning Electron Microscope (SEM) in the diode is confined to edges of the junction as shown in Figure 1.3.

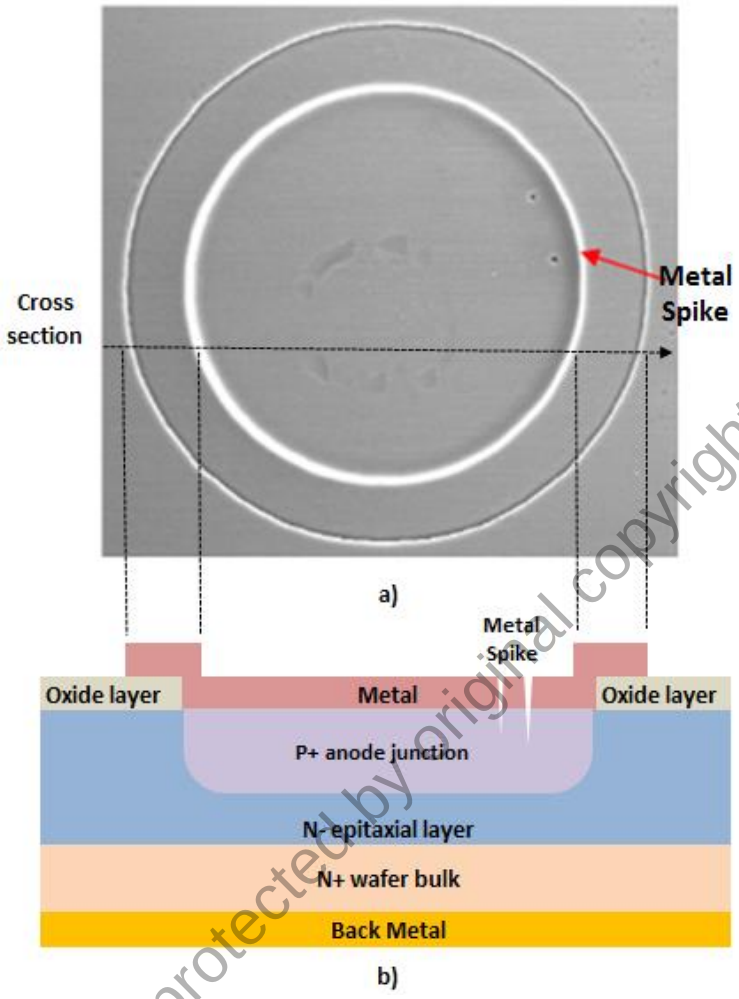

Figure 1.3: a) Top view of SEM images of ESD failures diode after de-processing and decorative etches. The metal spike dots that indicated as the red arrow are confined at the edge of junction b) Cross section illustration of the diode region

In Figure 1.3, the arrows indicate the weak points for the planar diode at the anode junction curvature where the exhibits the highest junction parasitic capacitance. During the ESD surge testing, the high current cause local heating in short timescale where the design of the junction does not allow heat flow to the surrounding regions equally. A hot spot can form and lead to metal migration and short-circuit of the junction. This metal migration is called metal spike. The red arrows indicate the metal spike which is the weak points for the planar diode at the anode junction curvature in Figure 1.3. These failures are further shown

to be caused by poor ESD. In order to study the improvement of the ESD performance, 300 V power switching diode available commercial device is used. The exploration and study of the P+ anode junction curvature profile changes in term of altering the resistivity and the junction depth of the P+ anode junction is carried out.

The diffusion of the P+ dopant into N- epitaxial layer will cause the junction depth of the N- region to be shortened. The deeper the junction depth of the P+ region, the shallower will be junction depth of the N- region. Thus lower reverse breakdown voltage will be obtained which due to more of the intrinsic region is consumed to form a P+ region. So, to improve the ESD performance of the power switching diode through the changes of the P+ anode junction depth and resistivity, a reduction of the reverse breakdown voltage will need to take into consideration. A series of the TCAD simulation and DOE will be performed to shows the effects of the anode junction formation process time and temperature on the ESD performance of the 300 V switching diode.

Whereas for the switching performance will not take into account of the both 250 V and 300 V P-i-N power switching diode optimization. The is because the key process of platinum diffusion to determine the switching performance is done after the N- epitaxial layer and P+ anode junction profile optimization.

1.3 Research objective

The objectives of the research can be summarized as follows.

- To improve 250 V power switching diode (with die size of 468 µm x 468 µm) reverse bias breakdown voltage through epitaxial layer optimization using TCAD simulation and DOE.

- To improve ESD performance of 300 V power switching diode (with die size of 400 µm x 400 µm) through the P+ anode junction profile characteristic in term of junction depth and resistivity using TCAD simulation and DOE.

Two commercially available power switching diode devices are the interest in this work which are 250 V and 300 V. The device failure for these two types of diode encourages us to explore and to understand the problem. The failures are low breakdown voltage for 250 V power switching diode and poor ESD performance for 300 V power switching diode.

For the first objective, 250 V P-i-N power switching diode with larger die size of 468 µm x 468 µm are used to investigate the effects of changes in intrinsic i-region width on the reverse bias current-voltage (I-V) performances. The intrinsic i-region is referring to the N- epitaxial layer of the substrate. In this thesis, the objective is to increase the reverse breakdown voltage from 250 V to 450 V. The reason of increasing reverse breakdown voltage is to widen the operating range of the switching avalanche diode that can be operated more than 300 V. Since P-i-N diode operates in a thickness-limited mode, which is controlled by the width of n- epitaxial layer i-region, the factors need to be taken into consideration is the epitaxial layer specification which includes epitaxial thickness and epitaxial resistivity. The given specification for epitaxial thickness is from 34 – 42 µm with resistivity ranges from 26 – 32 ohm.cm. With the fixed P+ anode junction depth, we will monitor the variable of the epitaxial thickness and resistivity that give us the reverse breakdown voltage of 450 V.

For the second objective, the attention will focus on the ESD performance improvement of the 300 V power switching diode with die size of 400 µm x 400 µm. The power switching diode of 300 V has a smaller die size compare to 250 V power switching

diode. With the same diode cross section design, the P-i-N power switching diode structure consists of circular shaped boron diffused P+ anode junction into the intrinsic region. The profile of the P+ anode junction can be changed by changing the process drive time and process temperature of the boron pre-deposition process and diffusion process.

1.4 Research scope

The research scope in this research is mainly divided into four main stages. The initial stage of this research includes identifying the existing problem of both low range (< 300 V) and high range (> 300 V) voltage power switching diode.

Second stage of the research scope is about validating for the improvement hypothesis of power switching diode via TCAD simulation.

For third stage of research scope, the implementation of the improvement that validated from the TCAD simulation result on the wafer fabrication using DOE approach. During the third stage, validation with fabrication of power switching diode is executed to get the real result. The DOE method is applied in the third part together with power switching diode fabrication to prepare samples for analysis and verification. Fabrication of a power switching diode included oxidation, photolithography, etching and metallization process.

Once fabrication processes completed, the samples are tested for its functionality as the fourth stage. Functionality test can be divided into two types which are the non-destructive test and destructive test. The non-destructive functionality test included electrical testing to check for the forward voltage, reverse leakage current and reverse breakdown voltage. The destructive analysis in this work scope includes the ESD surge test on human body model (HBM) and machine model (MM).

The non-destructive device characterization analysis is performed using JMP statistical software on the electrical characteristic. The core of the electrical testing is to validate the hypothesis in earlier stage. Multiple units across variety of process groups wafers will be tested using probe tester. The multiple data point will be compiled using JMP statistical software to monitor the electrical performance data distribution. With the final confirmation analysis result that obtained with JMP statistical software, a verification process to repeat the exact series of the wafer fabrication process are carried out to verify the consistency of the electrical performance and the hypothesis that made earlier from the TCAD simulation.

Besides non-destructive analysis, we also perform ESD surge test as the destructive analysis to validate the hypothesis and the impact of the process changes as well.

1.5 Thesis Organization

The thesis has covered the simulation, wafer fabrication and characterization of the P-i-N power switching diode. Chapter 1 brings an insight of research to the audience. The fundamentals and also evolution of power switching diode are discussed in literature review section Chapter 2. Besides fundamental theory, the application of power switching diode is discussed too.

Chapter 3 has demonstrated the process flow of designing the experiments and also power switching diode wafer fabrication process. Device characterization test after fabrication is also discussed in this chapter. There are two types of device characterization test, the destructive and the non-destructive. Characterization test carry the purpose to test