Design and Implementation of Laser Missile Frequency Jamming System Using Spatial Parallelism on FPGA for Better Performance and Throughput

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DESIGN AND IMPLEMENTATION OF LASER MISSILE FREQUENCY JAMMING SYSTEM USING SPATIAL PARALLELISM ON FPGA FOR BETTER PERFORMANCE AND THROUGHPUT

by

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To my beloved mother, father, and wife

"I would never achieve this without all of you"

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LIST OF ABBREVIATION

AADL	Architecture Analysis and Design Language
ASIC	Application-Specific Integrated Circuit
BCD	Binary Coded Decimal
CAD	Computer Aided Design
CB	Connection Block
CFAR	Constant-False-Alarm-Rate
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CREW	Current Read Exclusive Write
DDL	Double Dabble Algorithm
DDR	Dynamic Random Access
DGAS	Distributed Global Address Space
DLL	Delay-Locked Loop
DLP	Data-Level Parallelism
DSK	Digital Signal Processing Kit
DSM	Distributed Shared Memory

DSP	Digital Signal Processing
FIFO	First-In-First-Out
FMCW	Frequency Modulated-Continuous Waveform
FPGA	Field Programmable Gate Array
FSK	Frequency-Shift Keying
GPIO	General Purpose Input / Output
GSB	General Switch Box
HDL	Hardware Description Language
IEEE	Institute Of Electrical And Electronic Engineering
ILP	Instruction-Level Parallelism
IP	Intellectual Property
IR	Invisible Radiant
LCD	Liquid Crystal Display
LF	Loop Filter
LIFO	Last-In-First-Out
LUT	Look-Up Table
MIMD	Multiple Instruction Multiple Data

MISD	Multiple Instruction Single Data
MMP	Massively Multi-processing
MPSoC	Multiprocessor System-on-Chip
NCD	Native Circuit Description
NEEK	Nios II Embedded Evaluation Kit
NUMA	Non-Uniform Memory Access
PD	Phase Detector
PE	Processing Element
PLD	Programmable Logic Devices
PLL	Phase-Locked Loop
PRAM	Parallel Random Access Memory
PWM	Pulse Width Modulation
ROM	Read-Only Memory
RTL	Register Transfer Level
SAR	Synthetic-Aperture Radar
SARH	Semi-Active Radar Homing
SIMD	Single Instruction Multiple Data

SISD	Single Instruction Single Data
SMP	Symmetric Multi-processing
SoC	System on Chip
SRAM	Static Random-Access Memory
TLP	Thread-Level Parallelism
UMA	Uniform Memory Access
UML	Unified Modeling Language
VCO	Voltage-Controlled Oscillator
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

Reka bentuk dan Pelaksanaan Sistem Laser Missile Frekuensi jamming Menggunakan Spatial Parallelisme pada FPGA untuk Prestasi Yang Lebih Baik dan Pengendalian Yang Lebih Baik.

ABSTRAK

Apabila sesuatu pemprosesan terdapat banyak data masukan pada satu masa, peneroka mekanisme keselarian diperlukan. Keselarian ruang yang boleh menyediakan keupayaan untuk menduplikasi petugas bagi modul tertentu. Kekerapan sistem jamming semasa mempunyai keupayaan untuk mengesan isyarat satu frekuensi pada satu masa dan menghadapi isu kritikal seperti kelewatan dalam pemprosesan isyarat. Kelewatan ini dianggap sebagai sebab semula jadi untuk modul sistem seni bina atau cara di mana isyarat-isyarat ini diproses atau keupayaan pengkomputeran modul ini. Mengesan frekuensi yang dipancarkan daripada berganda dicadangkan laser peluru berpandu pelancar dilakukan dalam kajian ini. Menggunakan mekanisme keselarian ruang atas FPGA memperkaya sistem yang dicadangkan dengan pelbagai ciri-ciri kritikal. Ciri-ciri ini diperolehi dianggap sebagai faktor utama dalam mana-mana kegagalan sistem atau kejayaan seperti mengurangkan kos sistem, mempercepatkan prestasi sistem serta meningkatkan sistem bersama dengan mengurangkan penggunaan kuasa. Seluruh sistem Laser Missile Frekuensi Jamming direka dan dilaksanakan pada Field Programmable Gate Array (FPGA) cip. Sistem yang dicadangkan disintesiskan dan dinilai berdasarkan Nios II Embedded Evaluation Kit (NEEK). Prestasi sistem yang dicadangkan menunjukkan kecepatan berskala dan prestasi sistem boleh dipertingkatkan. Pelaksanaan itu mencapai pemprosesan diterima dan kerumitan yang lebih rendah (saiz kecil (2604)) elemen logik dari segi penggunaan sumber FPGA dan kekerapan operasi yang tinggi (200 MHz)). Di samping itu, kaedah reka bentuk struktur juga membolehkan kebolehan untuk diskala oleh sebagai keseluruhan sistem berkembang.

Design and Implementation of Laser Missile Frequency Jamming System Using Spatial Parallelism on FPGA for Better Performance and Throughput

ABSTRACT

When a processing multiple data input at a time, exploring the parallelism mechanism is required. The spatial parallelism can provide the ability for duplicating the task for a specific module. The current Frequency Jamming systems have the ability to detect one frequency signal at a time and confront critical issue like delay in processing the signals. This delay is considered as a natural reason for the system modules architecture or in which way these signals were processed or even the computational ability of these modules. Detecting the emitted frequencies of four proposed laser missiles launchers is done in this research. Applying the spatial parallelism mechanism over the FPGA enriches the proposed system with multiple critical features. These gained features are considered as a key factor in any system failure or success like decreasing the system cost, speed up the system performance as well as increasing the system alongside with decreasing the power consumption. The entire Laser Missile Frequency Jamming system is designed and implemented on Field Programmable Gate Array (FPGA) chip. The proposed system is synthesized and evaluated based on the Nios II Embedded Evaluation Kit (NEEK). The performance of the proposed system shows scalable speedup and enhanced system performance. The implementation has achieved acceptable throughput and lower complexity (small size (2604)) logic elements in terms of FPGA resource usage and high operating frequency (200 MHz)). In addition, the structural design methodology also allows scalability of the ECCA as the entire system grows.

CHAPTER 1

INTRODUCTION

1.1 Overview

The most core aspects that should be addressed in system development are improving the overall system performance as well as pushing the system towards responding in real-time manner. These features can force hard constraints in the complex systems; therefor the need for adopting more and more sophisticated mechanisms which can be embedded within these systems is increasing. The embedded systems can perform much more complexity than the general purpose systems.

The embedded systems considered as a reactive system, meaning that these systems react to the environment in a continuously manner and most of those embedded systems have the real-time respond characteristic. The trend in development embedded systems is moving away from being restricted to a specific function while the alternative trend was the flexibility to add, modify, and even delete sub-functionality units of the embedded system. In fact, the changes in embedded systems world are occurring even while this research is being written and the ambition is to make these embedded systems faster and smaller as possible as can. One of the application areas that the embedded systems cover is the mission critical which includes frequency jammer, radar, avionic, and spacecraft.

This thesis is to provide the ability to processing multiple signals at time and detect the frequencies used to guide multiple laser missiles that can be launched to strike a target and to control multiple defused platforms in the same time in case that more than one missile launcher are used to strike a specific target. The key proposition of this thesis is that the efficiency of the embedded systems that can used to implement jamming

functionalities can be improved via applying the parallelism principle (Shalf, 2007). The proposed design improved the utilization of the processing cores since that the sub-functionalities has been distributed among those cores to be processed which resulting in increasing the system overall performance and also reducing the total time required for processing. Extra functionality units have been added to the proposed system to decrease the processing time and to provide a concurrent processing design.

Although this thesis focused on improving the system performance and increasing the throughput via applying the spatial parallelism, the relatively complexity has been taken into consideration whereas the mapping tasks from the high-level designing stages into a lower-level sub-tasks could reducing the complexity of the functionality units. The proposed design strived to simplify the complex tasks in order to provide a system with real-time respond as much as possible. The hard competition between the Giant companies and the need to meet the customer requirements made it imperative for those companies to consider some key features when designing and implementing their systems. The most important features which should be taken in consideration are the reconfigurability, cost, power consumption, and time to market. The FPGA has all of these features and more characteristics like the ability to process data in parallel manner, and reliability.

Nowadays FPGA-based systems could combine the advantages of both of DSPs and ASIC which resulted in systems capable for rapid development cycles, high flexibility, high reliability, easy upgrading, and moderate costs (Demler, 2011; Joost & Salomon, 2005; Wilson, 2009). This research used the FPGA to design and implement its functional units to gain the advantage of these features and even more. The harnessing of

the FPGA resources in this project resulted in higher performance and better throughput since the spatial parallelism has been used to implement it.

As the code is broken into discrete parts, each is treated as an independent process that can be executed concurrently via various modules. In this case, the interpolation algorithm can be clearly divided into a set of independent processes using a coarse-grained approach to parallelism in which the computation of an interpolated value for each grid cell in the lattice is treated independently from the computation of values for all other cells. Where firstly, the jammer analyses the signal's spectrum which was received from frequency hopped transmitter, extracts the signal's features; then takes the features to the frequency synthesizer and controls the frequency synthesizer to produce the same hopping frequency; finally sends the narrow-band interference signals to display units on board like the LCD touch screen.

The time and the cost as well as the power consumption consider as critical factors which determines the failure or the success of any systems in general and the embedded systems specially. To solve these problems, the need for processing multiple signals by a system instead of processing single signal at a time is required. Accordingly, FPGA-based frequency jamming system design is proposed to process multiple signals using the spatial parallelism principle. The proposed design consists of modules suitable for control-intensive tasks and custom accelerator cores suitable for data-intensive tasks. The use of the system functionality units reduces the design effort to process a single data input per time separately.

1.2 Problem Statement and Motivation

When the functionality of the system is critical and closely related to human life, the ability of these systems to process data in real-time respond and taking an accurate decision-making with lower complexity as much as possible must be considered. The frequency jamming system can be included within this category, where the computational platform for such a system should be accurate, efficient, and robust. In addition, such systems with functionality like the jamming system should be portable and scalable.

Nowadays processing platforms of the frequency jamming systems have a core problems represented in their complexity and the time required to process signals. The delay of processing can be considered as a nature result for the system design, the power consumed to perform the system functionality and other reasons. For these key reasons and more, these platforms used to implement the frequency jamming functionality are not capable to provide the requirements for effective and fast processing systems. In order to reduce the complexity of the system and reduce the delay time required for processing data, the spatial parallelism principle can be applied with a concurrent design to have an efficient and real-time frequency jamming system.

The other issue which has been handled by this proposed design is to process multiple signals at a time and to control multiple platforms to direct the platforms towards the air jets.

1.3 Research Objectives

The aim of this research is to design and implement a frequency jamming which harnessed the principle of the spatial parallelism and obtain the full advantage of the FPGA unique features. In order to achieve this aim, the objectives of this research are:

1. To design and implement an embedded frequency jamming system using spatial parallelism on FPGA including the following specifications:
    i. Decreased system overall complexity level, improved operating frequency, consumed chip resources, and improved throughput.
    ii. Speed up the processing time, increase the processing cores utilities, and reduce the delay occurring in the processing modules.
2. To verify and evaluate the design performance of the system by using FPGA CAD tool and on board testing.

1.4 Research Scopes

This research focused on aspects which should be improved to increase the frequency jamming systems performance and throughput via using the characteristics embedded within the FPGA as well as explaining the designed system which has been implemented on the FPGA's board. These aspects which has been improved are included the processing of multiple data per time by harnessing the spatial parallelism principle. The results obtained from this research has been presented and analyzed not for the final system response only, but also for each stage of the system modules in order to be understood by other researchers and readers.