DEVELOPING INCREMENTAL CAPACITY DURING SEASONAL DEMAND FOR TECHNOLOGIES BEYOND 90 NM IN SEMICONDUCTOR FABRICATION INDUSTRY

by

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LIST OF SYMBOLS

$\sum$	Summation over defined variable
λ	Lambda
σ	Sigma, standard deviation
D^2	Sample variance
df	Degree of freedom
e	Exponential
mm	Millimeter
n	Sample size
N	Population size
R^2	R-square, coefficient of determination
µm	Micron meter

LIST OF ABBREVIATIONS

ArF	Argon-Fluoride
APC	Advanced Process Control
APF	Advanced Productivity Family
ASP	Average Selling Price
BNI	Bottleneck Index
CAGR	Compounded Aggregate
CAPEX	Capital Expenditure
CIM	Computer Integration Manufacturing
CMOS	Complementary Metal Oxide Semiconductor
CR	Critical Ratio
CT	Cycle Time
DPML	Day per Mask Layer
EDD	Earliest Due Date
E&E	Electrical and Electronic
Equip. ID	Equipment Identification
FAB	Semiconductor Fabrication
FDC	Fault Detection Control
FIFO	First In First Out
FWLRANK	Dispatching Policy
GF	Global Foundry
HF	Hunger Factor
IC	Integrated Circuit
IDM	Integrated Device Manufacturer
JDBC	Java Database Connectivity

KrF	Krypton-Fluoride
LBA	Least Balance Ahead
LP	Lowest Priority
LPStep	Lowest Priority Step
MAPE	Mean Absolute Percentage Error
MBP	Most Batch Pieces
MedAPE	Median Absolute Percentage Error
MES	Manufacturing Execution Systems
ODBC	Open database Connectivity
OEE	Overall Equipment Effectiveness
PE	Process End
PEMANDU	Performance Management Delivery Unit
PS	Process Start
RF	Radio Frequency
RUL	Ready To Unload
SDL	SilTerra Dispatching List
SEMI	Semiconductor Equipment and Materials International
SICAS	Semiconductor Capacity Utilization
SIA	Semiconductor International Association
SMIC	Semiconductor Manufacturing International Corporation
SPC	Statistical Process Control
SPT	Shortest Processing Time
SRPT	Shortest Remaining Processing Time
SQL	Structured Query Language
SQN	Smallest Queued Number

SSU	Same Equipment Setup
STNCAPTY	Station Family Capacity Type
STNFAM	Station Family or Equipment Group
STNFAML	Station Family Location
TI	Track In
TO	Track Out
TSMC	Taiwan Semiconductor Manufacturing Company
UMC	United Microelectronics Corporation
USD	United States Dollar
WPH	Wafer per Hour
X-site	Equipment preventive maintenance application

Pembangunan penambahan kapasiti pada permintaan bermusim untuk teknologi 90 nm dan berskala besar di semikonduktor industri

ABSTRAK

Kajian ini bertujuan mencari cara baru untuk menambah kapasiti pengeluaran wafer sebanyak 10 peratus dengan masa singkat dalam pemprosesan semikonduktor untuk memenuhi pasaran mendadak. Trend pasaran turun naik meramalkan kemungkinan permintaan mendadak sebanyak 10 peratus akan berlaku pada masa terdekat dan sejarah menunjukkan permintaan pernah mencecah 35 peratus. Oleh itu, penyelidik dan industri antarabangsa sentiasa memfokuskan menambahbaikan mesin pengeluaran untuk menambah kapasiti pengeluaran. Proses pembuatan wafer yang rumit kerana langkah pemprosesan wafer di antara 300 hingga 1000 dan masa kitar antara 30 hingga 90 hari, menyebabkan masa yang diambil sehingga 6 bulan untuk mencapai penambahbaikan. Cara ini tidak dapat meningkatkan kapasiti pengeluaran dengan kadar cepat untuk memenuhi permintaan pasaran yng mendadak, malah ia mengurangkan kapasiti pengeluaran akibat daripada masa mesin yang digunakan untuk ujian penyelidikan. Oleh sebab itu, kebanyakan industri yang berskala besar telah menetapkan untuk sentiasa melabur sekurang-kurangnya USD20 hingga USD30 juta untuk membeli mesin yang baru untuk tambahan pengeluaran 1,000 wafer sebulan. Pelaburan ini tidak mampu dilakukan oleh syarikat berskala kecil dan sederhana. Penyediaan mesin baru mengambil masa antara 10 hingga 14 bulan untuk melayakkannya beroperasi. Terkini ialah bekerjasama dengan pengusaha semikonduktor yang lain untuk berkongsi kapasiti. Cara ini juga mengambil masa melebihi 6 bulan untuk kelayakan pengeluaran untuk sesuatu produk baru. Kesimpulannya, kesemua cara yang telah ada tidak dapat menampung permintaan tinggi yang mendadak. Setelah dikaji dengan teliti, gabungan pasaran turun naik dengan komplikasi pembuatan wafer telah berjaya menghasilkan penemuan sistem peningkatan kapasiti yang dapat menampung lebihan pengeluaran daripada permintaan yang mendadak tanpa mengeluarkan kos pelaburan. Ini dilakukan dengan meminjam kapasiti masa depan untuk digunakan pada masa kini. Cara ini dapat dilakukan dengan mengurangkan langkah perkongsian untuk proses pada mesin yang mempunyai kapasiti terendah. Penyusunan semula kapasiti ini dilakukan dengan memberi keutamaan kepada produk yang mempunyai baki langkah proses yang terendah. Pada peringkat permulaan, pembinaan semula kapasiti asas dilakukan dengan menggunakan campuran produk yang aktif dan dijangka mempunyai hayat melebihi 1 tahun. Pengumpulan data setiap mesin dan produk berlandaskan spesifikasi SEMI serta kajian perpustakaan yang lain, kapasiti asas pengeluaran berjaya dibina pada 22,511 wafer sebulan. Seterusnya, simulasi model dibangunkan dengan tatarajah komponen penting seperti campuran produk,masa kitar, yang digunakan untuk membina WIP dan sistem penjadualan untuk WIP dan mesin. Model simulasi Autoshed AP yang diintegrasikan dengan sistem APF telah digunakan untuk analisa ini dan bejaya mencapai tahap ketepatan pada 97 peratus. Simulasi model ini juga telah berjaya memberi keputusan sama seperti ujikaji kajian perpustakaan yang lepas. Eksperimen pada simulasi model ini berjaya menambah kapasiti sebanyak 21 peratus berbanding kapasiti asas dan telah berjaya menyakinkan pelaksanaan pada peringkat sebenar. Di peringkat sebenar, kapasiti tambahan berjaya ditingkatkan sebanyak 33 peratus pada sepanjang pelaksanaannya. Cara pelaksanaan ini diteruskan hingga masa kini dan tesis ini berjaya mencapai objektifnya.

Developing incremental capacity during seasonal demand for technologies beyond 90 nm in semiconductor fabrication industry

ABSTRACT

This research is to develop a new approach to accelerate capacity increment from unexpected additional demand at semiconductor fabrication by 10%. The issue is from unpredictable demand at short notice to increase capacity by 10% in future period or as high as 35%historically. Current improvements practice for capacity increment such as increase in equipment throughput, availability and manufacturing efficiency will take up to six months to be effective are not able to solve this issues. This is due to the processing steps that range from 300 to 1000 with cycle time 30 to 90 days. Plus, the new improvements from equipment usually need data to verify electronically to understand the impact from the product quality and reliability. The traditional improvements from equipment are still relevant for medium or long-term solution. Another approach for capacity increment is through investing in new or refurbished equipment. Investing new equipment required Capital expenditure (CAPEX) range from USD 20 to 30 million for additional capacity of 1,000 wafers per month. This huge investment will takes up from 10 up 14 months for equipment ready to support production and only afford by big scale companies. Newly popular strategy is to do outsourcing to another fab, but again, initial stages needs six to nine months for product to qualify for production, however when the outsourcing fab is qualified and fully loaded, it is not guaranteed to absorb additional loading. Thus, make this research topic valuable and significant for the situation current economic trends. The new approach is based on the philosophy of borrowing the future capacity into current time when immediate capacity increment is needed. As the capacity usually determine by total number of processing steps that need to process at the constraint equipment, this research concluded that the higher re-entrance steps caused lower the capacity of a fab at exponential trend. Through similar approaches taken from specification from SEMI and others literature the baseline capacity successfully developed at 22,511 wafers per month. Therefore in this case to increase the capacity at a time, it needs lowered re-entrance steps, by recalculating the capacity not based plan order demand but by using preferred WIP to reduce the impact from exponential impact. In order to this, the cycle time and the equipment output needs to be integrated in production systems for real time validation and the information then needs to store into databases and integrated with simulation model for the system to be able identify immediately for the WIP that able to help to increase the capacity with high accuracy planning. The data collection and the simulation models used commercial software from Applied Material which is Advance Productivity Family and AutoshedAP, that proven in this research at 97% accuracy for 30 days output WIP forecasting. The simulation results in the models successfully demonstrated accelerate capacity increment by 21%, and actual implementation of capacity increment by 33% and the research meets its original objective.

CHAPTER 1

INTRODUCTION

1.1 Semiconductor Fabrication

Semiconductor factories are complex environment that extend across several manufacturing domains (ITRS, 2008, 2010, 2012). Fig 1.1 shows the process of semiconductor fabrication scopes starts with wafer manufacturing, then chip manufacturing that involves probe/e-test, backgrind, singulation, and through to product manufacturing where the final package is assembled and tested. Semiconductor fabrication is the heart of the electronics supply chain, where a physical integrated circuit (IC) is fabricated and developed (Ang, 2006; Chyi, 2007; Kowaliski, 2010).

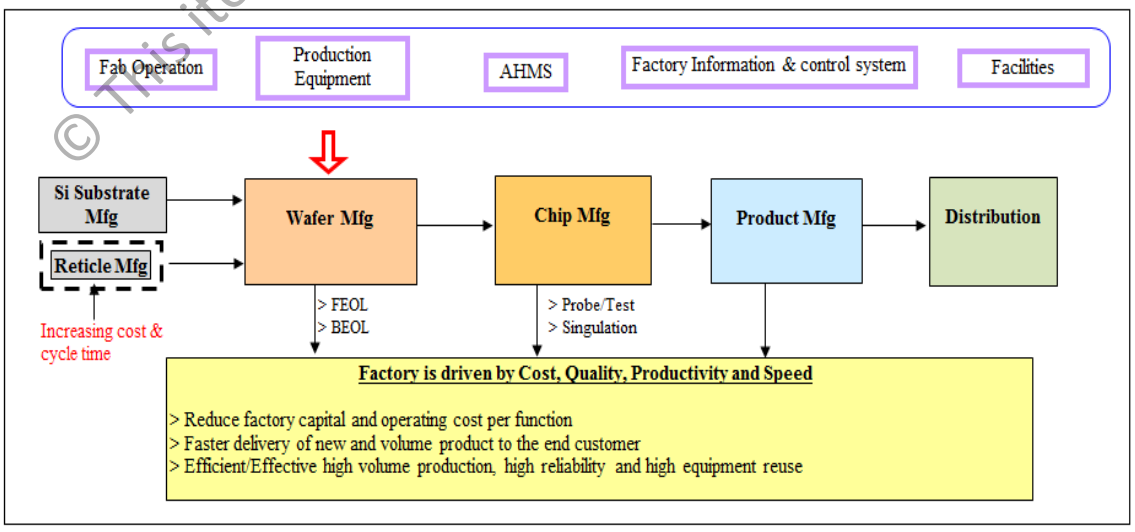

Figure 1.1: Overall semiconductor factory integration scope defined by International Roadmap of Semiconductor.
(Source: ITRS, 2008, 2010, 2012).

A semiconductor fabrication plant, commonly called a fab, is a clean room facility that manufactures integrated circuits (Chyi, 2007; PEMANDU, 2012; Robert & Yoshio, 2007). Full of expensive manufacturing equipment, cost estimates for building a new fab are over one billion US dollars, with values as high as 3 – 4 billion (SIA, 2011; TSMC, 2010; Zack, 2013). For example, chip manufacturer TSMC invested 9.3 billion dollars in its 300 mm wafer manufacturing facility in Taiwan in 2013 (TSMC, 2010). Capital investment for expanding capacity of existing 200mm fab by an additional 1,000 wafers per month requires an investment of USD 20 – 30 million (PEMANDU, 2012).

The first stage in the wafer production process is for a chip to be designed by a customer (Chyi, 2007; Global Foundries, 2012; SilTerra Manufacturing Systems Department, 2013). Before moving into scale production, small quantities of wafers are produced for prototyping (Chyi, 2007; SilTerra Manufacturing Systems Department, 2013; TSMC, 2010) using the least amount of equipment possible because the quantity is small and the customer needs the prototype in the shortest time possible (Chyi, 2007; SilTerra Manufacturing Systems Department, 2013). Once the product is ready for volume production, the improvement plans qualify more steps for the products on the rest of the equipment to allow the new product to absorb more equipment capacity. This method leads to capacity increments to manufacture the respective products and is widely discussed topic in conferences and journal papers.

Table 1.1 lists the largest semiconductor factories or fabs in the world the globe, with the major players located in Asia, North America and Europe (Gartner, 2012). The list of companies, sorted on revenue, reports Malaysia's SilTerra Sdn Bhd, which is

owned by Khazanah and has a fab facility in Kulim, as 15th (Gartner, 2012). Much of the industry's IC fabrication revenue comes from Taiwanese companies. The top fab based on revenues is Taiwan Semiconductor Manufacturing Corporation (TSMC). This research uses literature from TSMC reports, Global Foundries representative updates, UMC and SMIC as part of the discussion to review and compare their process and production data related to this research.

Table 1.1: Major IC foundries, ranked by revenue 2012 (Gartner, 2012).

2012 World Rank	Company (Country Headquarters)	2012 Sales ($USD M)	2012 Share of Total
1	TSMC (Taiwan)	17,167	53%
2	GlobalFoundries (U.S)	4560	14%
3	UMC Group (Taiwan)	3730	12%
4	SMIC (China)	1682	5%
5	Hua Hong Grace (China)	940	3%
6	TowerJazz (Israel)	644	2%
7	Vanguard (Taiwan)	582	2%
8	Dongbu HiTek (S. Korea)	540	1%
9	WIN (Taiwan)	382	1%
10	SSMC (Singapore)	370	<1%
11	X-Fab (Europe)	260	<1%
12	Altis (Europe)	228	<1%
13	Telefunken (Europe)	220	<1%
14	He Jian (China)	215	<1%
15	SilTerra (Malaysia)	213	<1%
16	ASMC (China)	149	<1%
17	Lfoundry (Europe)	140	<1%
18	Mosel-Vitelic (Taiwan)	34	<1%
-	Others	254	<1%
-	Total	32,310	

One of the main strategies SilTerra Malaysia Sdn Bhd is currently researching is how to improve revenue by improving fab capacity. This research forms the basis of this study. Their research and this study use real data from production equipment and wafer specifications, such as process flows, processing times, equipment shared steps, equipment availability, and method of process.

Literature shows that the main challenge to improve capacity is the equipment shared steps concept, where products are repeatedly processed through the same equipment, from three to fifteen times, with processing times from 45 minutes to nine hours depending on the deposit thickness, surface removal rates, implantation ion dose, or complexity of pattern exposure at respective lithography layers (Asmundson, J., Rardin, R. L., Turkseven, C. H., Uzsoy, 2009; C. F. Chien & Chen, 2011; Gultekin, 2012). When different products are mixed in a production loading plan the shared steps increases, which can increase setup changes for the equipment, reduce equipment availability, and increase the complexity of the overall improvement process (Ang, 2006; C. F. Chien & Chen, 2011; Chiou & C., 2013; Fredendall, Ojha, & Patterson, 2010). With investment in semiconductor fabrication equipment costing millions of dollars, competitive pressures to produce more products at the lowest cost, and cyclic or trending markets (Ang, 2006; H. A. David, 2012; Leachman, Ding, & Chien, 2007), research in improving or maximizing output is important (Ang, 2006; H. A. David, 2012; Leachman et al., 2007).

In Malaysia, fab process research is limited because there are only a handful of less experienced fab operators who are unable to convert operational gaps into research opportunities. The exploration in this research topic enriches our understanding of wafer

fab challenges and potential improvements. It carefully reviews all the variability parameters existing in wafer fabrication and explores new approaches to rapidly increase fab capacity to meet sudden surges in demand requirements.

1.2 Semiconductor Fabrication Business Outlook

Semiconductor fabrication, physically fabricating and developing integrated circuits (IC), is the heart of the electronics supply chain (Zin, 2010). Nowadays, most chips are fabricated in one of the top 200 or 300mm semiconductor fabrication pure play foundries, such as those owned by Taiwan Semiconductor Manufacturing Corporation (TSMC), United Microelectronics Corporation (UMC), Global Foundry (GF) and Semiconductor Manufacturing International Corporation (SMIC). These organizations have revenues in excess of USD15 billion per year (see Table 1.1) (Gartner, 2012). In Malaysia, the major foundries are SilTerra in Kulim, Kedah, and X FAB in Kuching, Sarawak (Zin, 2010). The key difference between a foundry and integrated device manufacturer (IDM) is the flexibility of processing mixed products at lower production costs (Kowaliski, 2010).

Pure-play foundry fabs have increased revenues over the last 10 years, compared to IDM fabs. Fig 1.2 shows revenues since 2003. As a result, more IDMs are changing to become foundries, which fuels the need for continuous improvement in foundry fab efficiency. Recently, AMD announced that its processor manufacture has been migrated from an IDM to foundries owned by Global Foundries (Kowaliski, 2010). Another change is that Intel and Taiwan Semiconductor Manufacturing Co. collaborated on the Atom chip production (CNET, 2009). Others IT companies such as Broadcom,

Qualcomm, and IBM already fabricate their chips in foundries, which supports the market trend towards semiconductor foundries compared with IDM.

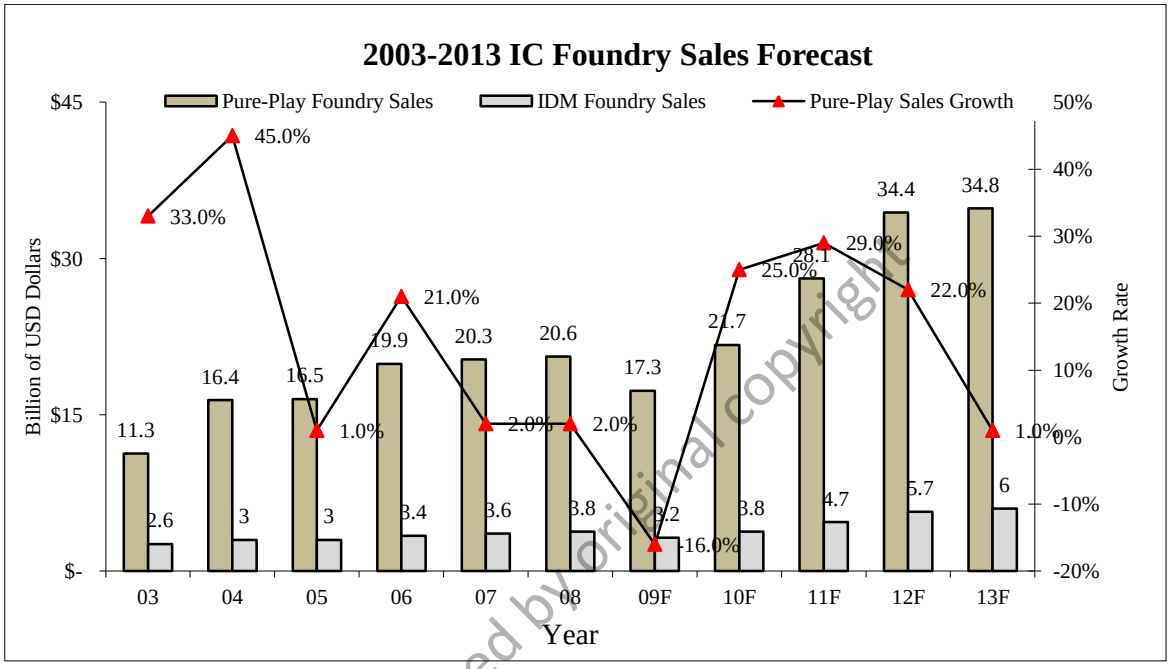

Figure 1.2: IC foundry sales continue to have better growth than IDM, and pure play foundries are expected to gain share against IDM foundries.
(Source: IC Insights, 2009).

In line with this growth is the fact that more products will be mixed and processed together in the same foundry, leading to work in progress (WIP) management challenges that require efficient application of shop dispatching policies. Analysis conducted by Semico Research in 2007 shows that the aggregate sales of game player devices, primarily those from Sony and IBM, reached 1 million within three months (Ogg, 2011). A staggering sales rate when compared with black-and-white television sets, which took almost 20 years to reach a similar figure. Since the demand for electronic goods has intensified, evidenced by October 2011 preorder sales for the iPhone 4S reaching more than 1 million on the first day (Ogg, 2011), electronics