FABRICATION AND CHARACTERIZATION OF ENGINEERED TUNNEL BARRIER FOR NONVOLATILE MEMORY APPLICATION

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DECLARATION OF THESIS

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LIST OF ABBREVIATIONS

Al	=	Aluminum
BOE	=	Buffered Oxide Etch
CHE	=	Channel Hot Electron Injection
CMOS	=	Complementary Metal Oxide Semiconductor
DRAM	=	Dynamic Random Access Memory
EEPROM	=	Electrically Erasable Programmable Read Only Memory
EPROM	=	Erasable Programmable Read Only Memory
FESEM	=	Field Emission Scanning Electron Microscope
HPM	=	High Power Microscope
IC	=	Integrated Circuit
ICP-RIE	=	Inductive Coupled Plasma-Reactive Ion Etching
IPD	=	Interpoly Dielectric
LOCOS	=	Local Oxidation of Silicon
LPCVD	=	Low Pressure Chemical Vapor Deposition
MOS	=	Metal Oxide Semiconductor
NAND	=	Not AND
NOR	=	Not OR
NVM	=	Non-volatile Memory
ONO	=	Oxide-Nitride-Oxide
PECVD	=	Plasma Enhancement Chemical Vapour Deposition
PR	=	Photoresist
PROM	=	Programmable Read Only Memory
PVD	=	Physical Vapour Deposition
RAM	=	Random Access Memory
SEM	=	Scanning Electron Microscope
Si	=	Silicon
SiH4	=	Silance
SiO_2	=	Silicon dioxide

Si_3N_4	=	Silicon nitride
SPA	=	Semiconductor Parametric Analyzer
SRAM	=	Static Random Access Memory
VARIOT	=	Variable Oxide Thickness
XRD	=	X-ray Diffraction

LIST OF SYMBOLS

QUANTITY	SYMBOL	UNIT
Applied voltage	V_{app}	V
Capacitance oxide	Cox	Pf
Current density	J	A/cm^2
Gate current	I_g	Ampere (A)
Drain voltage	V_{DS}	Volts (V)
Electric field	E_{inj}	MV/cm
Equavalent oxide thickness	EOT	nm
Gate area	*A*	cm^2
Gate voltage	V_G	Volts (V)
Load resistance	R_L	Ohm (**Ω**)
Load resistance voltage	V_L	Volts (V)
Permittivity of vacuums	ε_o	F/cm
Permittivity of silicon dioxide	ε_r	F/cm
Sheet resistance	R_s	ohms per square (**Ω/□**)
Thickness of oxide	t_{ox}	nm
Flatband voltage	V_{FB}	V
Threshold voltage	V_{TH}	V

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FABRIKASI DAN PENCIRIAN KEJURUTERAAN TEROWONG PERINTANG UNTUK APLIKASI INGATAN TAK MERUAP

ABSTRAK

Non-volatile memory (Memori tak meruap) adalah peranti ingatan di dalam keadaan pepejal yang boleh mengekalkan maklumat yang tersimpan walaupun kuasa tidak lagi dibekalkan, contohnya pelbagai jenis ROM dan Flash Memory. Berdasarkan mekanisme penyimpanan cas, ia boleh dibahagikan kepada dua kelas utama; peranti get terapung dan memerangkap cas. Struktur peranti yang paling banyak digunakan dalam teknologi ingatan kontemporari adalah jenis pintu terapung. Dalam ingatan jenis ini, elektron dipindahkan daripada substrat kepada get terapung, dan sebaliknya. Operasi memori ini dikenali sebagai menulis dan memadam. Untuk seni bina ingatan kilat jenis NAND pemindahan elektron telah dijalankan menggunakan mekanisme terowong yang dikenali sebagai *Fowler-Nordheim tunneling* (terowong Fowler-Nordheim), dan kecekapannya akan menentukan prestasi peranti ingatan. Mekanisme terowong ini berlaku melalui dielektrik lapisan nipis ultra, yang dikenali sebagai dielektrik terowong, yang secara fizikal dan elektrik memisahkan pintu terapung daripada substrat. Tradisinya, ketebalan SiO_2 di antara 5 nm hingga 10 nm digunakan sebagai dielektrik terowong. Ketebalan 5 nm dianggap had oksida terowong intrinsik, yang mana di bawah ketebalan ini kebocoran seperti kebocoran tekanan arus teraruh (SiLC) dan pemindahan elektron secara langsung menjadi faktor yang menonjol. Beberapa usaha telah dibuat untuk meningkatkan prestasi sel ingatan kilat dengan menggantikan SiO_2 dengan pelbagai dielektrik seperti Oxynitride, gabungan bahan-k tinggi dan sebagainya. Fokus kajian tertumpu kepada pendekatan kepada Keteblan Oksida Bolehubah (VARIOT) terowong kejuruteraan di mana struktur VARIOT tidak simetri dengan ketebalan oksida yang berkesan (EOT) di antara 5 nm kepada 14 nm dikaji di dalam bentuk struktur MOS kapasitor. Ketumpatan terowong semasa dalam struktur VARIOT menghasilkan 10^8 A/cm^2 dengan 15V voltan pengaturcaraan, berbanding 10^5 A/cm^2 untuk halangan terowong konvensional dengan voltan pengaturcaraan sama. Hasilnya menunjukkan bahawa VARIOT terowong kejuruteraan akan meningkatkan prestasi sel memori pintu terapung.

FABRICATION AND CHARACTERIZATION OF ENGINEERED TUNNEL BARRIER FOR NONVOLATILE MEMORY APPLICATION

ABSTRACT

Non-volatile memory is a solid state memory device that can retain the stored information even when the power is turned-off; examples of a variety of ROMs and Flash Memory. Based on the charge storing mechanism, it can be divided into two main classes; floating gate and charge trapping devices. The most widely used device structure in contemporary memory technology is of a floating gate type. In this type of memory, electrons were transferred from the substrate to the floating gate, and vice versa in memory operations known as write and erase. For NAND Flash Memory architecture, these electrons transfer were carried out using tunneling mechanism known as Fowler-Nordheim tunneling, and its efficiency would determine the performance of a memory device. This mechanism takes place via ultra-thin dielectric layer, known as tunnel dielectric, which physically and electrically separates the floating gate from the substrate. Traditionally, thermally grown SiO_2 thickness ranging from 5 nm to 10 nm is used as the tunnel dielectric. The 5 nm thicknesses is considered the intrinsic tunnel oxide limit, below which various leakages such as stress induced leakage current (SILC) and direct tunneling start to became a prominent limiting factors. Several efforts have been made to improve the flash memory cell performance by replacing the traditional SiO_2 with various dielectric such as Oxynitride, and combinations of High-k materials. This study focuses on the Variable Oxide Thickness (VARIOT) approach of engineered tunnel barrier where the asymmetrical VARIOT structure with the effective oxide thickness (EOT) ranging from 6 nm to 14 nm were studied in the form of MOS capacitor structure. The tunneling current density in the VARIOT structure yield 10^8 A/cm^2 at 15V programming voltage, compared to 10^5 A/cm^2 for the conventional tunnel barrier with the same programming voltage. The results show that asymmetrical VARIOT tunnel barrier would significantly improves the floating gate memory-cell performance.

CHAPTER 1

BACKGROUND

1.1 Introduction

Flash memory technologies have two main parameters governing the device performance. Firstly the programming speeds, which indicates how fast the memory contents can be programmed. For this parameter, it's desirable to achieve the programming time as short as possible i.e. < ns range. The second parameter is data retention which indicates how long it will take before the memory, lost its contents. The minimum technology requirement is 10 years retention. Current flash memory technology scaling (common technique practiced in the industry to enhance the device performance) required the shrinking of the tunnel oxide thickness (below 5 nm). This practice posed inevitable lost of data retention capability even though the programming speed is greatly enhanced. In this investigation flash memory performance of conventional and engineered tunnel barrier is presented and analyzed. This chapter focuses on the research workflow and it is simplified to overview of flash memory technology, problem statement, research objective, research scope and thesis organization.

1.2 Overview of Flash Memory Technology

Semiconductor industry has been growing rapidly in the past few decades especially in main memory market segment, driven by the semiconductor memory revolution. The revolution of semiconductor memory has to be fast due to its wellbalanced functionality and cost of semiconductor technology. Newer semiconductor technologies with new materials and manufacturing process emerge for realizing new products.

Semiconductor memory is a device, which stored information in the electronic form. The semiconductor memories can be classified into two main types of data mechanism; namely data storage and data access. Both, correspond to two main groups; volatile and nonvolatile memory (Kang, 2003). Volatile memory loses data as soon as the system is turned off and requires constant power to remain viable, while the nonvolatile memory does not lose its data (Makwana, 2004). A common nonvolatile memory device is a MOS transistor which consists of source, drain, an access or control gate and floating gate (Brown, 1997).

Flash memory is one of the non-volatile memory devices that have been continuously growing and it is mass solid-state storage application that relies on the success of flash technology in the electronic industry era. Over the past few years, flash memory has been used in portable electronic products such as cellular phones, laptops, digital cameras, modems, memory sticks, video game cards and personal digital assistance (PDAs) (Misra, 2011). During the evolution of flash memory technology, tunnel barrier materials and their thicknesses are the key important factors in improving its performance. Tunnel barrier is a vital counterpart in flash memory devices because in the floating gate type, an electron was transferred from substrate to the floating gate and vice versa. This

phenomenon requires several scaling approaches in improving tunnel barrier materials while taking into accounts their thickness.

The tunnel barrier in a flash memory technology is also known as a dielectric. When a dielectric is placed in an electric field, electric changes shift slightly from their average equilibrium positions causing dielectric polarization (Misra, 2011). Conventional tunnel barrier with SiO_2 (silicon dioxide) was used as a medium for electron tunneling from substrate to floating gate layer and vice versa. An electron tunneling efficiency is crucial since it will determine the device speed during programming and deleting process.

1.4 Problem Statement

The most impressive phenomenon of this decade is manufacturing challenges of dielectric tunnel barrier in flash memory manufacturing, while to enhance the performance for flash memory technology. Current flash memory technology employed the conventional SiO_2 as the tunnel barrier material 5 nm of SiO_2 thickness presently posed as a minimum tunnel barrier thickness by the nonvolatile memory device technology. Less than 5 nm thickness of SiO_2, would results in many undesired effects such as Stress Induced Leakage Current (SILC) and direct tunneling, which further deteriorate the data retention performance (Park, 1998).

These issues can be summarized in the following way. First, the traditional tunnel barrier is fabricated with conventional method using SiO_2 of about 5 nm thickness as dielectric material. This typical uniform deposited barrier can maintain the electron tunnel through the barrier but with extended charge retention times. The extended times requires resulted in higher voltage or longer time needed during programming process. In another

word, if the tunnel barrier is relatively thick, higher voltage will be used in the programming process (Brown, 1997). As the barrier gets thinner due to demands of smaller devices, problem such as charge leakage will occur (Brown, 1997).

As a result, the net performance gain cannot be achieved by scaling down the conventional SiO_2 tunnel barrier less than 5 nm thickness. A new tunnel barrier system which overcomes this seesaw effect has to be developed.

1.3 Research Objective

The followings are the objectives of the investigation.

i. To focus on finding and developing the alternative tunnel oxide structure for NAND flash memory device.

ii. To relate the critical parameters during fabrication of the dielectric tunnel barriers and their effects on the performance of the NAND flash memory device.

iii. To analyze the characterization of the layered tunnel barrier which minimize the programming speed and data retention trade-off.

1.5 Research Scope

The research is carried out according to the following scopes:

i. Various tunnel barrier and their applications are studied. Literature reviews and the theoretical knowledge of tunnel barrier and its parameters were conducted to achieve basic understanding.

ii. Mask design using AutoCAD software is based on Fowler-Nordheim tunneling concept for NAND flash memory structure. The layout is required for mapping the fabrication of the tunnel barrier due to growing flash memory technology.

iii. The various critical modules in NAND flash memory structure were fabricated such as mask fabrication description, pattern transfer process and floating gate/ control gate deposition.

iv. Fabrication of various tunnel barriers is performed to investigate the effects of using the MOS capacitor model. The tunnel barrier with tunnel oxide and high-κ material was fabricated and performed under various parameters. These parameters needed for fabricate layered tunnel barrier. Optimal parameters are then finalized, and the device is re-fabricated using the MOS capacitor model. These processes were performed to simulate an effect of engineered tunnel barrier compared to the conventional ones.

v. Physical and electrical characterizations of tunnel barrier are performed. The results of the performance are then compared between the conventional and engineered tunnel barrier.

1.6 Thesis Organization

This thesis consists of five (5) chapters and this subchapter necessary a quick overview of what the thesis presents. **Chapter 1** describes the historical background, problem statement, objectives and scopes of the research work carried out.

Chapter 2 presents the relevant literature review of this research work which is divided to subtopics. They are the overview of memory device technology, design and manufacturing processes, tunnel barrier structure, materials and functionality. This chapter, will be discuss the concept was applied to the layered tunnel barrier and the factors to change the gate material and thickness.

Chapter 3 introduces the process module development of NAND flash memory cell. The developments of NAND flash memory cell require the fabrication of the tunnel barrier with EOT less than 10nm.This chapter also describes the NAND flash memory cell and mask design, dielectric materials optimization and physical characterization of the device. A viable solution for development a new tunnel barrier system according to the dielectric materials thickness measurement will be discussed**.**

Chapter 4 focuses on the development and characterization of conventional and engineered layered tunnel barrier using thermal furnace and dielectric analyzer. The conventional and engineered tunnel barrier is then compared from result programming current and programming voltage.

Lastly, **chapter 5** concludes the research findings and suggests ideas for new flash memory technology integration as future work.