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Taguchi Method for p-MOS Threshold Voltage Optimization with a Gate Length of 22nm

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ABSTRACT

This paper describes the virtual design of a 22nm gate length p-type metal oxide semiconductor, PMOS. Silvaco, TCAD tools were used to fabricate the device design and to characterize the device's electrical properties. Fixed field scaling rules are applied to obtain the transistor's electrical parameters set by ITRS 2013. In order to take the challenges that arise in the fabrication of nano-sized transistors and enhance their performance, advanced and novel technologies are applied. Using the statistical modelling of L9 Taguchi methodology, the development process is primarily focused on the tool's edge voltage. Four parameters have been divided into three distinct steps in order to conduct nine different experiments. The final confirmation result indicates that VTH is closer to the nominal value -0.206V following optimization techniques. This matches the ITRS 2013 requirements for high performance. This paper examines the design of a p-MOS double gate containing a layer of graphene as it is known to have a high mobility value.

Keywords: Taguchi, statistical, graphene, optimization, p-type

1. INTRODUCTION

The goal of this study is to virtually design a p-MOS device by optimizing the threshold voltage (V_{TH}) by applying the Taguchi L9 Orthogonal Array approach to discover the optimal combination of process parameters, with the contribution of nominal the best (NTB) of signal to noise ratio (SNR) analysis. The V_{TH} results will be assessed accordingly to the ITRS (International Technology Roadmap for Semiconductors) 2013 specification. Table 1 shows the scaling of the IC technology. It is a compilation of some history and some ITRS technology projections. The physical gate length, Lg, is smaller than the technology node.

Table 1 Scaling from 90 nm to 22 nm [1]

Year of production	2003	2005	2007	2010	2013
Technlogy node (nm)	90	65	45	32	22
Lg (nm) (HP/LSTP)	37/65	26/45	22/37	16/25	13/20
V_{DD} (V) (HP/LSTP)	1.2/1.2	1.1/1.1	1.0/1.1	1.0/1.0	0.9/0.9
EOT(nm) (HP/LSTP)	1.9/2.8	1.8/2.5	1.2/1.9	0.9/1.6	0.9/1.4
I_{on} HP (μA/μm)	1100	1210	1500	1820	2200
I_{off} HP (μA/μm)	0.15	0.34	0.61	0.84	0.37

High-performance (HP) = high-performance computer processor technology. LSTP = low standby-power products. (Eg. mobile phones)

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The threshold voltage is an important characteristic that distinguishes single and multigate CMOS technology. VTH is also important in process monitoring, circuit design, and statistical analysis in general, including the device to device's mismatch. Whether they explicitly designate a threshold voltage or not, small MOSFET models for circuit simulation must appropriately represent the CMOS technology that they describe.

The minimal voltage necessary to turn on the transistor is defined as the threshold voltage. The transistor might be NMOS or PMOS. The threshold voltage for n-MOS is positive, while the threshold voltage for p-MOS is negative. It is the lowest gate voltage in a transistor at which current conduction begins. The threshold voltage is the level of voltage at which the transistor switches on and the drain to source current (I_{DS}) begins to conduct. The voltage necessary to produce a strong inversion is known as the threshold voltage.

In this study, we construct and model a PMOS with 22nm double gate MOSFET, and also with a high-κ metal gate graphene structure. As a result, we present bilayer graphene for planar p-MOS as the most recent breakthrough to boost the flow of performance drivers. Graphene is an atomic layer having a very fast carrier motion ($2x10^5$ $cm^2V^{-1}s^{-1}$), high saturation velocity, high current density, and thermal conductivity [2]. Because of its superior qualities, single layer and bilayer graphene are used as channel. However, it was then constrained due to the defection of the energy gap. Bilayer graphene was then used, coupled with the usage of a high-κ/metal gate as the top gate to produce the bandgap and adjust the drain current [3]. High-κ dielectric materials have a higher dielectric constant (, kappa) than silicon dioxide. High-κ dielectrics are utilised in semiconductor manufacturing procedures to replace a silicon dioxide gate dielectric or another device's dielectric layer. Dielectric constants ranging from 40 to 86 have been reported in studies on TiO_2 thin films [4]. Compared to SiO_2, Al_2O_3, HfO_2, and ZrO_2, the TiO_2 dielectric has the highest dielectric permittivity. The effects of TiO_2 on a single metal-gate MOSFET's device characteristics as high-k gate layer and tungsten silicide (WSi_x) as a metal-gate layer have been studied in our previous works [5]. The suitability of a single WSi_x gate with the TiO_2 dielectric has been successfully reported to achieve results in a nominal V_{TH} value -0.206V and 100nA/um a low leakage current that satisfies the ITRS standards for a bulk single-gate device [5, 6]. WSix is utilised as a metal gate as a consequence of the metal gate work function engineering offered by Hong et al. in their patent due to its compatibility with both n-MOS and p-MOS devices [7]. Figure 1 shows the planar graphene high-κ transistor under study that contains TiO_2 dielectric to replace the silicon dielectric layer.

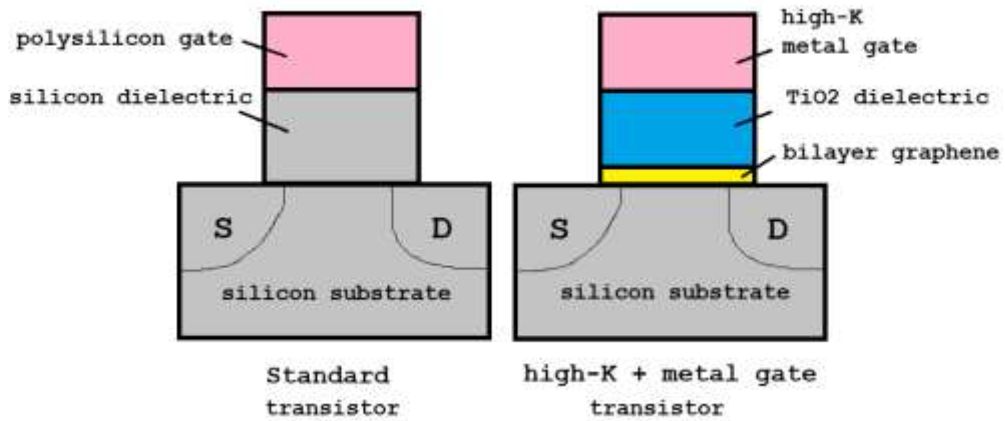

Figure 1. The design of high-κ metal gate transistor.

2. MATERIAL AND METHODS

The Silvaco ATHENA and ATLAS modules are an example of TCAD tool that has been used to investigate the downscaling process successfully. TCAD tools for semiconductors are a computer programme that enables the design, manufacturing, and simulation of semiconductor devices. These simulations allowed researchers to investigate the impact of various device settings on overall device performance [8]. Many hours of lab simulation effort are required to optimize these devices using TCAD software. Several features of each device were chosen for improvement. Dr. Genichi Taguchi invented the Taguchi approach, which has proven to be useful in a variety of technical domains [9].

The Taguchi method is based on a fundamentally different approach than traditional quality engineering approaches. The methodology focuses on incorporating quality into products and processes, as opposed to relying solely on inspection. Taguchi primarily used mathematical and statistical techniques, but he simplified the process by developing a set of standards for experiment design and analysis. The Taguchi experimental design methodology is appropriate for a wide range of applications involving a variety of variables [9]. Table 2 summarizes the device physical parameters. Figures 2 depict the finished layers material double gate device of the 22nm planar graphene p-MOS, respectively.

Table 2 Parameter design for double PMOS

Size and doping parameters	Set value
Gate length	22nm
Channel width	8nm
Source Drain doping	7.27×10^{14}
Channel doping	1.13×10^{11}
Gate to Source/Drain gap	1nm
Voltage threshold ITRS	-0.206V
Voltage threshold optimization	-0.20744V

For threshold voltage adjustment, the implant of phosphor dose was used in this design, and the source-drain implant used a boron dose. Table 3 shows the coding programming for this implanted dose.

Table 3 Implantation threshold voltage and source-drain

```
######################################################################
# Threshold voltage adjust implant
moments std_tables
implant phosphor dose=2.6e12 energy=17 tilt=60 rotation=30 crystal
implant phosphor dose=2.6e12 energy=17 tilt=60 rotation=120 crystal
implant phosphor dose=2.6e12 energy=17 tilt=60 rotation=2158crystal
implant phosphor dose=2.6e12 energy=17 tilt=60 rotation=300 crystal

# Source/drain implant
implant boron dose=7.4e15 energy=39 tilt=13 rotation=60 crystal
######################################################################
```

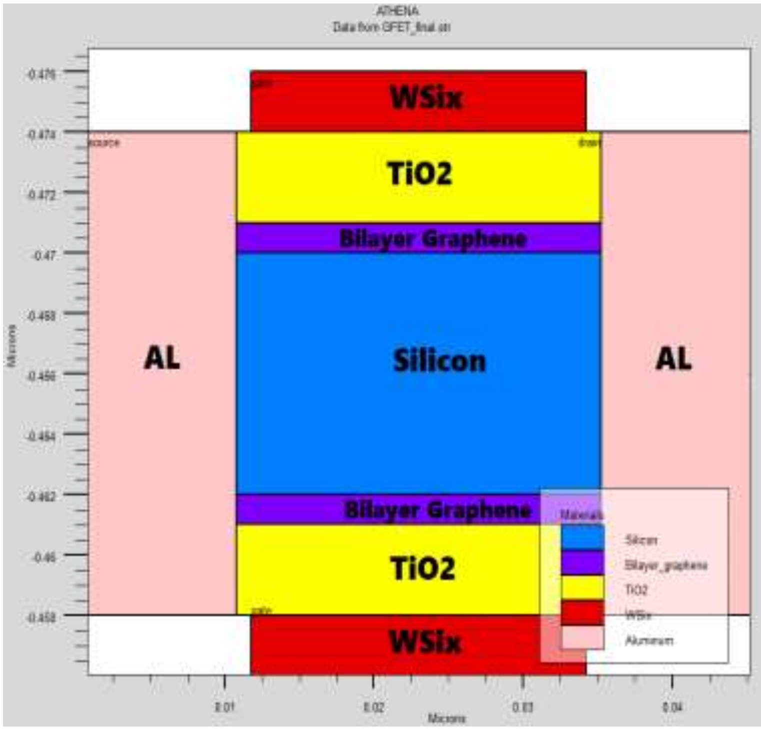

Figure 2. The p-MOS double gate device.

Figure 3 clearly shows the drain current versus drain voltage (V_{ID}). After finishing the design, the device structure, it was then used to simulate electrical characteristic performance, which was tested with the ATLAS module. Figure 4 shows the voltage threshold achieved the nominal target ITRS value ±12.7% of 0.206V.

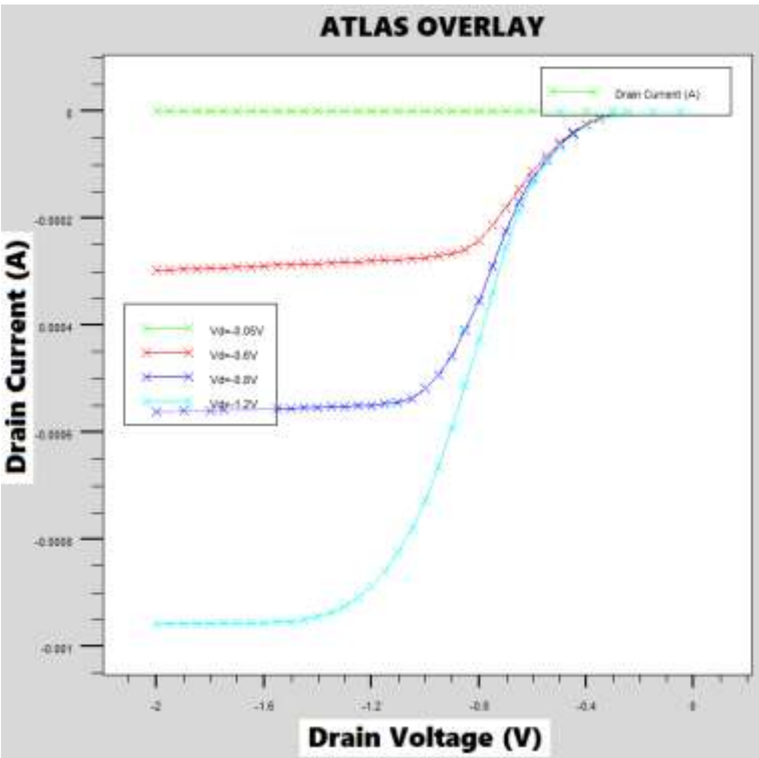

Figure 3. ID-VD graph ATLAS.

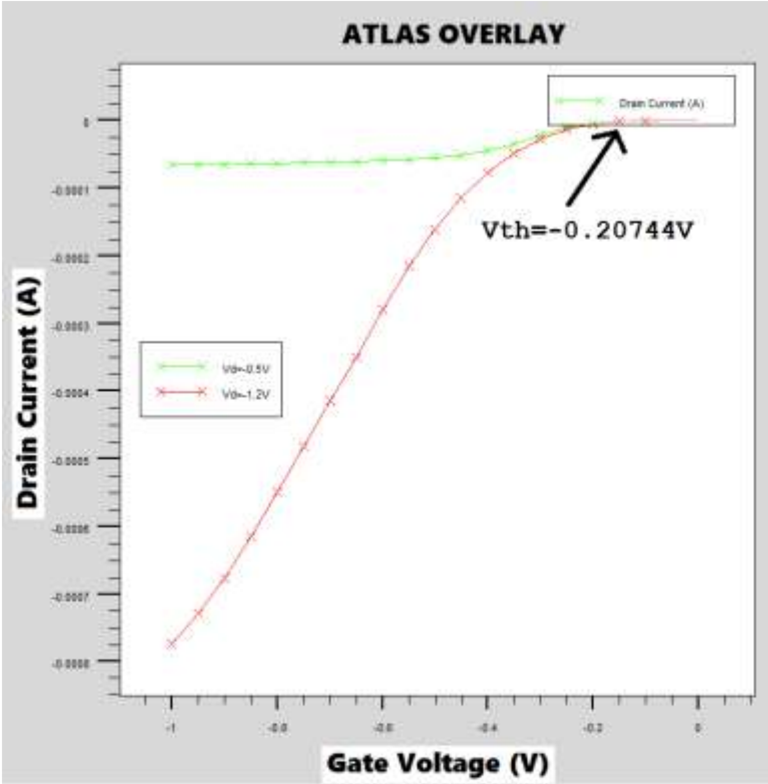

Figure 4. The ID-VG graph ATLAS.

3. RESULTS AND DISCUSSION

In this analysis, there were 3 stages involved such as designing, extraction of electrical characteristics and optimization of process parameters. For the designing stage, the Athena module was used while for the extraction stage, the Atlas module was used to extract the electrical parameters [10]. The Taguchi's L9 orthogonal array approach was employed for optimization. Based on Table 4, there are four selected process parameters and their level. The 4 process parameters that have been selected are S/D implant energy, S/D implant tilt, voltage threshold adjust implant energy and voltage threshold implant tilt. Table 5 shows the noise factors are S/D implant dose and voltage threshold adjust implant dose.

Table 4 Process parameter

Symbol	Parameter Process	Unit	Level1	Level2	Level3
A	S/D Implant Energy	keV	39	40	41
B	S/D Implant tilt	degree	11	12	13
C	VT Adjust Implant Energy	keV	17	19	21
D	VT Adjust Implant tilt	degree	60	62	64

Table 5 Noise factors

Symbol	Noise factor	Unit	Level1	Level2
X	S/D Implant dose	atom/cm^{-3}	7.40E+15	7.50E+15
Y	VT Adjust Implant dose	atom/cm^{-3}	2.50E+12	2.60E+12

A total of 36 simulations of the Taguchi method's L9 Orthogonal Array was used to maximize the V_{TH} values utilizing control variables. V_{TH} is a nominal-the-best quality characteristic in this study. V_{TH}'s preliminary findings were listed in Table 6 correspondingly.

Table 6 The threshold voltage experiments value

Experiment number	Threshold voltage , V			
	Vth1	**Vth2**	**Vth3**	**Vth4**
1	-0.216001	-0.21486	-0.22015	-0.220478
2	-0.223799	-0.223235	-0.226774	-0.226213
3	-0.230036	-0.229556	-0.23304	-0.232562
4	-0.199266	-0.198382	-0.20441	-0.203514
5	-0.206826	-0.205937	-0.212171	-0.21127
6	-0.209863	-0.208785	-0.21535	-0.214258
7	-0.180637	-0.179843	-0.185285	-0.184479
8	-0.183555	-0.182612	-0.188329	-0.187372
9	-0.190693	-0.189742	-0.195661	-0.194696

Table 7 shows the factor effect of the SNR and mean by ANOVA analysis. The S/D implant energy component, which scored the highest on the S/N ratio with a 72 percent contribution, was chosen as the dominant component based on the results of the ANOVA for V_{TH}. According to these analyses, the major factor affecting the V_{TH} is S/D Implant Energy (Factor A) with 72% whereas the second ranking factor was VT adjusts implant tilt (Factor D) which is 11%. The percentage factor influence on SNR reveals a factor's proportionate ability to reduce variation. A minor deviation will have a large impact on performance for a factor with a high percent contribution [11]. Based on ANOVA result, it clearly can be defined that, S/D implant tilt (Factor B) as since it is an adjustment factor; the variance has a tiny 7% influence, while the mean has a huge effect 90%.

Table 7 The factor effect

Control factors	DOF	Sum of Squares	Mean Square	F value	Factor Effect (%)	
					S/N ratio	**Mean**
A	2	37	18	36	72	8
B	2	4	2	4	7	90
C	2	5	3	5	10	1
D	2	5	2	5	11	1

The average performance analysis revealed that the Taguchi method's optimal levels of process parameters are A2C1D1. Table 8 shows the selected best value for running the final results of the threshold voltage. Because Factor B was found as an adjustment factor in V_{TH}, it may be set to any level. [12]. The whole optimization recommendation is A2B3C1D1.

Table 8 The best value for process factor

Symbol	Process Factor	Value
A	S/D Implant Energy	40 keV
B	S/D Implant tilt	13 degree
C	VT Adjust Implant Energy	17 keV
D	VT Adjust Implant tilt	60 degree

Table 9 shows the final confirmation result have done. The mean for V_{TH} after optimization approaches is -0.20744V. This result is still within a 12.7% range of the nominal goal value,-0.206V [13]. The number is also more in line with the ITRS. This proves that this approach can identify the best solution in finding the gate length of 22nm for p-channel double gate device with an appropriate threshold voltage value.

Table 9 Final results of the device threshold voltage

Threshold voltage (V)				SNR Mean	SNR Nominal the best
Vth1	**Vth2**	**Vth3**	**Vth4**		
-0.208565	-0.20744	-0.214035	-0.212894	-13.5	36.3

4. CONCLUSION

Finally, the device of a 22nm p-MOS design was successfully optimized. When a greater permittivity of high-K dielectrics is used as the gate insulator, the I_{ON} value is when a greater high-K dielectric permittivity is used, boron penetration is observed to raise leading to a decrease in depletion since there is less boron penetration. Table 10 shows the result after the optimization of the device. The subthreshold swing (SS) was also calculated from the subthreshold ID-VG curve using Kaharudin et al. [14]. This parameter was an important quality in MOSFET technology since it indicated a device's switching speed. At normal temperatures, the theoretical limit of SS in a MOSFET is 60 mV/dec [13]. A smaller SS, on the other hand, is preferable. Figure 5 shown the derived SS value from the curves was 93mV/dec.

Table 10 The result after optimization best value

Electrical responses	Results from this works	ITRS 2013 Prediction
Vth (V)	-0.20744	±12.7% of -0.206V
I_{ON} (μA/μm)	1784	≥ 1469
SS (mV/dec)	93	60
Ioff	95nA	100nA

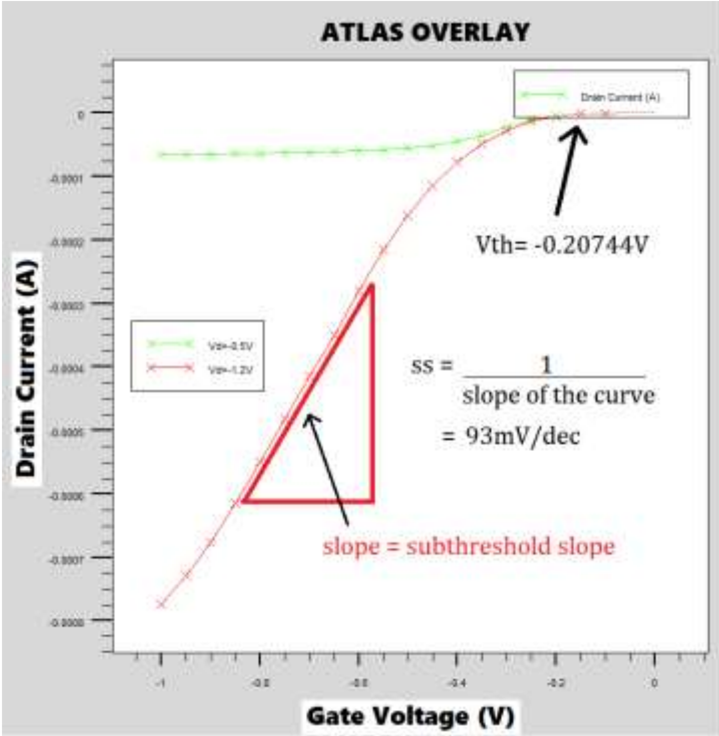

Figure 5. The subthreshold swing curve.

The orthogonal array L9 Taguchi approach was done to examine and optimize the device's V_{TH}. The threshold voltage is one of the most important parameters in influencing the performance and applicability of nano scaled devices [15]. The final process parameter combination of A2, B3, C1, D1, X1, and Y1 produced an optimum value threshold voltage of -0.20744V, which is still within the ITRS prediction of -0.206V [13].

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