An excellent gain flatness 3.0-7.0 GHz CMOS PA for UWB applications

Abstract

This letter presents an excellent gain flatness CMOS power amplifier (PA) for UWB applications at 3.0-7.0 GHz in TSMC 0.18 μ m CMOS technology. The UWB PA proposed here employs a current-reused technique to enhance the gain at the upper end of the desired band, a shunt and a series peaking inductors with a resistive feedback at the second stage to obtain the wider and flat gain, while shunt-shunt feedback helps to enhance the bandwidth and improve the output wideband matching. The measurement results indicated that the input return loss S₁₁ less than -6 dB, output return loss S₂₂ less than -7 dB, and excellent gain flatness approximately 14.5 ±0.5 dB over the frequency range of interest. The output 1 dB compression of 7 dBm, the output third-order intercept point (OIP3) of 18 dBm, and a phase linearity property (group delay) of ± 178.5 ps across the whole band were obtained with a power consumption of 24 mW.