International Journal of Nanoelectronics and Materials
Volume 15, No. 3, July 2022 [189-196]

Fabrication of Carbon Nanotube Field-Effect Transistor Using Shadow Mask Technique

Ankita Dixit, Navneet Gupta** and Suraj Baloda

Department of Electrical and Electronics Engineering
Birla Institute of Technology and Science, Pilani
Rajasthan, India

ABSTRACT

In this work, a new approach based on shadow mask has been reported for fabricating low-cost carbon nanotube field-effect transistor (CNFET) with interdigitated source and drain electrodes. The drop cast method is used for depositing CNTs, which was characterized using Field Emission Scanning Electron Microscope (FESEM) and RAMAN spectroscopy. The RAMAN spectroscopy confirms the deposition of CNT and SEM images demonstrated the deposition of CNT network on dielectric layer without using O_2 plasma etching. Further, Keithley 4200 SCS parameter analyzer was used to perform the electrical characterization of the fabricated device. The results indicated that the fabricated CNFET follow the trend of p-type multichannel CNFET.

Keywords: CNT, Interdigitated electrode, Multichannel Carbon Nanotube Field Effect Transistor, Shadow Mask Technique

1. INTRODUCTION

The next generation of electronics devices are blooming with carbon nano-materials. Among the carbon allotropes (graphite, diamond, fullerene, graphene and carbon nanotube), single wall carbon nanotubes (SWCNTs) evolve as most promising material as it has marvellous physical, electrical, thermal and mechanical properties [1-3]. The SWCNTs can be either semiconducting or metallic in nature which depends on chiral vectors ($\vec{n}$, $\vec{m}$). If the difference of chiral vectors is an integer multiple of three, CNT is metallic otherwise semiconducting in nature [4].

Many researchers have fabricated transistor based on SWCNTs as a channel and have shown the possibility of using it as an alternate of silicon in field effect transistors [5]. For fabricating the transistor, CNT can be deposited/grown on substrate using various methods, including; chemical vapour deposition (CVD), spray coating, spin coating, drop cast and Langmuir-Blodgett (LB) technique [6-11]. However, each of them has its own advantages and limitations.

The CVD method provides high quality of thin films with controllable diameter of CNT but the use of suitable substrate and catalyst, high pressure and temperature limits this process [12]. The spray coating is a chaotic method, which requires high pressure and temperature. In this method, as the molten particles strike on the substrate, they spread and splat the surface [13]. LB technique has potential to produce a smooth thin film without harming the surface. This process does not require high pressure and temperature but the use of smooth surface of substrate and slow deposition limits this process [14]. Although the drop cast deposition also does not require high pressure and temperature, it is an economical and a simple technique [15]. A suspension solution of CNT has been used for drop casting. The SWCNT have been solubilized in water, fluorine or alkanes [16]. In both of these cases, the properties of SWCNTs have been modified. In order to avoid the unwanted modification in the characteristics of SWCNTs, a desirable solvent is

*Corresponding author: ngupta@pilani.bits-pilani.ac.in

necessary. The reported solvents for the suspension solution of CNT are N-methyl pyrrolidone (NMP), Dimethylformamide (DMF), Hexamethylphosphoramide, Cyclopentanone, Tetraethylene sulfoxide and e-caprolactone [17-18]. In these solvents, NMP is the best suitable solution for the CNT [17], [19].

Since the first CNFET was fabricated, quit a few methods have been developed for the fabrication of CNFET. R. Martel *et al.* fabricated CNFETs using single wall and multiwall CNTs and analysed that multiwall CNTs (MWCNTs) have been unaffected by gate voltage [20]. K. C. Narasimhamurthy *et al.* presented n-type and p-type CNFET. They reported photolithography process for the fabrication of CNFET using O_2 plasma etching [21]. K. Maehashi *et al.* fabricated CNFET device using reactive ion etching (RIE) and electron-beam (EB) lithography [22]. The etchant used also effects the thickness of dielectric layer. Shadow mask process [23] is a chemical free technique that eliminate the intermediate steps as deposition and etching of photoresist (PR). The shadow masks process is ideal which eliminates multiple processing steps and is cost and time effective. Before depositing CNT, the dielectric layer of wafer was treated with O_2 plasma to improve the adhesion of CNT, which effects the thickness of dielectric layer [24]. This limitation is overcome using unpolished wafer surface. Silicon dioxide (SiO_2) has been used as dielectric layer that provides better isolation between gate and channel. There are many other dielectric materials such as Alumina (Al_2O_3), Hafnium Oxide (HfO_2), Hafnium Silicate ($HfSiO_4$), Lanthanum Oxide (La_2O_3), Silicon Nitride (Si_3N_4), Yttrium Oxide (Y_2O_3) and Zirconia (ZrO_2) [25-26] reported to be used in CNFET; however, SiO_2 layer can be grown easily on Silicon (Si) layer by oxidation. In this work, a cost-effective shadow mask technique is used to verify CNT as a channel for FET devices. Figure 1 illustrates the process flow used to study the CNFET device.

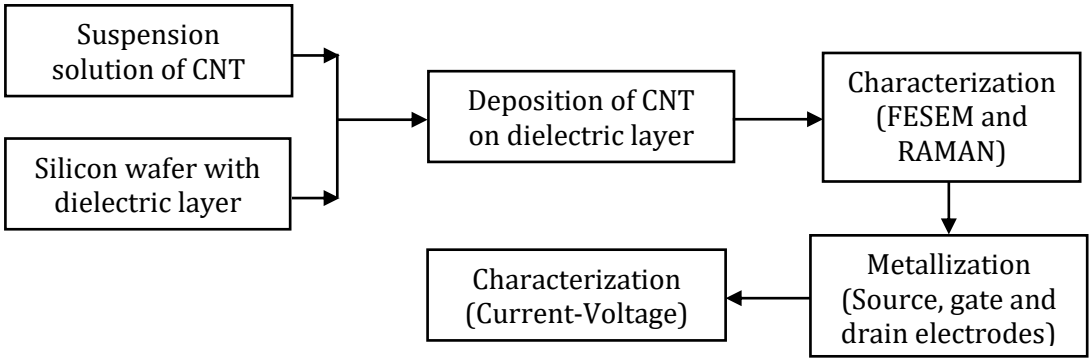

Figure 1. Process flow for CNFET

2. EXPERIMENTAL DETAILS

High purity (>99%) semiconducting SWCNTs with the chirality (7, 6) and average diameter of 0.83 nm were used for the fabrication of device. As shown in Figure 2, the SWCNT powder was ultrasonically dispersed in N-methyl pyrrolidone (NMP) solution. Semiconducting SWCNT powder of 0.6 mg was added into 60 ml of NMP solution and sonicated for two hours at 40 kHz with 100 W power. This provides the suspension solution of CNT.

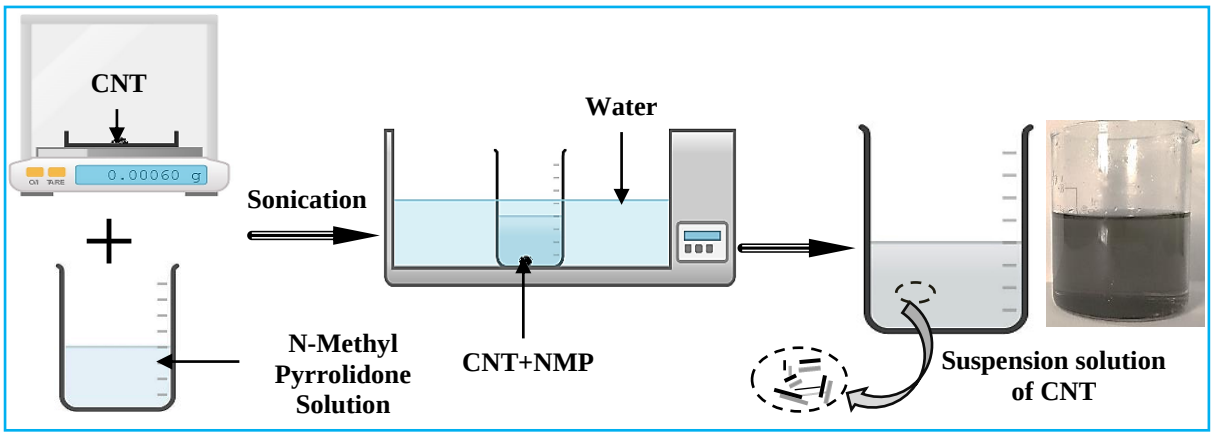

Figure 2. Pictorial representation of the formation of suspension solution of CNT with N-methyl pyrrolidone (NMP)

2.1. Device Fabrication

Figure 3 shows the flow-chart for the fabrication of planar CNFET. 2-inch n-type silicon (Si) wafer having the crystal orientation of <100> was used as the substrate for the device. The dry thermal oxidation at 900̊ C for 25 minutes was done to grow the silicon di-oxide (SiO_2) layer with targeted thickness of ~5 nm on Si substrate on both sides. After that, front side of wafer was coated with s-1813 positive photoresist (PR) and substrate is dipped into Buffered Oxide Etchant (BOE) solution to remove the oxide layer from backside. The drops of the SWCNT-NMP solution were cast on the SiO_2 layer of wafer by using adjustable pipette of 10-100 µL. The volume of the drop was low, so the duration of drying process to remove NMP was 5 minutes. This substrate was dried at 100̊ C to remove NMP. A bilayer of chromium (Cr) and Gold (Au) of thickness (Cr/Au- 2 nm/10 nm) was deposited on the backside of wafer using sputtering to fabricate the back gate of FET device. In the last step of the fabrication for back gate CNFET, the deposition of source and drain with Cr/Au (~10 nm/50 nm thick) was done by using a shadow mask with interdigitated electrode. The shadow mask technique (SMT) based all active sensor elements has a minimum feature size of ~0.5 mm [23]. So, the channel length of 0.7 mm has been selected, which is close to minimum feature size. The maximum distance between source and drain electrodes is 3.5 mm. The change in the channel length from 0.7 mm to 3.5 mm shows a significant change in the drain current.

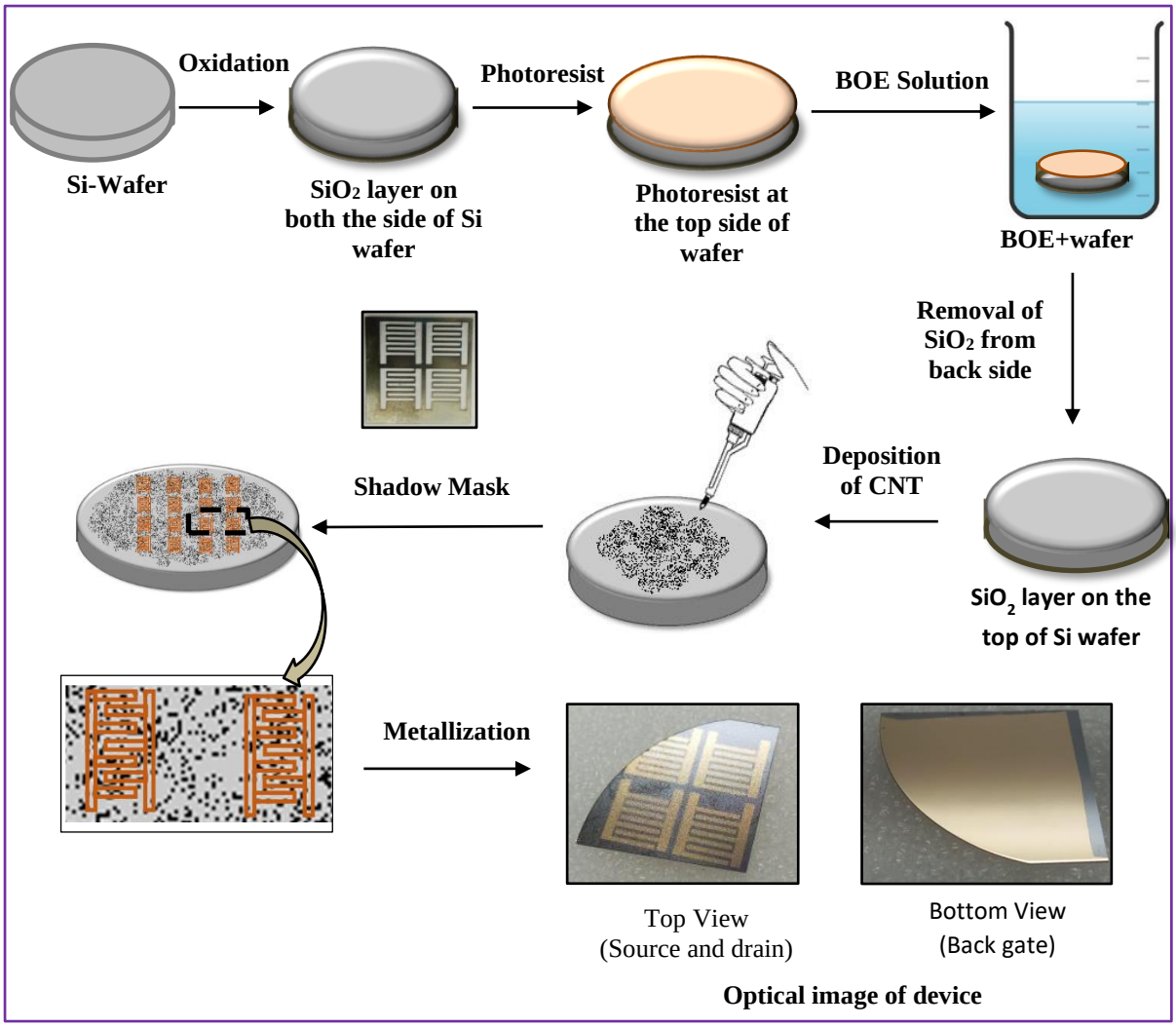

Figure 3. Steps used for fabricating the planar CNFET using shadow mask with interdigitated electrode

3. STRUCTURAL AND ELECRTICAL CHARACTERIZATION

Characterization technique is used to describe the physical and electrical properties of the device. The structural properties of device have been characterized using field emission scanning electron microscopy (FESEM) and RAMAN while the electrical properties have been explained using current-voltage characteristic.

3.1. Surface Morphology

The FESEM characterization gives the surface image and morphology of the sample. Figure 4 (a) shows the FESEM image of CNT. The interdigitated electrode (IDE) on CNT network was confirmed by using SEM characterization, as shown in Figure 4 (b). The inset of Figure 4 (b) shows the network of CNTs is present between source and drain electrode with gap of 0.5 mm.

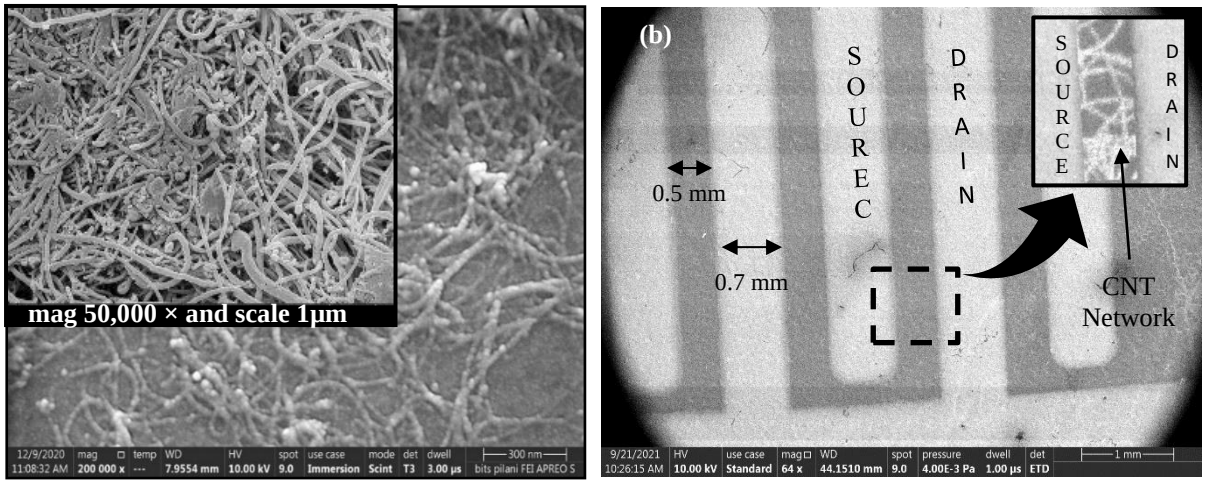

Figure 4. SEM image of (a) CNTs on SiO_2/Si wafer. The inset shows only CNT network (b) interdigitated electrode on CNT network. The inset shows CNTs network between source and drain

3.2. Raman Spectroscopy

The graph in Figure 5 shows Raman spectrum of SWCNTs. The Raman spectrum of SWCNTs exhibit four peaks; radial breathing mode (RBM) band (~265 cm^{-1}), D-band (1359 cm^{-1}), G^- (1573 cm^{-1}) band and G^+ (1592 cm^{-1}). The d-band has less intensity and blunt curve, which indicates that SWCNTs are highly pure. The G band splits into G+ and G- due to strain effect in SWCNTs. RBM mode confirms the presence of SWCNTs and Raman intensity defines the concentration of CNT. The Raman shift of this mode depends on the diameter of nanotube [26].

$$\omega_{rbm} = \frac{A}{d} + B \tag{1}$$

where ω_{rbm} is wave number, A is a constant of proportionality (A is 233±1.1 for LASER wavelength of 532nm [27]), d is diameter of CNT and B is interpreted which is related to the surrounding environment of nanotubes and it is expected to be zero for free standing isolated SWCNT [28].

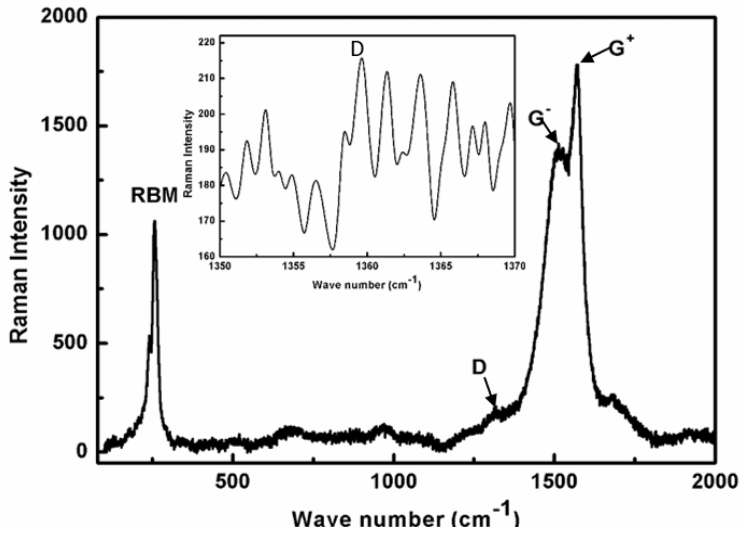

Figure 5. Raman spectra of Single wall Carbon Nanotubes

3.3. Electrical Characteristics

The electrical characteristics of device has been measured with the help of Keithley 4200 semiconductor parameter analyser. Output and transfer characteristics depend on the number of SWCNT channels. The output characteristics of the device is shown in Figure 6 (a). CNT network

represents the control of drain current (I_d) using drain to source voltages (V_{ds}) for a constant gate to source to gate voltages (V_{gs}). The drain current exhibits a linear dependency on V_{ds} up to about 5 V for V_{gs} of -6 V, -4.8 V, -3.6 V, -2.4 V, and then it approaches to the saturated value. As shown in the inset of Figure 6 (a), there is a considerable change in drain current. It is also observed that as the negative voltage increases, drain current also increases.
The transfer characteristics of CNFET is shown in Figure 6 (b) which exhibits the field control effect on drain current. It is observed that the drain current marginally decreases with increase in gate voltage. The transconductance of 1.8 μS at V_{ds} of 1.6 V and the inverse subthreshold slope of ~129 mV/dec has been achieved for fabricated multichannel CNFET.

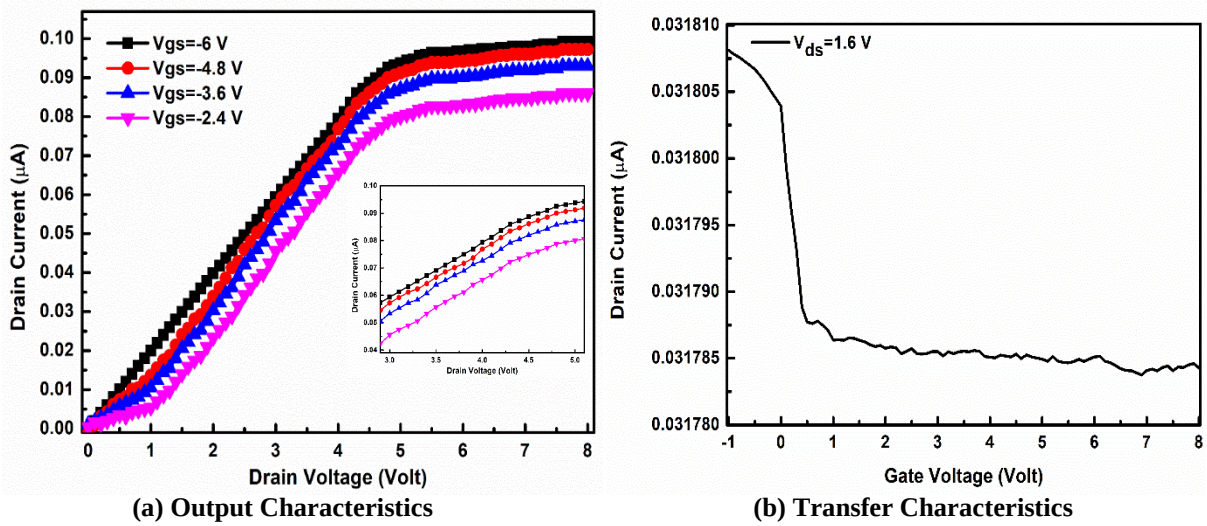

Figure 6. Electrical characteristics of CNFET (a) Output and (b) Transfer characteristics

The channel length between source and drain has substantial effect on the performance of the CNFET device. Figure 7 shows the output characteristics of CNFET for channel length (L_{ch}) of 0.7 mm and 3.5 mm. From the figure, it is clear that the drain current reduces when channel length increase [29-30], this is because small channel length provides less channel resistance.

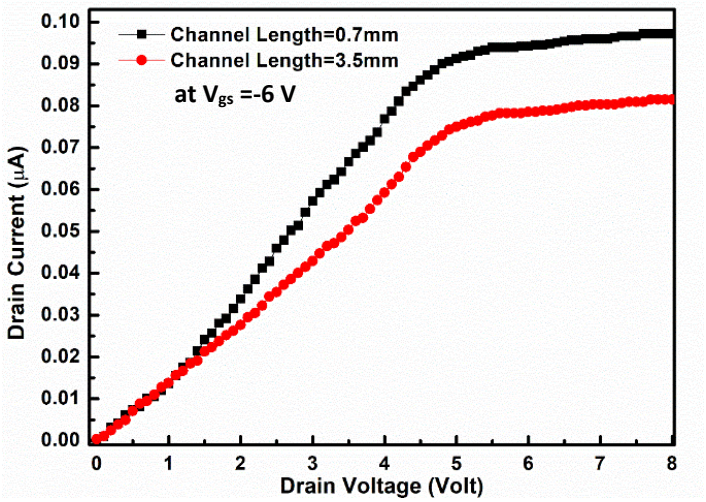

Figure 7. Output characteristics of CNFET with different channel length

The conductance of CNT channel between source and drain decreases with increase in the gate voltage. These characteristics follow the same trend as reported for p-type multi-channel fabricated CNFET. This behaviour is similar to the experimental result reported by C. Chen *et. al* [31]. This confirms that the drop cast method for the deposition of CNT network on insulator

without oxygen plasma etching can also be used to fabricate a cost-effective planar CNFET with interdigitated electrode using shadow mask technique.

4. CONCLUSION

This paper presented the fabrication of planar CNFET using shadow mask technique which is one of the cost-effective methods for fabricating multi-channel CNFET. To fabricate the device, first a suspension solution of CNT is prepared and deposited on dielectric layer. For the fabrication of channel between source and drain in CNFET, CNTs were deposited without chemical process and O_2 plasma etching. After fabricating the complete device, characterization was done to analyse the performance of the device. The RAMAN characterization shows less defects in CNTs and the deposition of CNT network using drop cast process on dielectric layer has been confirmed by FESEM characterizations. Finally, the electrical characteristics is done to confirm the working of CNT as a channel. The I-V characteristics verifies that CNT works as a p-type channel between source and drain. The transconductance of 1.8 μS at V_{ds} of 1.6 V and the inverse subthreshold slope of ~129 mV/dec is obtained. This confirms that CNT can be used as a channel for FET devices and the proposed method can be used to fabricate a cost-effective CNFET with interdigitated electrode using shadow mask technique. In future, this device can be used for gas sensing application due to interdigitated electrodes.

ACKNOWLEDGEMENT

Authors would like to thank the financial support of Ministry of Human Resource Development (MHRD) project under SPARC scheme and acknowledge to Central Facility of BITS, Pilani for providing characteristics facilities to carry out the research work in this paper. We would also thanks to Dr. Sumitra Singh, Principal Scientist (CEERI, Pilani) for her technical support in performing the characterization of the device.

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