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Design and Electrical Simulation of a 22nm MOSFET with Graphene Bilayer Channel using Double High-κ Metal Gate

Izwanizam Yahaya[1], A. H. Afifah Maheran [1*] , F. Salehuddin[1] and K. E. Kaharudin[1]

[1]Micro & Nano Electronics Research Group (MiNE), Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Melaka, Malaysia

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ABSTRACT

This paper will discuss the virtual fabrication design process of a 22nm MOSFET bilayer graphene with high-κ *metal gate (HKMG). Silvaco software's TCAD fabrication tools were utilized, with the Athena simulation module used to construct the device design and the Atlas module used to describe the device's electrical characteristics. To get the electrical characterization of a transistor specified by international standards, fixed field scaling methods were employed. Advanced and new methods were used to reduce the problems that occur during the manufacture of nano-sized transistors while increasing their performance. The material is Titanium dioxide (TiO2), while the metal gate is Tungsten Silicide (WSi_X). The simulated devices conform to the International Technology Roadmap Semiconductor (ITRS) specifications. The results show that Vth is 0.206 ± 12.7% V for high performance (HP) logic technology requirements.*

Keywords: graphene, design, Silvaco, n-type, MOSFET

1. INTRODUCTION

With the development of current technology, the chip semiconductor design industry relies heavily on the development of smaller, compact, faster, and cheaper solution to provide better products for digital electronics needs [1]. Metal Oxide N-type semiconductor (NMOS) technology with high-κ material with metal gate has been extensively studied for outstanding device performance. Driving current (I_{ON}) is a best value reaction to determine the driving capacity of NMOS devices [2]. The objectives of this progress work are to design and simulate a 22nm double gate MOSFET with high-κ metal gate graphene structure. From here, the bilayer graphene for planar NMOS is introduced as the latest innovations with increment in the flow of performance drives.

Graphene is an atomic film with very high carrier motion (2×105 $cm^2V^{-1}s^{-1}$), high saturation velocity, high current density, and thermal conductivity [3]. A single layer and bilayer graphene are chosen as the channel because of the excellent properties. However, it was then restricted due to defection of energy gap. Bilayer graphene was then introduced along with the use of a high-κ/metal gate as the top gate to generate the bandgap and modulates the drain current [4].

Graphene serves as the organic thin film transistor (OTFT) channel material [5]. Graphene transparent conductive thin films have traditionally been used as the conducting channel layer for graphene-based field effect transistors (GFETs). The major promise for graphene in high-performance and low-power applications derives from the atomic attenuation that graphene-based devices can accomplish, resulting in near perfect channel potential control. Several studies have been conducted on OTFT stability. At room temperature, graphene has excellent electron

*Corresponding author: afifah@utem.edu.my

mobility, with reported values in excess of 15000 $cm^2V^1s^1$. The mobilities of holes and electrons are largely similar [6].

Besides that, the use of a double gate in this device will increase the amount of current delivered by the device while maintaining the same channel length, as well as offering better electrostatic control of the silicon layer, resulting in a decrease of short-channel effects (SCE). Because of its outstanding optical and electrical characteristics, titanium dioxide (TiO2) has been widely investigated in this respect.

In investigating TiO2 thin films, dielectric constants ranging from 40 to 86 have been found. TiO2 dielectric has the highest dielectric permittivity when compared to SiO_2, Al_2O_3, HfO_2, and ZrO_2. Several articles on the effects of TiO2 have been published [6].

The compatibility of a single WSix gate with the TiO2 dielectric has been successfully reported, resulting in a nominal V_{TH} value of 0.306V and a low leakage current of 0.258 nA/um, which meets the ITRS requirements for a bulk single-gate device [7, 8]. As a result of experiments metal's gate work function engineering, WSix is used as a metal gate [5].

1.1 High Performance

Table 1 shows the high performance for logic technology requirement issued by ITRS made by SIA (Semiconductor Industry Association) with Japan, Europe, Korea, and Taiwan.

Table 1 High performance ITRS 2012 requirement

No.	Characteristics	Value
1	Physical length (Lg)	22nm
2	Equivalent Oxide Thickness (EOT)	0.92nm
3	Saturation Threshold Voltage (V_{th})	0.206V
4	NMOS Drive current ($I_{d, sat}$) I_{ONN}	1469uA/um
5	Leakage current, ($I_{sd, leak}$) I_{OFF}	100nA/um

These requirements must be followed to comply with the design issued by the ITRS roadmap prediction for 22nm multigate design. One of the most dominant factors in determining the performance and application of nano scaled device is the threshold voltage [9]. For this study, the ITRS requirement is 0.206V.

A critical parameter is the device threshold voltage that determines the performance of the device. The value of the source to source (V_{DS}) voltage in which the number of mobile electrons accumulates sufficiently in the channel area until a conduit is formed is called the threshold voltage. During the device off state, leakage current (I_{OFF}) is monitored. It is the value of the drainage current (I_D) when no gate voltage (V_G) is employed. The process of scaling the device causes the drain area to be closer to the source, thus introducing the effect of short channels; as a result of this, the leakage current increases [10]. The characteristics of the transistor decrease significantly when the substrate temperature is raised to 80° and above during the deposition process. Key device performance parameters, such as field effect mobility, on/off ratio, threshold voltage and current are removed from standard procedures [11].

2. MATERIAL AND METHODS

2.1 Device structure and simulation

The Silvaco TCAD software was used to design the NMOS structure and related simulations were performed using ATHENA and ALTAS. Table 2 shows the dosage parameters of n-type fabrication

procedures. Ion implantation is a process where dopant is introduced to the silicon substrate using chemical materials such as boron, arsenic, indium, etc. [12]. These materials are ionized and accelerated to a large amount of energy to form a perfect silicon surface. The cross sectional views for the virtual manufacturing process phases are depicted in Figure 1. For the entire design, the procedure includes adding, etching, and mirroring.

Table 2 Fabrication procedure

Process Step NMOS parameters	
Substrate	Silicon <100> orientation
Threshold voltages adjust	1.01×10^{13} cm^{-3} Boron
Graphene layer	1nm Bilayer Graphene
High-K dielectric	3nm high-K Titanium dioxide (TiO_2)
Metal gate	22 nm Tungsten Silicide (WSi_X)
S/D implantation	1.1×10^{19} cm^{-3} Arsenic
Metal	1nm Aluminum

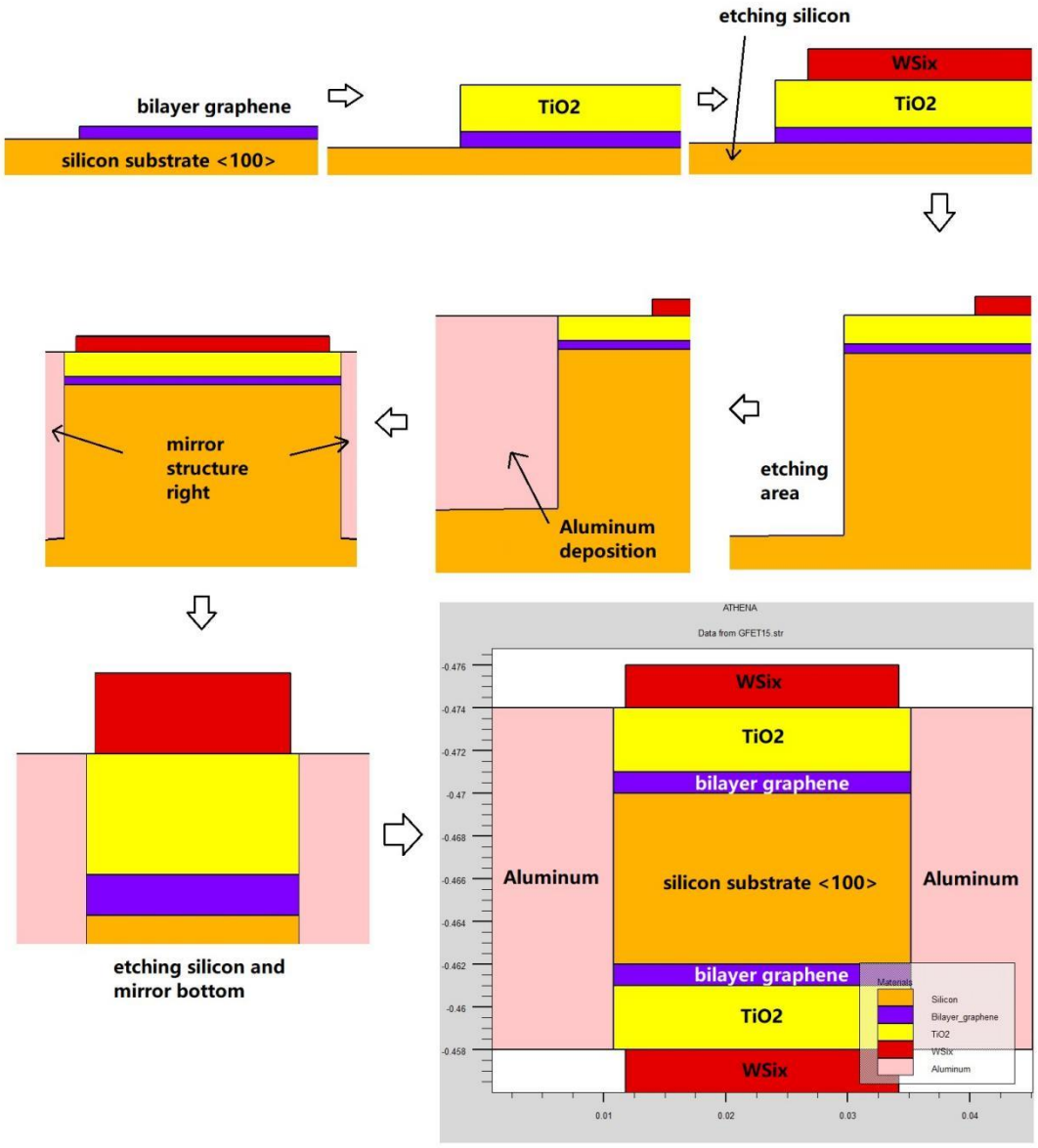

Figure 1. Cross-sectional views for fabrication process steps

The whole implantation process was tilted at various tilting angle to make sure that all sides of the device were implanted properly and hence, boosting the transistor performance. For threshold voltage adjustment, the implant concentration varies from 10^{12} atom/cm^{-3} to 10^{18} atom/cm^{-3} [14]. The threshold voltages adjustment of this device is 1.01×10^{13} cm^{-3} Boron to obtain the desired threshold voltage (Vth).

2.2 Design and optimization

To help design and optimize input process parameters consisting of two modules, ATHENA, and ATLAS, SILVACO Technology Computer Aided Design (TCAD) were used. For simulation processes in computer design, the module ATHENA was used. The ATLAS module, meanwhile, was used for system simulation and characterization. ATLAS has utilized a variety of physical and mathematical models to undertake analysis. The Shockley-Read Hall (SRH) model and the Lombardi model (CVT) are employed as physical models for the recombination mechanism and carrier mobility, respectively. For device simulations, the Newton and Gummel methods were used.

The gate length is 22nm for that device with a high-κ material. The replacement of SiO2 and poly silicon layers with high-κ and metal gate materials, respectively, is one of the main problems of further down scaling to keep planar MOSFET devices on track [15]. TiO2 material device has the superior electrical characteristics over others [16]. TiO2 has a diverse range of industrial applications [17]. For this design, the high-κ material, TiO2 was deposited at a thickness of 2 nm [18]. The compatibility of germanene materials based on semiconductor nanotechnology will make this material very attractive for device application purposes [19].

The development of a high dielectric combination of high permittivity gate high-κ and metal gate can solve the problem of gate leakage current [20]. Threshold voltage and the leakage current will be modulated by the transistor width, resulting in a significant narrow width effect. All these adverse effects will result in a reduction in threshold voltage then increased leakage current, especially on very small-scale devices [21].

3. RESULTS AND DISCUSSION

Figure 2 illustrates the basic design of a NMOS transistor. It consists of four terminal devices, a gate, a source, a drain, and a substrate or body. The NMOS device is made up of a p-type silicon wafer with two n+regions, the source, and the drain, while the PMOS transistor is made up of an n-type silicon substrate with two p+regions, the source and the drain. A thin oxide layer separates the gate electrode, which is doped by metal. A bilayer graphene was deposited doped after the silicon implantation into the device. Figure 2 also shows the graphene implementation material in designing MOSFET using high-κ metal-gate. The term high-κ dielectric refers to a material with a high dielectric constant K as compared to silicon dioxide. The implementation of high-κ gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components, colloquially referred to as extending Moore's Law.

The shift to new transistor technology is arduous, and delivery time frames for nano-sheet FETs differ, depending on the foundry. Samsung, for example, is producing a variety of technologies based on 7nm and 5nm FinFETs, with plans to debut 3nm nano sheets in 2022/2023. Meanwhile, IBS reports that Taiwan Semiconductor Manufacturing Company (TSMC) will grow FinFET to 3nm, but will transition to nanosheet FET at 2nm in 2024/2025. Intel and others are also working on nanosheets.

Throughout all generations of CMOS technology, silicon is the transistor channel material of choice up to 7nm nodes. TSMC's 5nm technology is the first advanced logic manufacturing approach to employ SiGe as the channel material in a p-type FinFET.

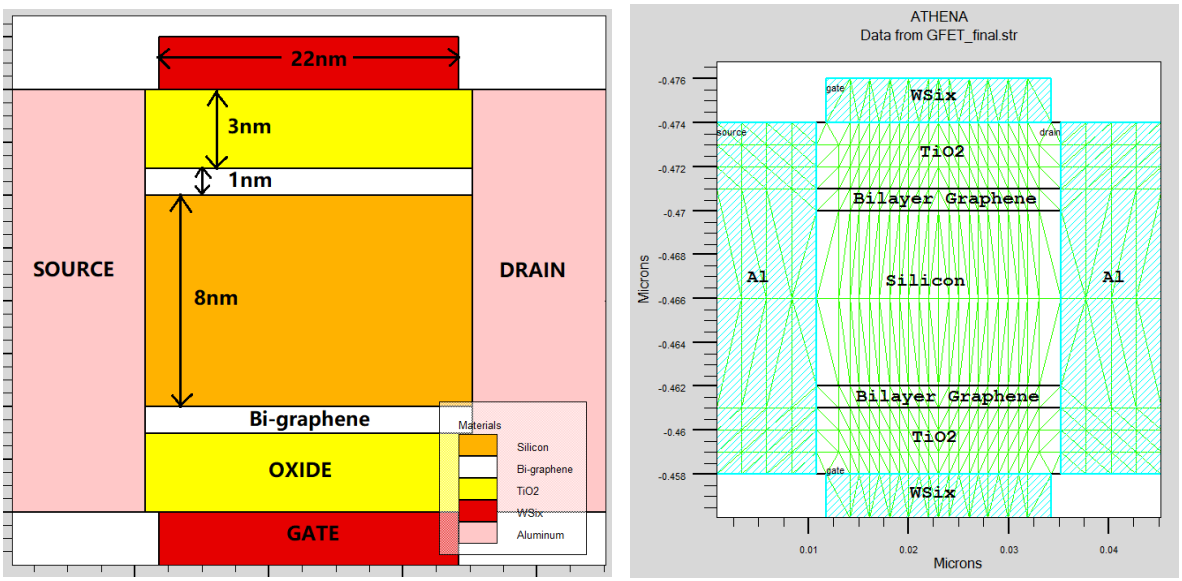

Figure 2. Cross section side-view of the 22nm length of n-channel Bi-GFET device

Silvaco TCAD tools' ATLAS module was used to perform electrical characterization of the 22nm n-channel Bi-GFET. The ATLAS script described the optical and electrical characteristics of bilayer graphene. The physical impacts of device structure are considered in the simulation process for this work. The entire project was performed at low temperatures, 300 K with a band gap of 0.55eV, permittivity of 2.4, electron mobility in an upper gate material, a radiative electron recombination rate, and holes with a time constant of 100 ns, and an effective field of Eeff = 0.4MV/cm2, whereas the electron and hole densities of the states were calculated using Equations (1) and (2) [22-23]:

$$Nc = \frac{8\pi meKT}{h^2} \ln 1 + (e^{-((ec - ef)/kT))}) \quad (1)$$

$$Nv = \frac{8\pi meKT}{h^2} \ln 1 + (e^{-((ef - ev)/kT))}) \quad (2)$$

The electron and hole masses of graphene have been set to me=0.06mo and mh=0.03mo, respectively, where mo is the free electron mass [24]. The coding material properties of bilayer graphene is as shown:

```
#Material bilayer graphene definition
material material=Bi-graphene=10000 mup=10000
material material=Bi-graphene permitivity=2.4
material material=Bi-graphene EG300=0.55
material material=Bi-grapheneEff=0.4M
material material=Bi-grapheneindex.file=Bi-graphene.nk
```

The design structure and doping profile is shown in Figure 3(a), where it displays contour, junctions, and electrodes for the design. It also shows the gate length measure perfectly at 22nm. To produce the characteristic curve of I_{DS} versus V_{GS}, a solution at each bias point and a solution at each phase point through the applied bias variable are obtained. For V_{GS} = 1.0V, a V_{DS} value is obtained. The output of this solution is stored in a log file. The log file is loaded for each drain bias, and the gate voltage is run in stages. V_{DD} drainage voltage is set at 0.5V while V_{GS} gate voltage is increased by 0.05V voltage step from 0V to 1V. Finally, an I_{DS}-V_{GS} curve is coated with Tonyplot, as shown in Figure 3(b).

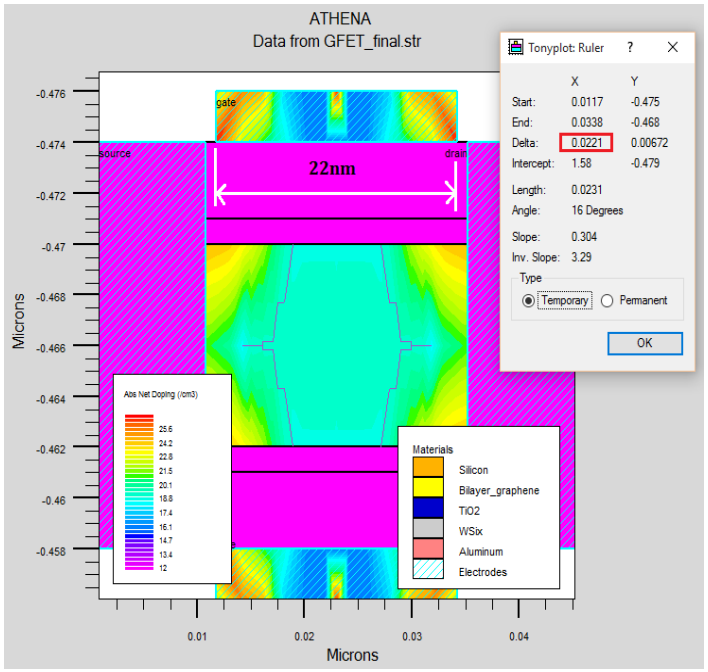

Figure 3. (a) Structure and doping profile

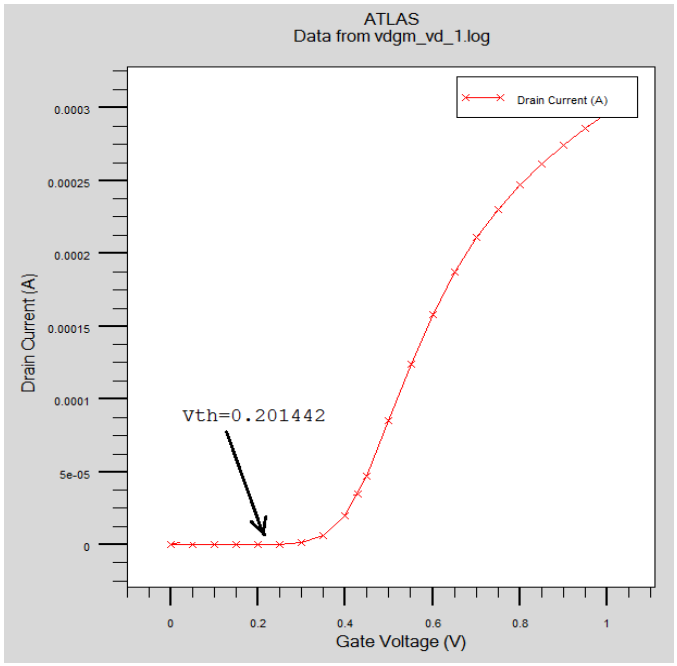

Figure 3. (b) Tonyplot I_{DS}-V_{GS}

It is important to determine the threshold voltage, V_{TH} of the gate voltage value when the transistor begins "ON" and to investigate the ratio of I_{ON}/I_{OFF} on/off current. When the I_{DS} is the minimum value, V_{TH} is extracted, where the point explicitly moves as the inversion point from the hole conductor to the electron conductor. We may also decide for V_{GS} trans conductivity is equal to zero, where when V_{DD} is equal to 0V, V_{TH} is removed when the gate voltage rises from 0V to 1.0V with a voltage step of 0.05V. Conditional transistor current, I_{OFF} is the conduction current when the gate voltage to the source is zero V_{GS} = 0V. There are several factors that can affect I_{OFF} such as V_{TH}, physical dimensions of doping channel, surface profile, drainage, source junction depth, oxide gate thickness and V_{DD}.

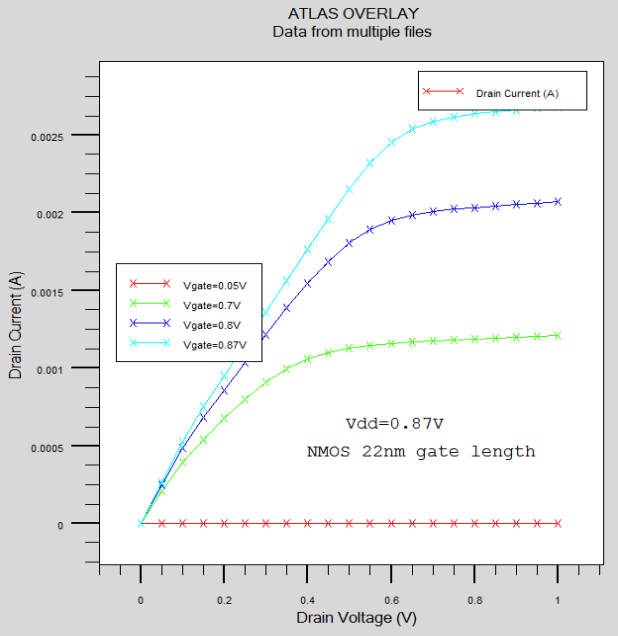

Figure 4. (a) Tonyplot I_{DS}-V_{DS}

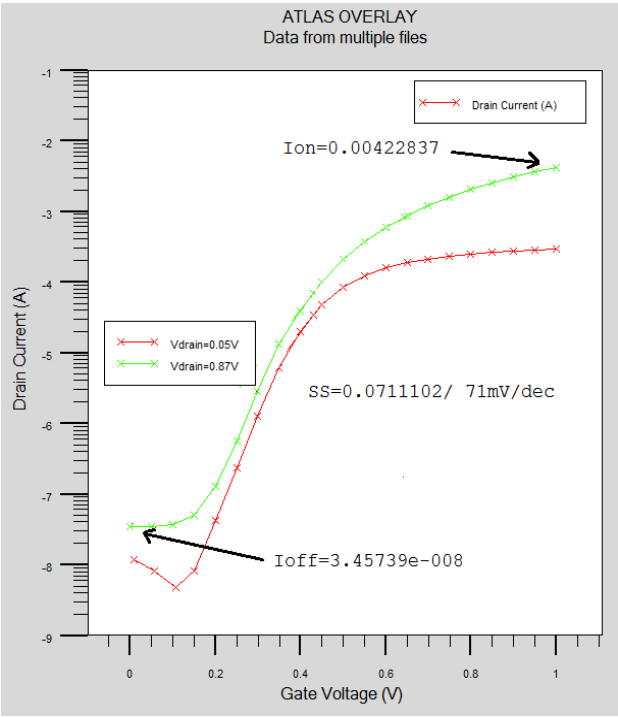

Figure 4. (b) The I_{ON}/I_{OFF} ratio

V_{TH} is 0.201V for V_{DD} = 0.87V. Figure 4(a) shows the graph of Tonyplot I_{DS}-V_{DS} simulation on the device. This DG MOSFET gate voltage is set within the range of 0.05 to 0.87V while the drain voltage is ramped by a voltage step of 0.05V from 0V to 1.0V. The ATLAS simulation characteristics given the value of drive current, leakage current and sub-threshold swing. All of these values were obtained from extraction device parameters as shown:

```
#Find Vt
method gummel newton
solve init

#Extract device parameters
extract name="Ion" max(abs(i."drain"))
extract name="SS" \1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
extract name="Vth"(xintercept(maxslope(curve(abs(v."gate"),abs(i."drain"))))-
abs(ave(v."drain"))/2.0)
extract name="Ioff" min(abs(i."drain"))
```

Figure 4(b) shows the I_{ON}/I_{OFF} ratio, which also shows that the external dopant profile on the outside of the bi-graphene channel can achieve a higher ratio of 1.22×10^5. The value of I_{OFF} must below than 100nA/um and I_{ON} value must over 1469uA/um.

4. CONCLUSION

The use of simulation software such as Silvaco TCAD is very useful in obtaining basic information on the performance of double-gate devices before undergoing actual fabrication. The design of a double gate high-κ metal gate with bilayer graphene transistor frame with a gate length of 22nm has been achieved. In this design, the best value of V_{TH} 0.201V, drive current 4228uA/um, leakage current 34nA/um and sub-threshold swing 71mV/dec within ITRS 2012 are required. The result describes the input process parameters for the minimum I_{OFF} in the double gate MOSFET device. Modeling input process characteristics allows for the optimization of specific design outputs. [11]. For further analysis, the Taguchi technique is a dependable approach for obtaining optimal solutions in the fabrication of nanoscale MOSFETs. V_{TH} is the primary response used to determine a device's level of functioning.

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