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Numerical Simulation and Characterization of Silicon Based OR Logic Gate Operation Using Self-Switching Device

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ABSTRACT

Logic gates are the main components inside the integrated circuit used for almost every technological application. Nowadays, in order to enhance the performance of the smart device, while targeting in cut down of the fabrication cost and achieve low power consumption, lithography-based VLSI design technology on silicon are still being widely applied. Hence, an OR gate structure, a silicon basedself-switching device (SSD) is introduced and investigated in this project. Such device is believed capable to act as an alternative for a low-powered logic gate application, suitable for CMOS devices. The SSD has an advantage in term of simplicity in fabrication process with a very low threshold voltage. Since SSD characteristics is similar to a conventional diode characteristic, the gate is designed in ATLAS Silvaco device simulator basedon a diode logic to perform OR logic function after a validation of the physical and materials parameters. The electrical characterization and structural analysis were also done to observe the electrical performance and physical condition in the device. The simulated design showed a good OR logic output response with the inputs, and acceptable output ranged from around 4.5 to 4.8 V with 5 V HIGH inputs. The results from this OR gate characterization may assist in developing the logic gate for device integration and may act as a reference for future complex integrated circuit design.

Keywords: OR gate, SSD, ATLAS Silvaco device simulator

1. INTRODUCTION

Logic gates are crucial components which are extensively used in computing applications in various devices and applications. It is not only applicable to electronics, but also widely researched using emerging technologies such as optical computing and DNA computing [1]. Often, logic circuits are interfaced and integrated with other devices, such that the electronic circuits control the behaviour of the other devices, thus higher scale integration of the components with other devices are recommended. In nowadays device fabrication, lithography-based VLSI design technology on silicon has been widelydeployed to minimize the cost of devices and is confronting critical challenges of designing ultra-low power consuming computational devices [2-4].

In this project, we proposed an OR gate structure by using a silicon based self-switching device (SSD) to provide an alternative for a low-powered logic gate application in nowadays CMOS devices. SSD is a rectifying device with a current-voltage (IV) characteristics similar to a diode (unipolar device)but without the use of any doping junction and barrier structure, which bring

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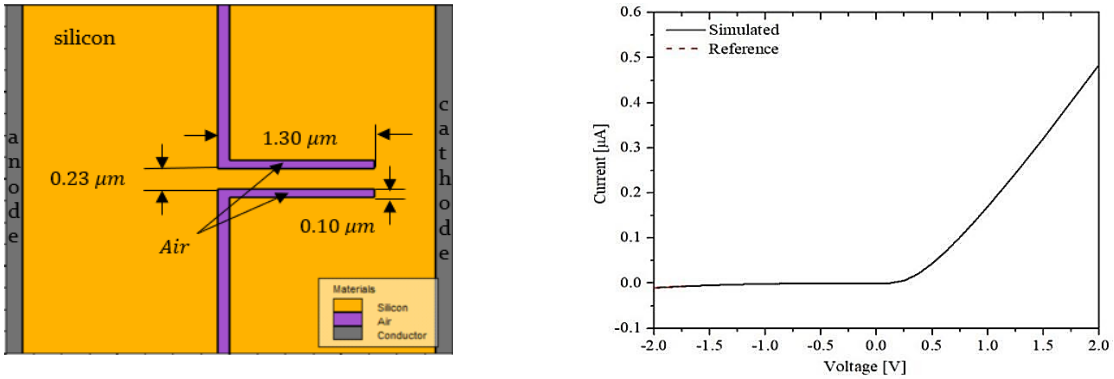
an advantage in term of fabrication simplicity where it only involves etching of the insulating trenches of a semiconductor surface to make an asymmetry channel [5]. The turn-on voltage of a silicon based SSD is reported at a very low bias of around 0.2 V compared to conventional diode with turn-on voltage at 0.7 V [6], and can be further lowered with manipulation of the structural length. Lower turn-on voltage in other substrates with higher electron mobility are also reported [7]. Implementation of a logic gate using SOI-SSD willhave the advantages in term of reducing the fabrication cost because of its fabrication simplicity, comply and easily integrated with nowadays technology, as well as providing a low-power consumption for the computing component.

The results from this OR gate characterization may assist in developing the logic gate for device integration in a fail-safes configuration, for shutting down or activating machinery features that protect them from damage in adverse working conditions and other related applications [8]. This project may as well be a reference and a basis for future complex design such as ternary logic gates and multi- operational logic gates using SSD.

2. METHODOLOGY

2.1 Device Parameters and Validation

The structure of SSD has been designed and simulated using ATLAS Silvaco device simulator. To validate the material parameters and the physics used in the simulator, we first simulated and comparedthe electrical characteristics result from the optimized SOI-based SSD structure from [9] as shown in Figure 1(a) with device parameters as stated in Table 1(Note that this optimized structure in [9] was designed after a validation process to experimental result of [7]). This step is crucial in order to achievea precise and accurate result.



(a) (b)

Figure 1. (a) Structure of optimized SOI-SSD and (b) IV characteristics comparison with reference from [7]

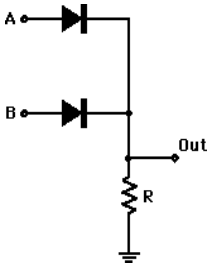
Table 1 Physical and device parameters for validation

Factors	Parameter values
Material	Silicon
Top layer thickness	205 nm
Type of substrate	p-type
Carrier density	2.45×10^{16} cm^{-3}
Mobility	400 cm^2/Vs
Temperature	300 K
Interface charge	3.16×10^{11} cm^{-2}
Anode input range	0 – 5 V

The channel length, L, channel width, W and trench width, Wt was 1.30 μm, 0.23 μm, and 0.10 μm, respectively. The substrate is silicon (orange in colour), the gray colour region is the electrode with anode at the left and cathode at the right side with the L-shaped etched region (air) shown in purple colour. This asymmetrical insulated region creates a conduction channel in the middle of the device[10]. The physical and device parameters are as shown in Table 1. As can be seen in Figure 1(b), the IV characteristics of the simulated device from -2 V to +2 V are similar to the reference structure, which validated the physical and material parameters used in the simulator.

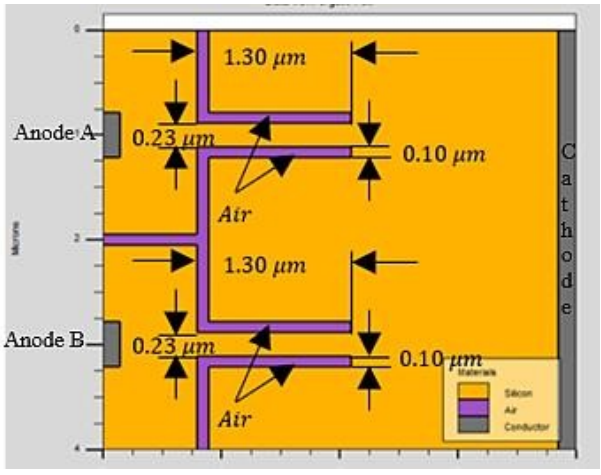
2.2 OR Logic Gate Design

The OR logic gate was designed by implementing the validated structure of optimized SOI-SSD, based on the diode logic circuit schematic and output as shown in Figure 2(a). Two SSDs were designed in parallel with an etch separator junction between two anode inputs; A and B [see Figure 2(b)]. By doing this, theconduction of holes from the inputs are forced to go through the channel in forward bias, and are closedin negative or zero bias because of the depletion region in the channel. Characterization on the OR gate SSD has been done in term of IV analysis, potential and current distribution to examine the output response, and the condition inside the device with different inputs.



Input A	Input B	Out
0	0	0
0	1	1
1	0	1
1	1	1

(a)



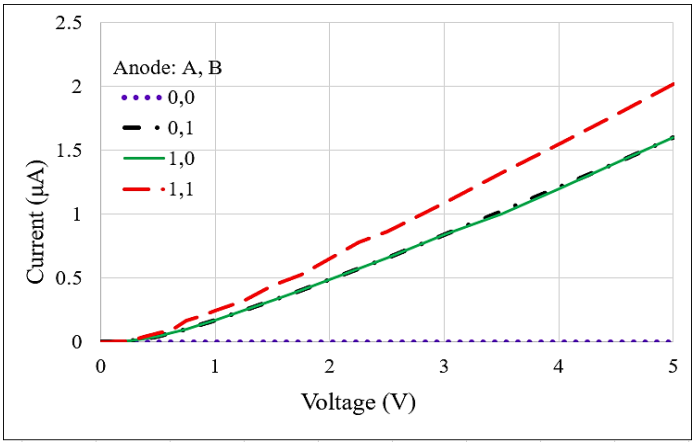
(b)

Figure 2. (a) OR gate diode logic schematic and its truth table, and (b) the designstructure of OR gate SOI-SSD

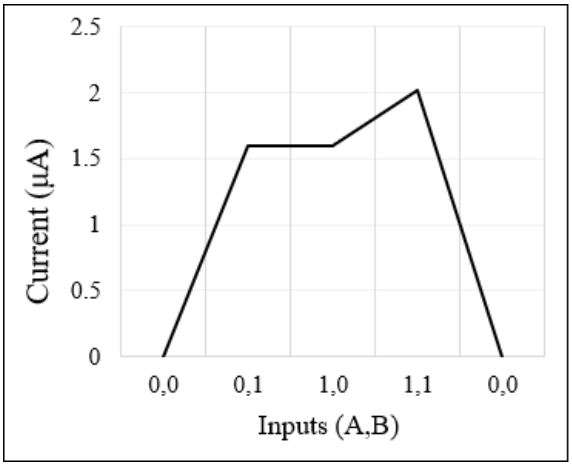
3. RESULTS AND DISCUSSION

3.1 Electrical characteristics and Potential Distributions

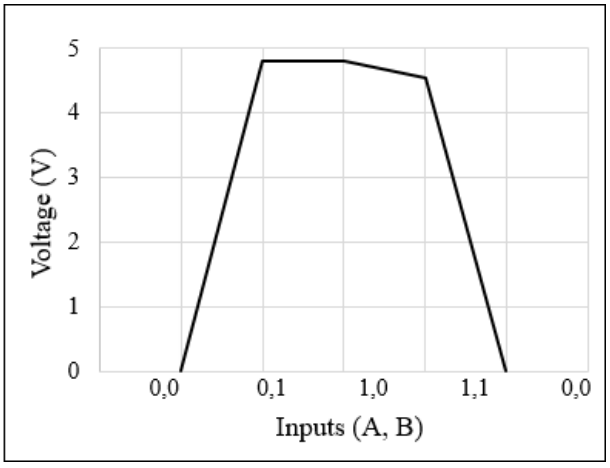
Figure 3(a) showed the IV characteristic of the simulated SOI-SSD OR gate with different inputs value in the anodes; A and B with biasing value of 0 V (LOW) to 5 V (HIGH) and the response is pictured in Figure 3(b). The value of 5 V is chosen to represent the HIGH condition as most of electronic applications implement the voltage in this range [11]. As can be seen, when both inputs are low (A,B = 0,0), the output current showed 0 A (LOW). Figure 4 shows the electrical potential distribution with different inputs value of Anode A and B. As can be seen in Figure 4(a), the potential distribution in the device and across the channel is very low when A,B = 0,0 which explained the low output current value in Figure 3(a). The barrier height is also the highest at around 0.3 V [see Figure 5(a)] where holes are not allowed to moves to the right side of the device.



(a)



(b)



(c)

Figure 3. (a) IV characteristics of OR gate, (b) output current, and (c) output voltage in different inputs conditions.

When either one of the inputs is high; A,B = 0,1 or 1,0 as shown in Figures 4(b) and 4(c) (5 V distribution in red, and 0 V distribution in blue), the output current started to increases with forward current, I_F of 1.6 μA at 5 V bias with very low threshold voltage, V_{TH} at around 0.2 V [see Figure 3(a)]. Assuming the output condition following the Ohm's Law, the calculated output voltage is around 4.8 V as shown in the inset of Figure 3(b).

When both inputs are high; A,B = 1,1 as shown in Figure 4(d), the output current increased to a higher I_F value of 2.02 µA [Figure 3(a)]. With both inputs HIGH, the series resistances of both anodes A and B are now in a parallel configuration, with addition of another series resistance at the output whichresulted in reduced equivalent resistances to 2.25 MΩ. This decreased in the equivalent resistance resulted in an increase of the output current value, and contributed to a decrease in the output voltage to around 4.5 V. Albeit the lower output voltage (compared to the input voltage of 5 V), the output voltage valueis comparable to minimum acceptable HIGH logical output of 2.7 – 5 V in a 5 V transistor-transistor logic (TTL) [11]. With nearly 0 V value of V_{TH}, the output voltage is assumed capable of turning-on the next SSD logic block in a circuitry since it is much higher than the noise margin of most SOI devices (furtherinvestigation on the noise margin of SOI-SSD is however recommended) [11].

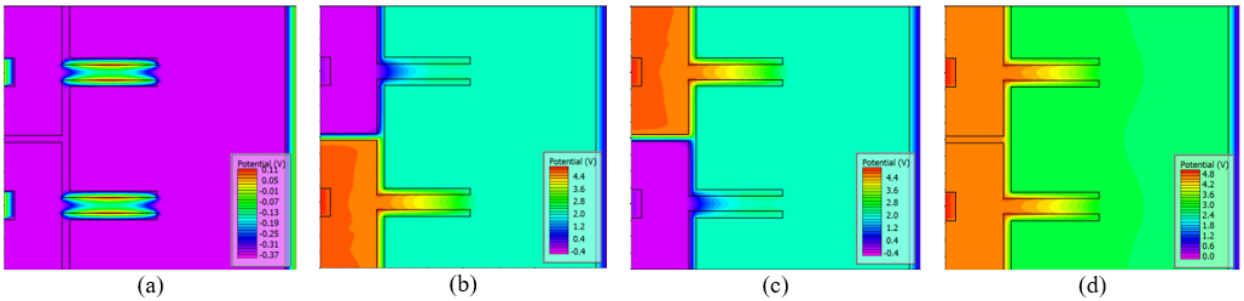


Figure 4. Potential distribution in SOI-SSD OR gate at A,B of (a) 0,0, (b) 0,1, (c) 1,0, and (d) 1,1.

3.2 Conduction current density distribution

Analysis on conduction current density and its distribution graph for input (A,B) = (0,0), (0,1), (1,0), and (1,1) are shown in Figures 5 and 6, (a) – (d), respectively where the cut lines were taken in the middle of channel A and B, to examine the current flows in the channel. As can be seen, no current flowed in the channel when A,B = 0,0. When one of the anode is HIGH (0,1 and 1,0), the current flowsin the open channel with h+ current density value of about 6000 A/cm^2 as shown in Figures 5 and 6, (c) – (d). And when both anodes are HIGH (1,1), less current flow to the right side of the device with conduction current at about 4000 A/cm^2 in in the middle of each channel because of the parallel series resistance in anodes. These current however, combined at the right side of the device which contributed to the increase of overall output current as can be seen in Figure 3(b).

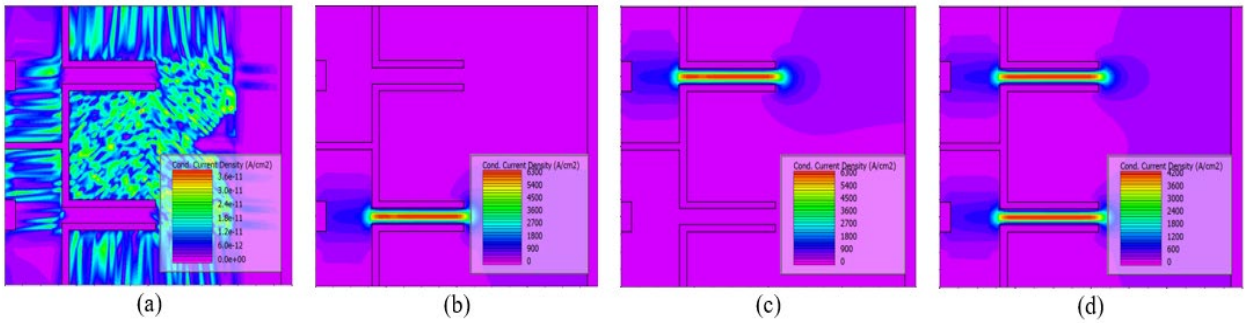


Figure 5. Conduction current density distribution at A,B of (a) 0,0, (b) 0,1, (c) 1,0, and (d) 1,1.

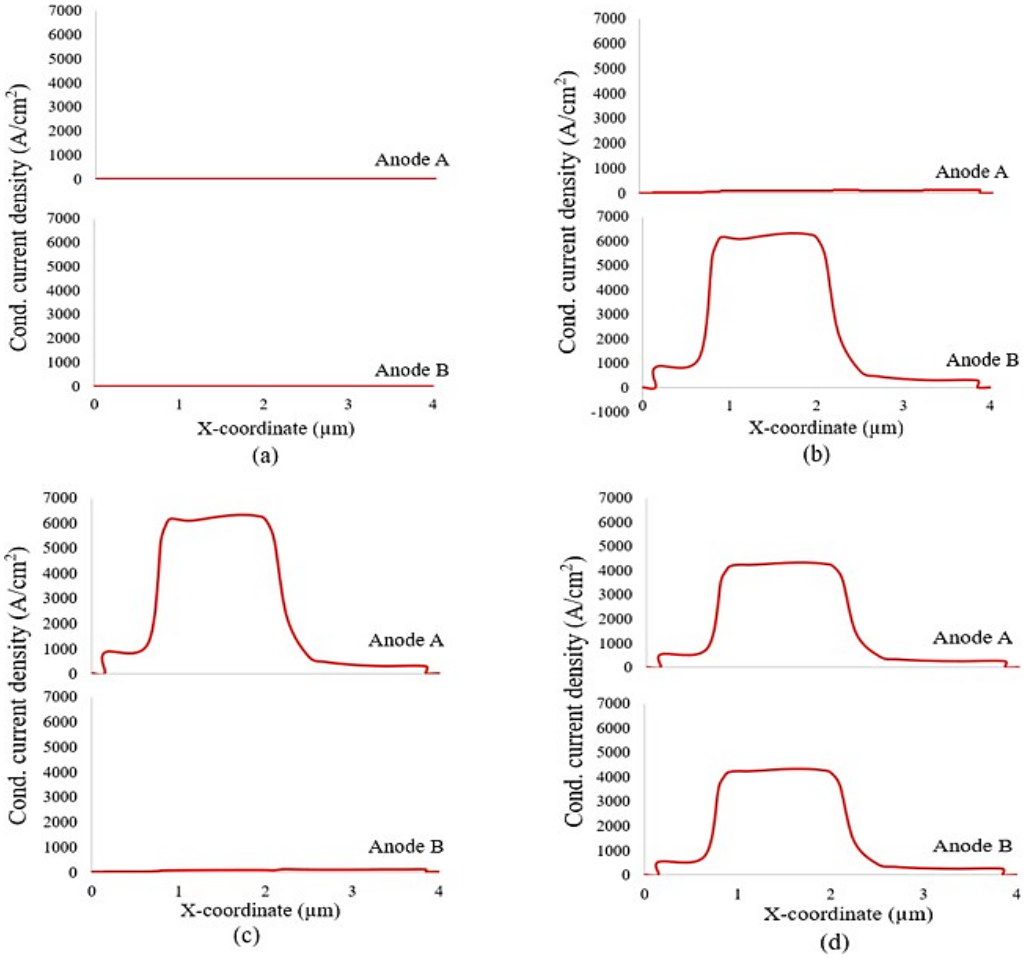


Figure 6. Conduction current density distribution graph at A,B of (a) 0,0, (b) 0,1, (c) 1,0, and (d) 1,1.

4. CONCLUSION

In conclusion, a functional SOI-SSD based OR gate device which consists of two SSDs have been successfully designed and simulated by using the ATLAS Silvaco device simulator. The simulated design showed a good OR logic output response with the inputs, and acceptable output ranged from around 4.5 to 4.8 V with 5 V HIGH inputs. The results from this OR gate characterization may assist in developingthe logic gate for device integration and may as well be a reference and a basis for future complex design such as ternary logic gates and multi-operational logic gates using SSD.

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