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Heavily Doped n++ GaN Cap Layer AlN/GaN Metal Oxide Semiconductor High Electron Mobility Transistor

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ABSTRACT

In this work, we report on the processing and device characteristics of n++ GaN/AlN/GaN metal oxide semiconductor high electron mobility transistors (MOSHEMTs). The AlN/GaN structure is capped with a highly doped n++ GaN layer which provides more free electrons in the cap layer thus helps in reducing the Ohmic contact resistance. However, this layer in the gate region needs to be removed prior to gate metal deposition to avoid a conducting path between gate metal and the cap layer. A conducting path between the gate metal and GaN cap layer creates gate to source and gate to drain short circuit. A selective etching recipe was developed between n++ GaN and AlN layers. The gas used is a mixture of SF_6 and O_2. A 5 nm SiO_2 is used as a gate dielectric and surface passivation to the device. The fabricated device shows a maximum drain current density of 800 mA/mm and a maximum peak transconductance of 135 mS/mm. The breakdown voltage of the device is 73 V. The measured contact resistance for the non-annealed and annealed Ohmic contact is between 5 to 10 Ω.mm and 0.4 to 0.6 Ω.mm, respectively. This indicates that the usage of heavily doped 5 nm n++ GaN cap layer helps in reducing the contact resistance. The results show the potential of the AlN/GaN MOSHEMT structure with a n++ GaN cap layer for future high frequency power application.

Keywords: AlN/GaN, metal oxide semiconductor high electron mobility transistors (MOSHEMTs), heavily doped GaN cap layer, selective etching the cap layer.

1. INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMTs) have been successfully demonstrated in MMIC technology for various frequencies including the mm-wave range [1-3]. While the gate length, L_G, scaling technologies enable AlGaN/GaN HEMTs to be promising candidates for higher frequency power applications, the gate to channel distance, d, must be scaled to mitigate the short channel effects [4]. To have a high aspect ratio of L_G/d, the ultra-thin AlN/GaN HEMTs also have been widely investigated. This is due to its large spontaneous and piezoelectric polarization effect which leads to a very high charge carrier density up to 3.6 x 10^{13} cm^{-2} [5], high mobility 1398 cm^2/V.s resulting from the absence of alloy disorder scattering in AlN [6] and provides low sheet resistance [5, 6]. Having these superior characteristics make the thin AlN barrier very attractive for millimetre-wave applications. There are two reasons for this: 1) sub-100 nm gates lengths can be employed without the device performance being degraded from short channel effects and 2) the large bandgap offset between AlN and GaN leads to high 2-dimensional electron gas density which would enable high power (millimetre-wave) operation.

Excellent DC and RF performances such as the highest maximum saturation currents of 4 A/mm [7], maximum peak transconductance of 2.2 S/mm [7], maximum cut-off frequency, f_T, of 454 GHz [8] and maximum oscillation frequency, f_{MAX}, of 518 GHz [7] have been achieved for this structure. Despite the reported advantages of the AlN/GaN heterostructure, the main challenge to fabricate this structure is to form low Ohmic contact resistance on this thin AlN barrier layer. In this work, the epitaxial structure is protected with a 5 nm heavily doped n++ GaN cap layer, with Si dopant concentration of 1 x 10^{19} cm^3. The usage of heavily doped n++ GaN cap layer is to help reduce the

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contact resistance of the device. We discuss the processing and device characteristics of the AlN/GaN MOSHEMT structures with a n++ GaN cap layers in the next sections of the paper.

2. Device structure and experiment

The epitaxial structure used in this work was grown by Orona Technologies, USA, using molecular beam epitaxy (MBE) on sapphire substrate. The wafer structure consists of (from top to bottom), a 5 nm heavily doped GaN cap layer with Si-doping density of 1 x 10^{19} cm^3, 3 nm AlN, 1.4 µm GaN channel layer, 0.8 µm GaN buffer layer, and a very thin AlN nucleation layer. The experimental work started with the optimization of the Ohmic contacts to investigate the optimized condition for making low contact resistance on this epilayer structure. The circular transfer length method (CTLM) was used for contact resistance measurements. The diameter of the centre circle of the CTLM structure is 150 µm with the gap spacings, L, of 4, 8, 12,16, 20, 24, 28, and 32 µm. The fabrication starts with the standard cleaning procedure for the samples. Then, an Ohmic metal stack of Ti/Al/Ni/Au (20/180/40/100 nm) was deposited using electron beam evaporator, followed by a lift-off process and annealing at 800 °C for 30 secs. Measurements were done before and after annealing to evaluate the contact resistance of the heavily doped n++ GaN cap layer AlN/GaN HEMT structure.

Next, the device was fabricated using the optimised condition of making low contact resistance from the previous experiment. A two-level wrap-around gate design (where the gate encircles the drain as shown in Figure 1a) was used to simplify the device process flow, removing the need for isolation. First, Ohmic metal contacts were formed by evaporation of Ti/Al/Ni/Au, and then annealed. Prior to gate metallization, a 5 nm n++ GaN cap layer in the gate region was selectively removed using the mixture of SF_6 and O_2 gases. Then, 5 nm of SiO_2 was deposited using plasma enhanced chemical vapor deposition (PECVD). The gate metal contacts were formed by evaporation of Ni/Au (20/400 nm), followed by a lift-off process. Finally, the 5 nm of SiO_2 in the Ohmic regions was removed using the mixture of CHF_3 and Ar gases with flow of 25 and 25 sccm, 50W, 30 mTorr at 20 °C for 60 secs for measurement purposes. All fabrication steps were defined using photolithography. The cross-section schematic diagram of the fabricated device is shown in Figure 1b. Device dimensions used in this work are as follows: Gate length, L_G, of 2 µm, gate-to-source distance, L_{GS}, of 3 µm, gate-to-drain distance, L_{GD}, of 5 µm, and gate width, W_G, of 75 µm. DC measurements were made at room temperature using Keysight's B1500A Semiconductor Device Analyzer.

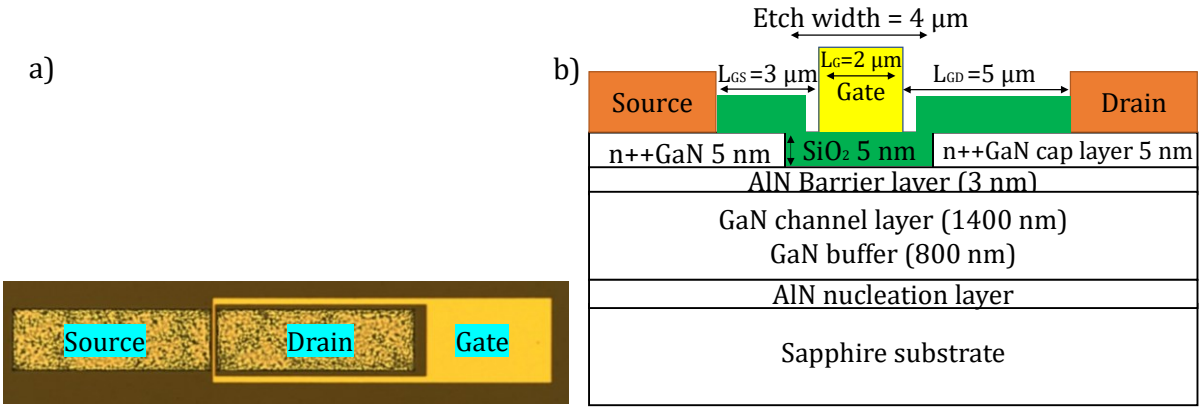

Figure 1. a) Top-view layout of a wrap-around gate device, b) Cross-section schematic diagram of fabricated n++ GaN/AlN/GaN MOSHEMT structure.

3. RESULTS AND DISCUSSION

3.1 Circular transfer length method (CTLM) measurements

Despite the benefits of using AlN as a barrier layer as mentioned in the earlier section, the main challenge of fabricating this structure is to form low Ohmic contact resistance due to the wide band gap of AlN layer. The most common method to form low Ohmic contact on GaN-based devices is by employing a high temperature annealing typically above 800°C to provide low contact resistance < 1 Ω.mm [9, 10]. Low Ohmic contact resistance is crucial for the realization of high performance GaN devices. In this work the heavily doped n++ GaN cap layer is used to help in reducing the Ohmic contact resistance. Ohmic contact optimization was performed first on the heavily doped 5 nm n++ GaN cap layer AlN/GaN HEMT structure.

The CTLM structure was fabricated as shown in Figure 2a, then the contact resistance is measured without performing a high temperature annealing process (non-annealed Ohmic contact). The measured contact resistance for the non-annealed Ohmic contact is between 5 to 10 Ω.mm. Typically, for the non-annealed Ohmic contact on GaN-based devices, it is very difficult to extract the contact resistance value due to the high resistance between the Ohmic metal and the barrier layer. However, the obtained value of non-annealed Ohmic contact is still considered high for making devices. Thus, the Ohmic contact was annealed at 800 °C for 30 secs in N_2 environment to further reduce the contact resistance (annealed Ohmic contact). The measured contact resistance for the annealed Ohmic contact is between 0.4 to 0.6 Ω.mm. The comparison between the non-annealed and annealed Ohmic contact measurements is shown in Figure 2b. From the measurements, the use of heavily doped 5 nm n++ GaN cap layer helps in reducing the contact resistance. The measured contact resistance of the annealed Ohmic contact structure is comparable with the previous published works on AlN/GaN heterostructures [11, 12].

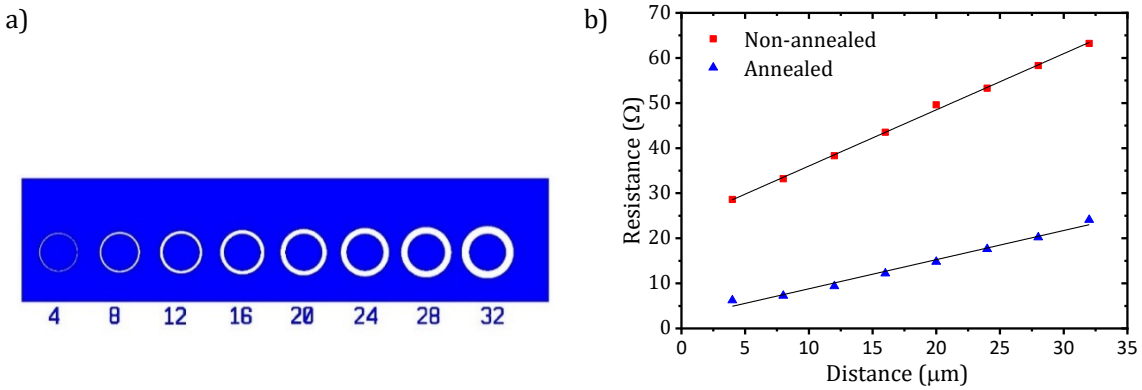

Figure 2. a) Top-view layout of CTLM structure, b) CTLM measurements for both non-annealed and annealed contact resistance of heavily doped n++ GaN/AlN/GaN HEMT structure.

3.2 Etching of 5 nm n++GaN cap layer in the gate region

The etching recipe for the removal of 5 nm n++ GaN cap layer in the gate region was developed before making devices. Four (4) samples were prepared and processed to find the etch rate of the heavily doped n++ GaN cap layer. The recipe used is as follows: SF_6/N_2 with flow rates of 20/20sccm, RF power of 70 W power and pressure of 50 mTorr with 4 different etching times (i.e 30, 60, 120, and 180 secs). Very rough surface was observed using the atomic force microscopy (AFM) scan image on the etched samples with etching time of 30, 60, and 120 secs thus resulting in difficulty to measure the etch depth. As for sample with the etching time of 180 secs, the measured etch depth was ~ 10 nm indicating that the recipe used not only etched the 5 nm cap layer, but it also etched the AlN and GaN layers.

To solve this problem, a process of selective etching of n++ GaN with respect to AlN was developed. This can be realized using the mixture of SF_6 and O_2, where the O_2 will reacts with aluminum (from the AlN barrier layer) then forms an Al_2O_3 layer which limits further etching [13, 14]. The recipe used was as follows: SF_6/O_2 with flow rates of 20/20 sccm, RF power of 70 W power and pressure of 50 mTorr, with different etching times (60, 120, 180 secs). From the AFM step height measurement, the etching time of 120 secs show the complete removal of 5 nm n++ GaN cap layer as shown in Figure 3a. The etched surface of this sample was smooth, and the measured surface roughness of 2.28 nm and 2.10 nm were obtained both for the etched and as-grown samples respectively as shown in Figure 3b. Figure 3c shows the top view of scanning electron microscope (SEM) image of the fabricated AlN/GaN MOSHEMT structure with a n++ GaN cap layer.

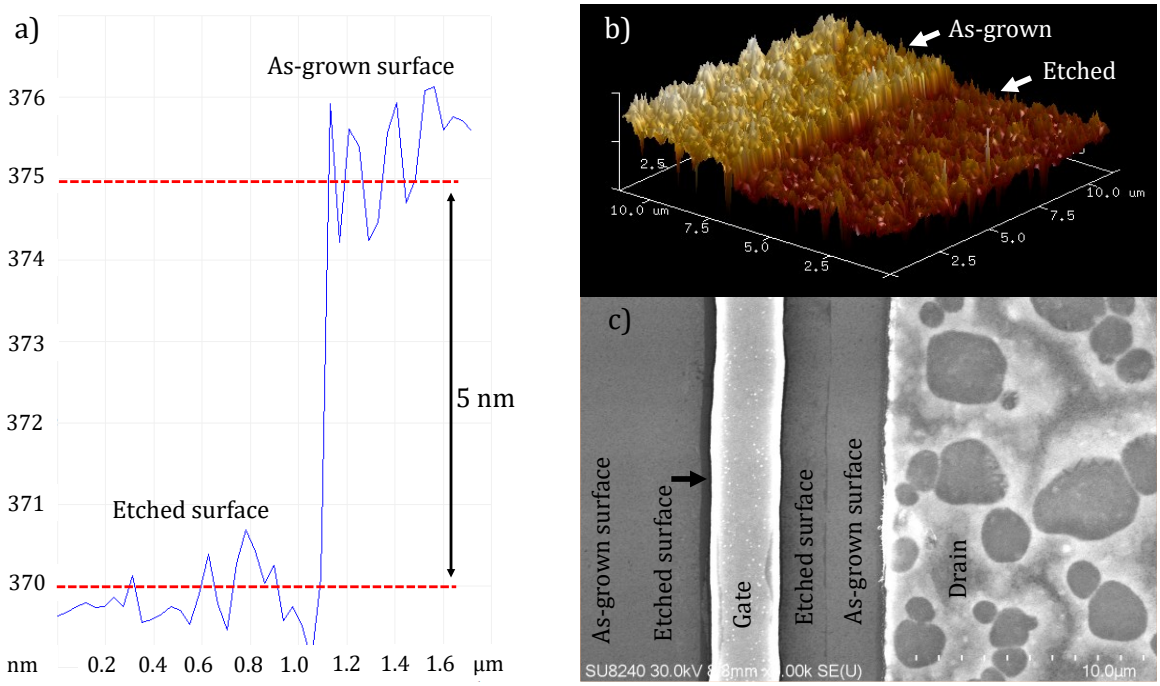

Figure 3. a) AFM step height b) AFM scan image, c) Top view of SEM image of n++ GaN/AlN/GaN MOSHEMT structure.

3.3 Device measurements

The maximum current density, I_{DS} (max), and maximum peak transconductance, g_m (max), of the fabricated device were 800 mA/mm and 135 mS/mm as shown in Figures 4a and 4b, respectively. The measured threshold voltage, V_{TH}, of -6.80 V (extracted value of gate-to-source voltage, at I_{DS} = 1 mA/mm) was obtained for the fabricated device. There is a shift to a more negative value of the measured threshold voltage due to the insertion of 5 nm SiO_2 used as a gate dielectric and surface passivation to the fabricated device as compared to our previous fabricated device of n++ GaN/AlN/GaN HEMT structure [15].

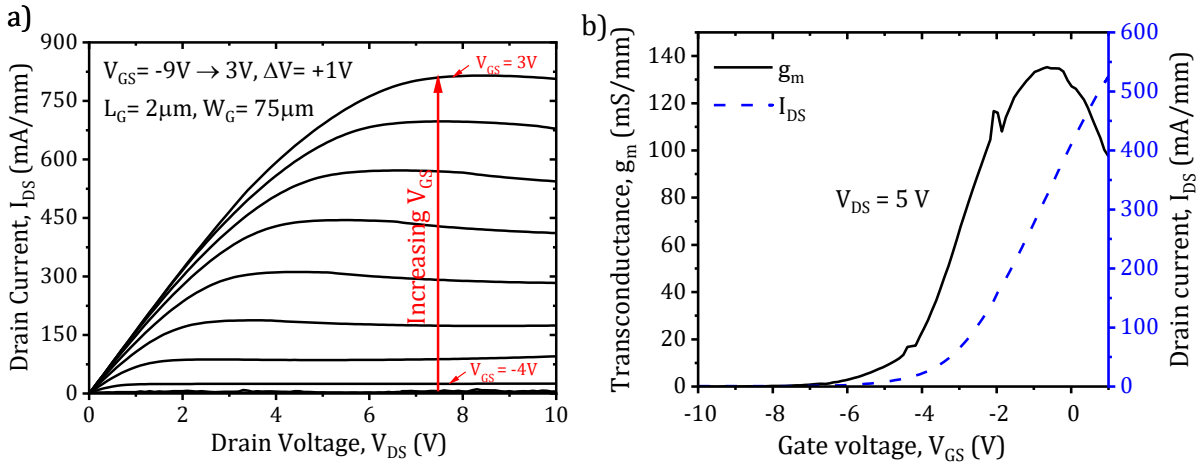

Figure 4. a) Measured output characteristics at V_{GS} biased from -9 V to 3 V (with step size of 1 V), b) Measured transfer characteristics at drain-to-source voltage, V_{DS} = 5 V of fabricated n++ GaN/AlN/GaN MOSHEMT structure.

High gate leakage current was observed for the fabricated device as shown in Figure 5a, compared to reported devices on AlN/GaN heterostructures [16]. The use of high-k dielectric materials such as Al_2O_3 and HfO_2 [17, 18] for the gate dielectric can further reduce the leakage current in the devices. The off state breakdown, V_{BR}, of 73 V was measured at V_{GS} = -10 V shown in Figure 5b. This work will be implemented in fabricating submicron devices ($L_G \leq 100$ nm) utilizing the T-gate technology to further optimize the device performance for use in the W-band (75-110 GHz) frequency band.

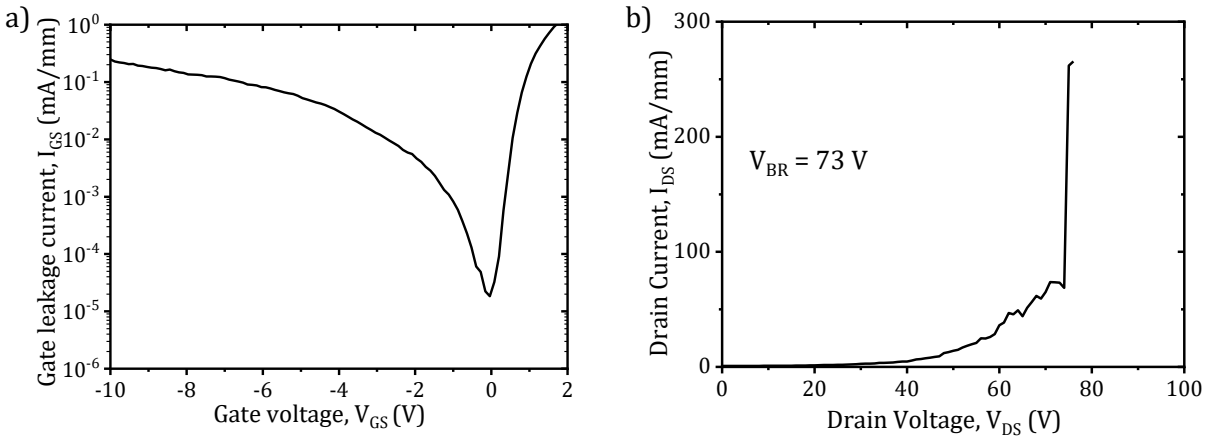

Figure 5. a) Measured gate leakage current characteristics at drain-to-source voltage, V_{DS} = 0 V, b) The off-state breakdown characteristics at gate-to-source voltage, V_{GS} = -10 V of fabricated n++GaN/AlN/GaN MOSHEMT structure.

4. CONCLUSION

We have successfully fabricated and measured an AlN/GaN MOSHEMT with a heavily doped n++ GaN cap layer. Good device characteristics have been demonstrated for this structure where the maximum drain current density of 800 mA/mm and maximum peak transconductance of 135 mS/mm were measured. The breakdown voltage of the device is 73 V. The measured contact resistance for the non-annealed and annealed Ohmic contact was between 5 to 10 Ω.mm and 0.4 to 0.6 Ω.mm respectively. The results show that the use of a heavily doped n++ GaN cap layer helps in reducing the contact resistance. Further device performance improvements can be expected by scaling down the device dimensions and utilizing the T-gate technology.

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