Genetic Algorithms For Vlsi Micro-Cell Layout Area Optimization Based On Binary Tree

Abstract

This paper presents a novel module placement based on genetic algorithm (GA) for macro-cell layouts placement that minimizes the chip area size. A binary tree method for non-slicing tree construction process is utilized for the placement and area optimization of macro-cell layouts in very large scale integrated (VLSI) design. The proposed algorithm have been developed using two types of GA: simple genetic algorithm (SGA) and adaptive genetic algorithm (AGA). The performance comparisons of these two techniques in achieving the optimal results are investigated and analyzed. The robustness of GA is also being examined in order to verify the GA performance stability. Based on the experimental results tested on Microelectronic Center of North Carolina (MCNC) benchmark circuit's data set, it exhibits that both algorithms acquire acceptable performance quality to the slicing floorplan approach. AGA performs better than SGA as it converges faster to the optimal result and obtains better optimum area. However, SGA appears to be more robust than AGA.

Author Keywords

Adaptive genetic algorithm; Binary tree; Genetic algorithm; Simple genetic algorithm; VLSI macro-cell layout