A genetic algorithm approach to VLSI macro cell non-slicing floorplans using binary tree

Abstract

This paper proposes an optimization approach for macro-cell placement which minimizes the chip area size. A binary tree method for non-slicing tree construction process is utilized for the placement and area optimization of macro-cell layout in very large scaled integrated (VLSI) design. Three different types of genetic algorithms: simple genetic algorithm (SGA), steady-state algorithm (SSGA) and adaptive genetic algorithm (AGA) are employed in order to examine their performances in converging to their global minimums. Experimental results on Microelectronics Center of North Carolina (MCNC) benchmark problems show that the developed algorithm achieves an acceptable performance quality to the slicing floorplan. Furthermore, the robustness of genetic algorithm also has been investigated in order to validate the performance stability in achieving the optimal solution for every runtime. This algorithm demonstrates that SSGA converges to the optimal result faster than SGA and AGA. Besides that, SSGA also outperforms SGA and AGA in terms of robustness.