

## IMPLEMENTATION OF FPGA-BASED ARTIFICIAL NEURAL NETWORK FOR CHARACTER RECOGNITION

049978 f QA76.87 M298 2014

# this ite OMAR SADEQ SALMAN (1332320881)

A dissertation submitted in partial fulfillment of the requirements for the degree of Master of Science (Embedded System Design Engineering)

0

School of Computer and Communication Engineering UNIVERSITI MALAYSIA PERLIS

2014

#### UNIVERSITI MALAYSIA PERLIS

	1	DECLARATION OF THESIS
Author's full name	:	OMAR SADEQ SALMAN
Date of birth	:	IMPLEMENTATION OF FPGA-BASED ARTIFICIAL
Title	:	NEURAL NETWORK FOR CHARACTER
		RECOGNITION
A		×
Arademic Session	:	
I hereby declare that t at the library of UniMA	he thesis .P. This t	becomes the property of Universiti Malaysia Berlis (UniMAP) and to be placed hesis is classified as :
	AL	(Contains confidentia   information where the Official Secret Act 1972)*
		(Contains restricted information as specified by the organization where research was done)*
OPEN ACCESS I agree that my thesis is to be made immediately available a copy or on-line open access (full text)		I agree that my thesis is to be made immediately available as hard copy or on-line other access (full text)
I, the author, give per research or academic	mission exchang	to the UniMAR to reproduce this thesis in whole or In part for the purpose of e only (except during a period of years, if so requested above).
SIGN	- K	Certified by:
G1558449	C.b.r.	SIGNATURE OF SUPERVISOR
(NEW IC NO. / PASSBORT NO.)		PORT NO.)
Date : 18/08/		2014 Date: 18/08/2014
A REAL PROPERTY.		

. If the thesis is CONFIDENTIAL or RESTRICTED, please attach with the letter from the organization with

NOTES :

or restriction.

#### ACKNOWLEDGMENT

I would like grateful to Allah for providing me with his generosity and blessing to finish this research.

I would like to express my sincere thanks and appreciation to Dr. Phaklen Ehkan, not only for his valuable advice, guidance and supervision, but also for theoretical and practical knowledge that I gained from his evolutionary for embedded system FPGA lectures during one semester.

I would also like to thank the Professor Dr. R. Badlishah Ahmad (Dean of the School) to help and support me In overcoming the difficulties that we face to complete the project perfectly.

I would like to extend my thanks to all my lecturer of School Computer and Communication Engineering Oniversity Malaysia Perlis (UniMAP), for shearing me all knowledge that some of jt has been very beneficial to achieve this work.

Last but not least, I would like to extend deepest gratitude to all my family members for their support and endless moral inspiration and encouragement to overcome all the obstacles to completing this research. And I would like to to thank in particular to my wife, who has provided moral support and stand by my side to complete the project fullest, and especially my friends Dr.Thanaa Hussain , Eng. Yee Ann and many others that whose names I cannot recall.

#### To my beloved mother and father

"I would not achieve this without both of you"

#### TABLE OF CONTENTS

		PAGE
THES	IS DECLARATION	i
ACKN	OWLEDGMENT	ii
TABL	E OF CONTENTS	iii
LIST	OF TABLES	vii
LIST	OF FIGURES	viii
LIST	OF ABBREVIATION SYMBOL	xi
ABST	RAK	xiii
ABST	RACT	xiv
	to.	
CHAI	PTER 1 INTRODUCTION	1
1.1	Problem Statement	3
1.2	Objectives Q	5
1.3	Scope	5
1.4	Contribution of the Research	5
1.5	Thesis Organization	6
СНА	PTER 2 LITERATURE REVIEW	7
2.1	Introduction	7
2.2	Neural Computation	9
2.3	Artificial neural networks (ANNs) and Back Propagation (BP)	13

#### Algorithm

2.4	Field Programmable Gate Arrays (FPGA)	17
2.5	Neural networks on FPGAs: specific assets	20
2.6	Optical character recognition (OCR)	25
2.7	Summary	32
СНАР	TER 3 RESEARCH METHODOLOGY	34
3.1	Introduction.	34
3.2	The specifications of the Altera DE2 board	35
3.3	Altera Quartus II Development Tools	36
3.4	Hardware Components	39
3.5	Structure Approach For Character Recognition System	40
	3.5.1 Study and Develop the architecture of ANN implemented on FPGA	41
	3.5.2 Train the ANN for character recognition and downloaded onto	42
<ul> <li>C)</li> </ul>	9.5.3 The ANN is later deployed for character recognition application using actual data.	44
	3.5.4 The resulting data obtained from the deployment of the ANN is collected and analyzed.	45
3.6	Algorithm	45
	3.6.1 Feed Forward	46
	3.6.2 Back Propagate	46
3.7	Project Design	47

3.8	Implementation	51
	3.8.1 Pattern Recognition Network	52
	3.8.2 Integration	54
3.9	Challenges	56
	3.9.1 Floating Point Implementation	56
	3.9.2 Neural Network Size Limit	57
	3.9.3 Training Length	57
	3.9.4 LCD_control limitation	58
	in al	
CHAI	PTER 4 RESULTS AND DISCUSSIONS	63
4.1	Introduction	63
4.2	Top Level Entity	63
	4.2.1 Artificial Neural Network Block	65
	4.2.2 ANN Fraining Supervisor Block	65
	4.2.3 Pseudo-random Number Generator Block	66
	4.2.4 Floating Point Processor Block	66
C	4.2.5 SRAM Driver Block	66
	4.2.6 LCD Controller Block	66
	4.2.7 LCD Driver Block	67
4.3	FPGA Device's Resources Used	67
4.4	Outcome	69

	4.5	The working system	73
	4.6	Analysis of the system	76
	4.7	Problems in the system	78
	4.7	Conclusion	79
	СНАРТ	TER 5 CONCLUSIONS AND RECOMMENDATION	81
	5.1	Introduction	81
	5.2	Conclusion	81
	5.3	Future work	83
		orio	
	REFEF	RENCES	84
APPENDIX A			88
APPENDIX B		89	
	APPEN	NDIX C	93
	APPEN	NDIX D	95
	APPEN	NDIXE	98
	-	(Kr.	
	$\bigcirc$		

vi

#### LIST OF TABLE

. .....

NO.		PAGE
2.1	Appropriate/inappropriate devices for neural network implementations.	20
3.1	The Main Lcd_Control To Defined All Character	59
3.2	The Lcd_Control To Defined Arabic Character.	60
3.3	The Pattern To Defined English Character	61
3.4	The Pattern To Defined Arabic Character.	62
4.1	Comparison between three project compilation report on Altera QuartusII.	67
4.2	Sample English Character Pattern Recognition and Its Expected Output.	70
4.3	English character with Toggle Key and ASCII code.	71
4.4	Sample Arabic Character Pattern Recognition and Its Expected Output.	72
4.5	Arabic character with Toggle Key.	73
4.6	English character (C and D) with Toggle Key and pattern.	79

 $\bigcirc$ 

#### LIST OF FIGURE

NO.		PAGE
2.1	Mapping of Human Brain.	9
2.2	Structure Of Neural Network.	10
2.3	Character Matrix A Of Different Fonts.	11
2.4	Neural Network Architecture.	11
2.5	Reconstructed Shape Of 'E' Using Features.	12
2.6	The Neuron Components.	14
2.7	An Artificial Neuron.	15
2.8	Step Of OCR.	17
2.9	How To Read ANN The OCR.	17
2.10	Altera FPGA Structure.	18
2.11	Xilinx FPGA Structure.	18
2.12	(a) nput Patterns With Three Different Fonts For Each Character. (b) Perceptron Model Used For The Character Recognition Problem.	23
2.13	Compare Left Halves And Right Halves And Upper Halves And Lower Halves Of Digits.	24
2.14	a ) Divide Picture To Four Horizontal And Four Vertical Section, b) Count The Number Of Intersections Along Middle Vertical Ray.	24
2.15	The Block Diagram Of Elastic Meshing Directional Feature Extraction.	25

	2.16	Stages In OCR Design.	27
	2.17	<ul> <li>a) Preprocessing Flowchart , b) Vertical Lines At Different Heights , c) Horizontal Lines At Different Heights , d) Horizontal &amp; Vertical Symmetry In Characters.</li> </ul>	28
	2.18	a) Embedded LPR System Block Diagram., b) Hardware Block Diagram.	30
	2.19	a) And b) Pictures Are Divided To Four Horizontal And Four Vertical Sections, c) Count The Number Of Intersections Along Horizontal Ray Of And Written And Typed Images., d). The Block Diagram Of Feature Extraction Block.	31
	2.20	Block Diagram Of Sequence Recognition Character.	32
	3.1	The DE2 Board.	35
	3.2	Block Diagram Of The DE2 Board.	36
	3.3	Altera Quarrus Ii Web Edition Software Version 9.1 Sp2.	37
	3.4	Designing Flow of FPGA.	38
	3.5	Flow Chart Of Process.	40
	3.6. xen	Explain each stage in step 1	42
~	X.A.S	Simulation of the system	43
)	3.8	Explain each stage in step 2	43
	3.9	Explain each stage in step 3	44
	3.10	(a) Structure Of A Artificial Neural Network Perceptron,	45
		(b) Represent The Weight Of Perceptron And Sigmoid.	
	3.11	Connection between tow layer	46

3.12	Component of Artificial Neural Network Block diagram for the system.	49
3.13	English Pattern Recognition On A 4x4 Binary Grid.	51
3.14	Arabic Pattern Recognition On A 4x4 Binary Grid.	52
3.15	Block Diagram of the ANN system	53
3.16	Block Diagram Of The Integrated System.	55
3.17	a) Display Of DE2 FPGA Board 32 Character Has 2 Raw Each Raw 16 Character, b) Matrix Of Character 5x8 Pixel In Screen.	58
3.18	The Display Showed The Character ( A) And Recognized It.	59
4.1	Synthesized Top-Level RTL Circuit	64
4.2	Project compilation report on Altera QuartusII for 20 English and 3 Arabic character	68
4.3	Compilation Tools Of The Program.	69
4.4	a) How the distribution the toggle key in the Lcd_screen, (b) The form of pattern represent by matrix 4x4 for each character (Example: Character A)	69
4.5	System Output During Initialization.	74
4.6	System Output During Ann Training Phase.	74
4.7	System Output During Training Mode.	74
4.8	System During Reset The FPGA Board.	75
4.9	System During Reset The Software.	75
4.10	System Output Running Mode.	76
4.11	Time to detect the accepted character	77

O This teen is protected by original copyright

performances

#### LIST OF ABBREVIATION

ANN	Artificial Neural Networks	
ALU	Arithmetic Logic Unit	
ASIC	Application-Specific Integrated Circuit	
BIST	Built-in Self-Test	×
BP	Back Propagation	
BPNN	Back Propagation Neural Network	
CLB	Configurable Logic Block	
CPLD	Complex Programmable Logic Device	
CPU	Central Processing Unit	
DSP	Digital Signal Processor	
FP	Forward Propagation	
FPGA	Field Programmable Gate Array	
Flopoco	Floating Point Cores	
HDL	Hardware Description Language	
IC	Integrated Circuit	
IEEE	Institute Of Electrical And Electronic Engineering	
IOB	Input Output Block	
LCD	Liquid Crystal Display	
LFSR	Liner Feed Back Shift Register	
LPR	License Plate Recognition	

MLP	Multilayer Perceptron
MSE	Mean Squared Error
N_H	Number of perceptrons in the hidden layer
N_I	Number of perceptrons in the input layer
N_O	Number of perceptrons in the output layer
NN	Neural Network
OCR	Optical Character Recognition
PI	Programmable Interconnect
PR	Pattern Recognizer
RR	Relative Risk or Risk Ratio
RTL	Register-Transfer Level
SOM	Self-Organizing Map
SRAM	Static Random Access Memory
VHDL	VHSIC Hardware Description Language
VHSIC	Very-High-Speed Integrated Circuits
VLSI	Very-Large-Scale Integration
	- Au

#### Implementation Of FPGA-Based Artificial Neural Network For Character Recognition

#### ABSTRACT

Artificial Neural Networks (ANN) are non-linear applied math knowledge data modeling tools, usually used model advanced relationships between inputs and outputs or to seek out patterns in data. A generic hardware primarily based ANN is planned and executed using VHDL coding. This project may be seen as a place to begin for learning ANN. It explores in approach a hardware-based application of ANN employs FPGA. The sixteen toggle switches are given as input while the end product is exhibited on the LCD display. This classifier is trained to identify letters on a 4x4 binary grid filled by a user through 16 toggle switches. The most probable class suggested by the ANN is displayed on an LCD screen. To demonstrate the practicality of FPGA execute of ANN, the ANN trained to acknowledge twenty English and nine Arabic character patterns on a 4x4 grid. In structural of ANN, the used of three-layer is implemented entirely with 32-bit single exactitude floating purpose arithmetic to ensure flexibility and accuracy for its wide selection of applications. The resulting design file is programmed into the Altera Cyclone II FPGA on the Altera DE2 development and education board. The design also includes a training supervisor that trains the ANN recognized the total of 29 English and Arabic alphabet predefined characters. The result is promising as the ANN is able to recognize all characters defined to training characters patterns. Each alphabet is tested in 20 English alphabet and 9 Arabic alphabet, after implementation, are done and performance issues of the design are analyzed. The output gives good results, and finally this project shows the flexibility and also the endless chance of hardware primarily based implementation of ANN, the achievement of recognition rate for alphabet English and Arabic character are 76.92% and 32.14% respectively.

#### Pelaksanaan FPGA Berasaskan Buatan Neural Rangkaian Untuk Watak Pengiktirafanm

#### Abstrak

Rangkaian neural tiruan (ANN) adalah alat pemodelan pengetahuan matematik bukan linear, kebiasaannya digunakan untuk hubungan model canggih antara masukan dan keluaran atau untuk mencari corak dalam data. Satu perkakasan umum terutamanya berdasarkan ANN dirancang dan dilaksanakan menggunakan kod VHDLX Projek ini boleh dilihat sebagai tempat untuk memulakan pembelajaran ANN. Jao menerokai dalam pendekatan aplikasi perkakasan berasaskan ANN menggunakan FPGA. Enam belas suis togol diberikan sebagai masukan manakala produk akhir dipamerkan pada paparan LCD. Pengkelas ini dilatih untuk mengenalpasti dua puluh huruf bahasa Inggeris dan sembilan huruf bahasa Arab pada grid binari 4x4 yang diisi deh pengguna melalui 16 suis togol . Kelas paling tinggi kemungkinannya dicadangkan oleh ANN dipaparkan pada skrin LCD. Untuk memperlihatkan praktikal FPGA melaksanakan ANN, ANN dilatih untuk mengakui dua puluh corak huruf bahasa Inggeris dan sembilan corak huruf bahasa Arab pada grid 4x4. Dalam struktur ANN, tiga lapisan dilaksanakan sepenuhnya dengan 32-bit terapung aritmetik ketepatan tunggal bertujuan untuk memastikan fleksibiliti dan ketepatan pilihan aplikasi secara meluas. Fai keputusan rekabentuk diprogramkan ke atas Altera Cyclone II FPGA pada papan pembangunan dan pendidikan Altera DE2. Rekabentuk ini juga termasuk penyelia atihan yang melatih ANN mengiktiraf 29 huruf bahasa Inggeris dan bahasa Arab Rasilannya amat memuaskan kerana ANN dapat mengenali semua hurufhuruf yang telah ditakrifkan kepada corak-corak huruf latihan. Setiap abjad diuji dalam 20 abjad bahasa Inggeris dan 9 abjad arabic, Selepas pelaksanaan, selesai dan isu-isu prestasi reka bentuk dianalisis. Output yang memberikan keputusan yang baik Secara keseluruhannya, dan akhirnya projek ini menunjukkan fleksibiliti dan pelaksanaan juga peluang yang tidak berkesudahan perkakasan terutamanya berasaskan ANN, pencapaian kadar pengiktirafan untuk abjad Inggeris dan Bahasa Arab adalah watak masing-masing 76,92% dan 32.14%.

#### CHAPTER 1

#### INTRODUCTION

The electronic devices production field has witness a great revolution by having the new birth of the extraordinary FPGA family platforms recently. These platforms are the optimum and best choice for the modern digital systems nowdays. The parallel structure of a neural network (NN) makes it potentially fast for the computation of certain tasks. The same feature makes NN well suited for implementation in VLSI technology. Hardware realization of an NN to a large extent depends on the efficient implementation of a single neuron. FPGA-based reconfigurable computing architectures (Ali & Mohammed, 2010) are suitable for hardware implementation of NNs. FPGA realization of ANNs with a large number of neurons (Jung & su Kim, 2007) is still a challenging task.

An ANN is the information processing paradigm that is inspired by the way biological nervous systems, such as the brain and process information. The key element of this paradigm is the novel structure of the information processing system. It is composed of a large number of highly (J. Khan et al., 2001) interconnected processing elements called neurons, working in unison to solve specific problems (Shukla and Kumar (2012)). ANNs, like people, learned by example. An ANN is configured for a specific application, such as pattern recognition or data classification, through a learning process. Learning in (J. Khan et al., 2001) biological systems involves adjustments to the synaptic connections that exist between the neurones. This is true of ANNs as well. Optical Character Recognition, usually abbreviated to OCR, is the mechanical or electronic conversion of scanned images of handwritten, typewritten or printed text into machine-encoded text. It is widely used as a form of data entry from some sort of original paper data source, whether documents, sales receipts, mail, or any number of printed records. It is a common method of digitizing printed texts so that they can be electronically searched, stored more compactly, displayed on-line, and used in machine processes such as machine translation, text-to-speech and text mining the is a field of research in pattern recognition and computer vision.

Automated OCR has gained impetus largely due to its application in the fields of computer vision, intelligent text recognition applications and text based decision making systems. The approach taken to solve the OOR problem was based on psychology of the characters as perceived by the humans. Thus the geometrical features of a character (Shrivastava & Sharma, 2012) and its variants were considered for recognition (Lerman, Furuyama, & Nugent, 1990. Later, a Template-matching approach was followed that involved comparing input characters to pre-defined templates. This method recognized characters either as an exact match or no match at all (Chandra & Sudhakar, 1988). It also didn't accommodate effects like tilts and style variations that didn't involve major shape alterations. Another approach, namely recognition using correlation coefficients was based on the cross correlation of input characters or their transforms, with the database templates, so as to accommodate minor differences was used. It introduced false or erroneous recognition among characters very similar in shape, such as 'I' & 'J', 'B' & '8', 'O' and 'Q' & '0'. The solution to this problem lies in ANN, a system that can perceive and recognize a character based on its topological features such as shape, symmetry, closed or open areas, and number of pixels. The advantage of such a system is that it can be trained on 'samples' and then can be used to recognize characters having a similar (not exact) feature set. The ANN used in this system gets its inputs in the form of feature vectors. This is to say that every feature or property is separated and assigned a numerical value. The set of these numerical values that can be used to uniquely identify each character is called its vector. Thus, a vector database is utilized to train the network, so as to enable it to effectively recognize each character based on its topological properties.

An FPGA is one of the technologies which is getting much attention in recent field of research when it comes to parallel processing. FPGA is a programmable device on which can be developed almost any digital system that using HDL. Since it is programmable and many convenient HDL languages have been developed, engineers tend to use it for their prototype designs before going into ASIC. In this project, the development of recognizing optical characters was performed on hardware using Altera Cyclone II EP2C35F672C6 FPGA chip. A satisfying analysis result of the hardware has demonstrated that the character recognition project using ANN approach shown very promising.

### 1.1 Problem Statement

The ANN has been widely implemented, however, the current implementations of ANN is mostly software based. This limits the actual capabilities of the ANN as the actual processing is done by the conventional general-purpose processor of the computer system of which the ANN is running on. Even though the ANN had been implemented in hardware before, the total number of hardware based implementations of ANN is limited as compared to the software based implementations. This is because of the complexity of the ANN itself and the complexity of the resulting circuit when the ANN is to be constructed using hardware devices. The complexity is coming from the structure of the ANN that is depended on three main element, this elements are:

- · The structure of the nodes.
- · The topology of the network.
- · The learning algorithm used to find the weights of the network

For practicality because of this construction, it is more ideal for the ANN to be constructed on a single chip. This again posed another problem as the development of application specific integrated circuit (ASIC) is extremely costly.

Hardware implementation of ANN using ASIC faced another issue due to the high cost that came from the development of the complex ANN circuit, the process to produce the IC, and the lack of demand for ASIC based ANN devices. Furthermore, ASIC based ANN is application specific and cannot be reconfigured for other purposes. This is where FPGA based implementation of ANN comes into perspective. Previously, the FPGA was not seriously considered as the hardware base for implementation of ANN mainly due to its poor performance in yesteryears, but the advancement in FPGA technologies nowadays made ANN implementation on FPGA possible. Moreover, despite the FPGA has considerably inferior performance than ASIC, the flexibility offered by FPGA made it better choice for small-scale implementation of ANN, and it is also possible to reconfigure the FPGA according to the ANN to be implemented.

#### 1.2 Objectives

This project is aimed to acknowledge the character recognition ANN approach on hardware-based FPGA. This contain the fundamental purposeful structure and style of ANN, the algorithms to run the ANN and conjointly (training and educational) rules to training the ANN to produce the expected result. The main objectives of this project is to implement the FPGA primarily based ANN for character recognition application and to be prepared acknowledge type of characters to match the output from the ANN with the by original co actual result.

#### 1.3 Scopes

The research focusing on improving the system performance of the character recognition ANN approach using FPGA, and explain the architecture for ANN implemented on FPGA board. These included learning algorithm to train the ANN system using feed forward (FF) and back probagation (BP) algorithms. An analysis the classification of training and accuracy of analysis cost and effeciencies. The resulting data obtained from the deployment of the ANN is collected and analyzed. Data analysis is presented to be used by others in a format and easily understood by other reader. Moreover, the illustrate the advantage of this system to people in the life.

#### 1.4 Contribution of the Research

This analysis will introduce a new hardware based totally implementation of ANN and to preface a brand new FPGA style for implementing academic degree ANN to undertake to cut back the price and power consumption, the implementation of ANN on hardware as in FPGA is anticipated to beat the slower method speed of current package primarily based mostly implementation of ANN, i.e. character recognition. That associate with these systems have driven researchers to seem for appropriate platforms.

#### 1.5 Thesis Organization

This thesis will cover the project of FPGA implementation of ANN for character recognition. It is organised as follows:-

- Chapter 2 will introduce the structure of biological neuron, the basic of ANN and its learning algorithm, the HDL used in this project, and the FPGA. This chapter also explore the related works regarding this project and the tools used throughout the project.
- Chapter 3 discusses the proposed methodology and how to implemented this system on the FPGA DE2 board. It will explain the steps taken to implement the ANN on FPGA device and to apply the developed ANN for character recognition.
- Chapter 4 demonstrates the result of the system and explain the number of character using in this work.
  - Chapter 5 concludes the whole project and provides a few things that can be improved concerning the project in the future.

#### **CHAPTER 2**

#### LITERATURE REVIEW

#### 2.1 Introduction

ideas **Bio-inspired** such as NNs. evolution and learning have attracted abundant attention. Recently, a result of growing interest in the automatic design of advanced and intelligent systems that result in adaptation and fault tolerance. Engineers and computer scientists have studied these biological concepts in an effort to replicate their desired qualities (Hanan A. R. Alskar & Mahdi, 2010) in computing systems. The necessities for advanced integration, intensive on board process, and low power consumption, so FPGAs emerge as a technology of alternative that strikes the best balance between process power, energy necessities, and flexibility , through the power of reconfigurability (Khammas, 2012).

The conception of ANNs is emerged from the principles of brain that translated to digital computers. In 2007, this is the first works of ANNs were the models of neurons in brain arithmetic rule by Haykin (Haykin, 2007). These works show that neuron in ANNs take some data as associate number of input from associate degree other neuron or from an external input. This data is propagated as associate degree output that computed as weighted add of inputs and applied as non-linear perform.

Architectural ANNs parameters such as numeral of inputs per neuron and every neuron's conduction variation remarkably from one application to another. Thus, for special purpose network architectures parameters should be neatly balanced for effective implementation (Sahin, Becerikli, & Yazici, 2006).

FPGA is a sort of programmable logic, which provide flexibility in style like software system, however with performance speeds nearer to Application specific integrated circuits (ASICs), NN implementation in hardware employ FPGAs are chosen for implementation ANNs with the following reasons (Khammas, 2012)

- They can be applied a wide range of logic gates starting with tens of thousands up to few millions gates.
- They can be reconfigured to change logic function while resident in the system.
- FPGAs have short design cycle that leads to fairly inexpensive logic design.
- FPGAs have parallelism in their nature. Thus, they have parallel computing environment and allows logic cycle design to work parallel.

· They have powerful design, programming and syntheses tools.

Until recently, the sole alternatives were to develop custom hardware (typically board level or ASIC), buy expensive fixed function processors, or use associate degree array of microprocessors. FPGAs provide a chance to accelerate your digital signal process application up to a thousand times over a conventional DSP chip. The most goal here is coming up with associate degree OCR system in FPGA and to develop algorithms that are appropriate for hardware implementation of OCR. The applying projected here is automatic activity of instrument supported OCR system in FPGA. This solution benefits from significant reducing of work quantity for calibration as well as from better