UNIVERSITI MALAYSIA PERLIS SCHOOL OF MICROELECTRONIC ENGINEERING



Thesis in partial fulfillment of requirements for the Degree of Bachelor of Electronic Engineering

April 2011

UNIVERSITI MALAYSIA PERLIS

SCHOOL OF MICROELECTRONIC ENGINEERING

ABSTRAK

REKAAN SEBUAH CIP ENKRIPSI MENGGUNAKAN VIGENERE CIPHER

oleh Tan Shih Peng

Projek ini mencadangkan pelaksanaan peranti keras pada sebuah algoritma Vigenère cipher yang dinbahsuai. Pengubahsuaian algoritma Vigenère terdiri daripada plaintext tersebar disulitkan dengan pseudorawak sesi kunci secara simetris. Kunci utama kemudian disulitkan menggunakan teknik enkripsi asimetris. Kombinasi algoritma enkripsi simetri dan asimetri mencapai keselamatan mesej dan kunci semasa penghantaran kepada penerima. Perekaan ini ditulis dalam kod HDL Verilog disintesis, dan ciphertext disahkan melalui dekripsi kepada mesej asal. Peranti keras menggunakan 3,215 elemen lojikal pada cip FPGA Altera Cyclone II dan beoperasi pada 10.76 MHz.

April 2011

UNIVERSITI MALAYSIA PERLIS

SCHOOL OF MICROELECTRONIC ENGINEERING

ABSTRACT

THE DESIGN OF AN ENCRYPTION CHIP USING VIGENÈRE CIPHER

by Tan Shih Peng

This project proposes a hardware implementation of a modified Vigenère cipher algorithm. The modified Vigenère algorithm comprises of a diffused plaintext encrypted with a pseudorandom session key generator symmetrically. The master key then is encrypted using asymmetric encryption technique. The combination of symmetric and asymmetric encryption algorithm achieves security of the message and the key during transfer to the receiver. The design is written in synthesizable Verilog HDL code and the ciphertext is verified through decryption of itself to obtain the original message. The hardware resource consumes 3,215 LEs on an Altera CycloneII FPGA chip and operates at 10.76 MHz.

Contents

Abstrak	ii
Abstract	iii
List of Tables	vi
List of Figures	vii
Declaration of Authorship	viii
Acknowledgement	ix
Nomenclature	x
Chapter 1. INTRODUCTION	1
1.1 Project Background	1
1.2 Problem Statement	2
1.3 Objectives	3
1.4 Scope of Project	3
Chapter 2. LITERATURE REVIEW	4
2.1 Overview of Vigenère Cipher	4
2.2 Vigenère Algorithm with Padded Plaintext	5
2.3 Plaintext transformations	7
2.4 Asymmetric Key Encryption	10
Chapter 3. METHODOLOGY	14
3.1 Design of the Algorithm	14
3.1.1 Analysis of Existing Cipher Structure	14
3.1.2 Design of the Padding Component	15
3.1.3 Design of the Key Stream Generator	17

3.1.4 Design of the Vigenère Cipher	19
3.1.5 Asymmetric Encryption of Key	19
3.1.6 Top Level Design	22
3.2 Project Flow	22
3.3 Simulation and Design Validation	23
3.4 FPGA Implementation	24
3.5 Gate-level Synthesization-LeonardoSpectrum	24
Chapter 4. RESULTS AND DISCUSSIONS	26
4.1 Functional Simulations	26
4.1.1 Waveform of the Padding Algorithm	26
4.1.2 Waveform of the Keystream Generator	27
4.1.3 Waveform of Vigenère Algorithm	28
4.1.4 Waveform of Asymmetric Encryption	28
4.1.5 Waveform of Top Level Design	29
4.2 Verification of Ciphertext by Decryption	31
4.3 Timing and Area of Encryption Algorithm	
4.4 ASIC Synthesization Report	37
4.5 Discussion on Overall Project	39
Chapter 5. CONCLUSION	41
5.1 Summary	41
5.2 Recommendation for Future Project	42
References	43
Appendices	45
A. Block Diagram of Top Level Interface	45
B. Design Source Codes	46
C. Block Diagram of Encryption Algorithm Sub-Modules	66

List of Tables

Table 1.1 Mono alphabetic cipher system	…1
Table 1.2 Vigenère Tableau	·· 2
Table 2.1 Playfair Table	8
Table 2.2 Encrypting "CR"	9
Table 2.3 Symmetric Key versus Asymmetric Key	· 12
Table 3.1 Number of padding bits for each character of plaintext	·16
Table 3.2 Distribution of padded bits, x is a random bit, t is the bit value of plaintext	·17
Table 3.3 Diffusion of 'HELLO WORLD'	·17
Table 3.4 Linear Congruential Generator Parameters	·18
Table 3.5 Input Key Used As Keystream Generator Parameters	·18
Table 3.6 Steps to calculate 255143 mod 493 = 306	20
Table 3.7 Montgomery Domain in Right-to-Left Exponentiation	· 21
Table 4.1 Input Plaintext and Key	26
Table 4.2 Top Level Inputs	30
Table 4.3 Comparison Between Two Methods	36
Table 4.4 Benchmark Specification	37
Table 4.5 Synthesis Area Report	·37
© this item is pre	

List of Figures

Figure 2.1 Flow of modified version of Vigenère Cipher 5
Figure 2.2 Example implementation of RSA algorithm11
Figure 3.1 Algorithm Design 15
Figure 3.2 Project Implementation Flow23
Figure 3.3 LE in FPGA25
Figure 3.4 Timing Report of FPGA25
Figure 4.1 Individual Plaintext Diffusion of "MY NAME IS"
Figure 4.2 Diffusion of "MY NAME IS" 27
Figure 4.3 Combining Plaintexts 27
Figure 4.4 Keystream Sequence 28
Figure 4.5 Vigenere Cipher Waveform28
Figure 4.6 Asymmetric Encryption Waveform 29
Figure 4.7 Fast Exponentiation Waveform 29
Figure 4.8 Top Level Waveform
Figure 4.9 A Complete Simulation Waveform of the Overall Cipher
Figure 4.10 Encryption Waveform Using Another Key and Plaintext Message33
Figure 4.11 Decryption of Encrypting Key Waveform
Figure 4.12 Decryption of Ciphertext
Figure 4.13 STDOUT of Plaintexts
Figure 4.14 Modular Exponenatiation in Single Clock Cycle
O THIS HER

Declaration of Authorship

I, TAN SHIH PENG, declare that the thesis entitled THE DESIGN OF AN ENCRYPTION CHIP USING VIGENÈRE CIPHER and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a bachelor degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;

I have acknowledged all main sources of help;

• where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;

Signed: 20/4/11 Date:

Acknowledgement

I am heartily thankful to my supervisors, Siti Zarina Md Naziri and Mohd Fairus Bin Ahmad, whose encouragement, guidance and support from the initial to the final level enabled me to develop an understanding of the subject.

The lessons and experience gained over this two semesters has been immeasurable.

Lastly, I offer my regards and blessings to all of those who supported me in any respect and patiently gave me their time in all of my case studies during the completion of the project.

Despite the geographical distance, my family was always nearby. My mother made sement sement orietted by orietted this item is protected this item is protected sure I felt her confidence and encouragement, and his advice was consistently

Nomenclature

РТ Plaintext СТ Ciphertext K Encryption/Decryption Key (for symmetric encryption) Ν Modulus of asymmetric encryption Encryption key, public key (for asymmetric encryption) Ε Decryption key, secret key (for asymmetric encryption) D modu, oriteinal Mathematical representation of modulus