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Low Loss Optimization of Strip Channel Polysilicon Waveguide Fabrication

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ABSTRACT

Research on waveguide structures, its behaviour and material properties are very extensive for a wide range of applications. Generally, waveguides are used for optical devices such as biosensors. This paper investigates and presents an overview of the formation of waveguides using polysilicon as a waveguide material. Besides that, this paper elaborates and summarizes the important control parameters which influence the waveguide performance such as thickness, flatness, surface roughness, grain side, defects among others. The aimed that this review paper to come up with optimized parameters for the design of linear waveguides with maximum sensitivity in an evanescent field and low optical loss.

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INTRODUCTION

Optical detection are gaining reputation as the desirable technology for biosensors due to its quick response, can be miniaturized, low cost and highly sensitive to analytes detection[1]. In recent years, biosensors based on waveguide technology have attracted much attention due to their ability and versatility in high throughput applications. Linear waveguide is the fundamental component for optical devices which are used to guide the power of light, thereby playing an important role in optical biosensor design. Linear waveguide is comprised of a material with a high refractive index surrounded on all sides by materials with lower refractive indices. This arrangement allows coupled light to propagate through the high refractive index waveguide by total internal reflection. Part of the light will penetrate into the upper cladding layer and this portion of light is known as the evanescent field.

Therefore, this review paper is aimed at optimizing the fabrication process of linear waveguide so as to maximize the evanescent field. Among waveguide materials, polysilicon is the most intensively investigated material due to its high refractive index and yet high through output which leads to low production cost [2]. Polysilicon has a refractive index that is almost equivalent to silicon wafer and the deposition of polysilicon also can be done by a low pressure chemical vapour deposition (LPCVD) system that allows a batch (25 wafers) process. A high refractive index increases the optical power capacity of the waveguide thus increasing the strength of the evanescent field, making it more sensitive to thickness of adlayer change upon binding of analyte.

However, polysilicon suffers high optical loss mainly due to the nature of polycrystallization [2]. This is caused by a grain boundary which induces a refractive index of non-homogeneity in the material and thus causes scattering loss. Due to this reason, this paper specifically is looking into methods and techniques in minimizing optical loss in polysilicon waveguide. In summary, an evanescent field biosensor provides attractive advantages such as high sensitivity for small analyte detection and a simple process for ease of handling, not forgetting real-time detection. Besides, a polysilicon waveguide that is to be used in biosensors can be fabricated using existing CMOS fabrication technology and thus reduce the production cost. A combination of both advantages gives rise to low cost and yet still provides a high sensitivity sensor that is highly useful in many applications.

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Methodology:

This section includes the details of a single-mode channel waveguide with the aim of minimizing optical power loss and maximizing the evanescent field. The single mode behaviour of a waveguide is important in the designing of an optical transducer such as, an interferometer that is used in high sensitivity biosensing application. In order to achieve single mode behaviour using polysilicon, a waveguide of width < 3μm is used with a strip waveguide design [1]. It is mainly because of its extreme high refractive index of 3.5 [1].The width in a sub-micron region causes difficulty and complexity in the fabrication process especially photolithography [2]. The main advantage of a rib waveguide is that it allows for a bigger width (~4μm) in achieving single mode behaviour. This type of waveguide is commonly used in an interferometer biosensor with a silicon based waveguide material that has a refractive index of around 2 [3].

The fabrication process is started with wafer cleaning which is needed in order to remove unwanted organic and in-organic particles on the wafer surface prior to any fabrication process. After the cleaning process, a wet oxidation process is performed so as to grow a thermally thick oxide layer that is used to isolate the penetration of optical power into the silicon wafer. Polysilicon (amorphous silicon) is then deposited on the oxide layer which is serves as waveguide material by the LPCVD process. A process known as annealing is performed on the polysilicon layer in order to improve the homogeneity of the polysilicon layer which is important since it helps reduce power loss. It is after this that, waveguide patterns are transferred with specific width to a photoresist layer by using standard photolithography and dry etching to define waveguide structure on polysilicon layer. Each fabrication processes is discussed in detail in Section III.

Optimization of Waveguide Fabrication:

a. Wet cleaning of polysilicon:

The removal of contaminants is extremely important prior to oxidation process. Cleaning steps are required because of the inevitable contamination which occurs during storage and handling and also between processing steps may be an influence to the non-uniformity of oxide thickness. Commonly, standard RCA is used to eliminate the contaminant on the silicon surface and the sequence process step is as shown in **Table 1**. Rinsing of DI water followed by a spin dry process is performed after soaking of wafer in each solution [4].

Table 1: The wafer cleaning process step [4].

Process step	Solution	Time (s)
1	RCA-1	30
2	RCA-2	30
3	BOE	10

Visual inspection with high power microscope (HPM) is performed to evaluate any abnormalities or defects on the surface of the oxide layer at the end of each cleaning process. In conclusion, wafer cleaning is primarily focused on removing particulates and contaminants as well as preparing a surface by controlling roughness.

b. Wet oxidation of polysilicon:

A silicon oxide (SiO_2) layer with approximately 1.8μm thick is grown on the silicon substrate by thermally oxidizing the silicon substrate using wet oxidation. Wet oxidation is chosen since it requires a thick oxide layer that is used to isolate the polysilicon waveguide from silicon wafer to prevent optical leakage and also because the rate of wet oxidation growth is faster than that of dry oxidation [4]. In this process, an oxidation temperature of 1100°C is used to maximize growth rate so that shorter time is used to grow thick oxide layer. Besides, flow rate of oxygen is at a maximum of 13-14 litre/min. This is to help in increase the growth rate so that a shorter time is used to grow thick oxide layer [5]. The process is repeated with certain oxidation time until the targeted thickness is achieved. **Table 2** shows rate constants for oxidation of silicon in wet oxygen. A straight line is obtained where value of A increases when temperatures decreases and value of slope B decreases when temperatures decreases [11].

Table 2: Rate constants for oxidation of silicon in wet oxygen [11].

Oxidation temperature (°C)	A (μ)	B ($μ^2$/h)	B/A (μ/h)	T (h)
1200°	0.05	0.720	14.40	0
1100°	0.11	0.510	4.64	0
1000°	0.226	0.287	1.27	0
920°	0.50	0.203	0.406	0

Oxide layer can be optimized in term thickness and thickness of non-uniformity, flatness, surface roughness and defects on the layer. Thickness and thickness of non-uniformity of SiO_2 can be affected by the local growth rate of silicon oxide on the wafer surface which is in term affected by gas flow uniformity as well as the evenness of temperature on the entire water surface. This process can be prevented by controlling the direction

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and distance of wafer surface against the oxygen flow and monitoring by use of a spectrophotometer (SPM) where SPM is used to measure the thicknesses of oxide layer.

Besides that, low flatness of the oxide layer can cause transmission loss due to non-linearity of the fabricated polysilicon waveguide, thus uniformity of oxide layer must be well controlled and this can be monitored by using SPM. Next is the surface roughness which indicates the grain on oxide layer which can be monitored using an atomic force microscope (AFM). Lastly is the defect which can influence the next fabrication process steps and it can be controlled well by performing wafer cleaning and can be monitored by using a high power microscope (HPM).

c. LPCVD of polysilicon:

Low pressure chemical vapour deposition (LPCVD) is one of the most common methods in the deposition of polycrystalline silicon or commonly known as polysilicon. Polysilicon waveguide suffers a high transmission loss compared to single crystalline waveguide. This is mainly due to the grain structure of the material. A dangling bond at the grain boundary causes absorption loss that contributes significantly to transmission loss. Thus, several methods including solid phase crystallization (SPC) of the polysilicon layer are employed to improve the grain size and surface roughness [6],these include: high temperature annealing to reduce stress [7, 8], hydrogenation passivation to passivate the dangling bond [7, 9], use of SION as a cladding layer [9]. Thin thermally grown polyoxide to reduce sidewall roughness [10, 9] had been proposed recently to reduce the transmission loss.

Among these methods, SPC which is of upmost importance had been used by all researchers that intended to fabricate low loss polysilicon waveguide. SPC is performed with LPCVD at a temperature below 560°C to form amorphous silicon. This is followed by annealing at 600°C for 15 hours to crystallize the amorphous silicon into polysilicon [2]. The result of SPC is a smooth surface roughness that contributes to lower scattering loss at a waveguide’s surface. Besides, the grain size is bigger with a lower dangling bond density that contributes to the absorption loss in polysilicon material. The process parameters of LPCVD are process temperature, total process pressure, silane partial pressure for diluted process gas and dopant concentration. Polysilicon is normally deposited at a temperature range of between 600°C and 650°C and the resulted deposition rate at this temperature range are from 100 to 200Å with the use of either pure silane or 20 to 30 percent silane diluted in nitrogen [8]. The deposition rate is linearly affected by deposition temperature. The process parameter of LPCVD is summarized in **Table 3**.

Table 3: A process parameter of the LPCVD process [8].

Parameter	Value
Pressure	0.095 Torr
LPCVD temperature	600°C
Time	20 minutes

This process can be optimized in term of thickness and thickness of non-uniformity, flatness, grain size, surface roughness and defects. The LPCVD process is a batch process with a maximum of 25 pieces of wafer which can be loaded at the same time. However, wafer spacing and load size affects wafer non-uniformity which is normally around 4 per cent. This process can be prevented by controlling the direction and distance of wafer surface. Flatness must be controlled well in this process since it can influence the waveguide and cause high transmission loss. Grain size of polysilicon layer which directly affects the resistivity of the layer is controlled by deposition temperature, dopant concentration and annealing temperature.

Deposition temperature has a negative effect while annealing temperature has positive effect on the grain size. The bigger the grain size, the lesser the grain boundary. Besides, large polysilicon grain size can cause difficulty in polysilicon sidewall etching and induce sidewall roughness. Thus, the polysilicon process is normally deposited at lower temperature to achieve smaller grain size. Only then, is the annealing process performed after the etching process to improve the grain size of polysilicon layer. Visual inspection is performed to optimize the mechanisms as stated above where thickness, thickness non-uniformity and layer flatness can be inspected by using SPM, surface roughness, grain and crystallinity can be evaluated by using AFM, defects on the surface of layer can be evaluated by using HPM.

d. Annealing of polysilicon:

Annealing is a heating process in which a wafer is heated to achieve a desired physical state with minimum material being added to or removed from the wafer surface. The purpose is to reduce the strain of polysilicon layer due to varying size of grains and to increase grain size. The annealing process of the polysilicon layer is highly dependent on the deposition conditions which affect the crystallinity of the layer. Annealing is performed to study the influence of the annealing process on the polysilicon layer. As stated in polysilicon LPCVD process, the polysilicon layer is crystallized due to high deposition temperature. Thus, low temperature

annealing for crystallization is not necessary. During the annealing process, grain size increases through intermixing of grain boundary and thus resistance of electron flow caused by grain boundary is reduced.

There are several mechanisms such as thickness, thickness non-uniformity, surface roughness, grain size, flatness and defect which can be identified and optimized as well. The thickness, thickness non-uniformity, flatness are evaluated by SPM, polysilicon film crystallization and grain size are investigated by AFM. The process parameter of the annealing process is summarized in **Table 4**.

Table 4: A process parameter of annealing process of polysilicon [2].

Parameter	Value
Loading temperature	500°C
Annealing temperature	850°C
Time	1hour

e. Photolithography of polysilicon:

To achieve high resolution, the photolithography process consists of a series of processes starting with photoresist coating, alignment of mask to silicon substrate, UV exposure of the silicon substrate and development of a photoresist to transfer the strip pattern from the mask to the silicon substrate. First, hexamethyldisilazane (HDMS) is coated and the photoresist is dispensed onto the wafer by using a spin speed as stated in Table 6. After photoresist coating, the wafer is pre-exposed to bake at 110°C for about 60seconds to remove the resist solvent and increase resist to wafer adhesion. This process decreases the resist thickness and the surface will become less susceptible to particulate contamination. After that, a waveguide mask and wafer are then exposed to UV light with an exposure time of 10seconds. Development is a critical step in photoresist process which defines the shape of resist profile and thus controlling the line width. It very much depends on the exposure time. After development, the wafer is proceeds to a hard baking process at 110°C for 90seconds. The purpose of hard baking is to strengthen the photoresists and improve the photoresist etching resistance. The temperature and time must be well controlled because under baking can cause a high photoresist etch rate and affects its adhesion to the wafer whereas over baking will cause bad resolution. The process parameter of the photolithography process is summarized in **Table 5**.

Table 5: A process parameter of the photolithography process of polysilicon.

Parameter	Value
Spin speed	1st 500 RPM for 5 seconds 2nd 3500 RPM for 20 seconds 3rd 500 RPM for 5 seconds 4th 0 RPM for 5 seconds
Soft bake	110 °C for 60 seconds
Exposure time	10 seconds
Pre- exposure bake	110 °C for 60 seconds
Hard bake	110°C for 90 seconds

The photolithography process can be optimized in term resolution, waveguide width and side walls and the defects. A high resolution is needed to achieve a completion of waveguide pattern transfer and it is the key to determine the waveguide width deviation. Generally, the thinner the photoresist film, the higher the resolution. The width of the waveguide will influence the mode of propagation thus increasing the propagation loss. Besides, the deviation of actual waveguide structure will affect the mode of propagation. Defects on the wafer surface can cause pinholes in the photoresist. The organic and inorganic contamination will cause PR adhesion problems and device defects. Therefore, it is important to eliminate the defects before the photolithography process and this can be done by using HPM for defect inspection.

f. Dry etching of polysilicon:

The etching process is required in the fabrication process for thinning of the polysilicon layer and to define waveguide structure or geometries. For etching strip waveguide structure,an extremely low etch rate is of upmost importance. Due to this reason, dry etching is chosen in this process to obtain an isotropic profile. The wafers are subsequently patterned into strips and ribs with widths of 1, 2 and 3μm and are reactive ion etched in sulphur hexafluoride (SF_6) with a combination of oxygen (O_2) to obtain the polysilicon channel waveguide [6]. The ideal process parameter of dry etching process is shown in **Table 6**.

In the dry etching process, the mechanisms control are such as etched depth, resolution, surface roughness and defects. The different structure will influence the mode of propagation. Surface roughness which is produced on the exposed sidewalls is the main challenge in dry etching process. It can increase the scattering of light and thereby the optical losses because the high refractive index contrast increases the scattering losses [5]. The mechanisms control stated above can be inspected by using SPM, AFM, and HPM.

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Table 6: A process parameter of the dry etching process.

Parameter	Strip waveguide
Dry etching method	Inductive coupled – reactive ion etching
Bias voltage	250
ICP power	650
Gas flow rate	SF_6 = 10sccm O_2 = 30sccm
Etching time	7 seconds

Prospect and Conclusion:

In this review paper, optimization of fabrication technique to the linear waveguide is presented. Optimization of the physical design of the waveguide is the main purpose to maximize the sensitivity of evanescent field and reduce the optical power loss. There are several techniques under review all in a bid to reduce the transmission loss. First is using solid phase crystallization (SPC) of the polysilicon layer to improve the grain size and surface roughness. Second is using high temperature annealing to reduce strain. Third is thermally growing a thin polysilicon oxide to reduce the sidewall roughness.

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