Proceedings of the Symposium on Computer Applications and Industrial Electronics, 2012, pages 43-47

A Firefly Algorithm approach for routing in VLSI

Abstract

Many studies had been conducted in improving the performance of large scale integration circuits that heavily depends on the interconnected routing in the circuits. Strategic choice of wire placement and buffer placement for very large scale integration (VLSI) routing can improve time delay of VLSI circuit. This paper explores the use of Firefly Algorithm in VLSI routing. The location of doglegs is employed to model the firefly that represents the routing solution. The proposed approach is then compared with previous literature for benchmarking. The result indicates that it has a good potential in VLSI routing and can be further extended in future.

Keywords — Buffer insertion, firefly algorithm, interconnect, routing, swarm intelligence.