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The Effect of Gap between Plastic Leaded Chip Carrier (PLCC) Using Computational Fluid Dynamic (CFD) Software, FLUENT^{TM}

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ABSTRACT

This paper presents the effect of gap between Plastic Leaded Chip Carrier (PLCC) by using three dimensional numerical analysis of heat and fluid flow in computer. 3D model of microprocessors is built using GAMBIT and simulated using FLUENT software. The study was made for twomicroprocessors arranged in line under different types of inlet velocities and package (chip) powers. The results are presented in terms of average junction temperature and thermal resistance of each package. The junction temperature is been observed and it was found that the junction temperature of the microprocessors is not exceed 70º C. It also found that the gap between PLCC play important rolesto control and manage the junction temperature. The strength of CFD software in handling heat transfer problems is proved to be excellent.

INTRODUCTION

Nowadays, the major trend in electronic industry is to make the products smarter, lighter, and highly compact, at the same time can reduce the heat of electronic component. This trend has necessitated stringent packaging requirements is a promising option to tackle this issue. However, a serious issue in electronic packaging is the thermal management. The electronic components made using silicon chip and the organic substrate, which generates heat and causes malfunction for some electronic components when the temperature above 70ºC. This problem is effectively solved by control the gap between PLCC. Two PLCC used in this simulation and been tested in mini wind-tunnel and air inlet velocity used as cooling device. Three types of arrangement were made in order to verified the suitable gap used between PLCC start with 0 cm, 1.5 cm and 3.0 cm. In normal case, when electronic components operate in long period, the temperature of chip in electronic components will easily exceed 70ºC.This will cause electronic components malfunction or overheated. That why there are a lot of researchers doing study on thermal management over 30 years ago.

In electronic industries, the continuing increase of power densities in microelectronics and simultaneous drive to reduce the size and weight of electronic products have led to the increased importance of thermal management issues in electronic industry. The temperature at the junction of an electronic package has become the important factor that determines the lifetime of the package. The thermal management had been started over 30 years ago. Initially, the studied had been conducted by experiment only. The heat transfer and pressure drop for airflow in arrays of heat generating rectangular module had been studied by Sparrow [1]. Later Sparrow [2] made an experimental investigation of heat transfer and fluid flow characteristics of arrays of heat-generating block-like modules affixed to one wall of a parallel-plate channel and cooled by forced convection airflow. They also investigated the convective heat transfer response to height differences in an array of block-like electronic components. Gupta and Jaluria [3] carried out experiments to study forced convection water cooling of arrays of

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protruding heat sources with specified heat input. Hwang [4] investigated forced convection from discrete heat sources mounted flush on a conductive substrate in a rectangular duct. Molki and Faghri [5] made an experimental investigation of forced convection air-cooling of a 4 by 3 copper rectangular block positioned along the lower wall of the test section in an in-line arrangement. Ramadhyani, Moffat and Incropera [6] made a 2D numerical study on the conjugate analysis of forced convection heat transfer from discrete heat sources mounted on a solid substrate and exposed to fully developed laminar flow. Davalath and Bayazitoglu [7] considered a conjugate heat transfer for two-dimensional, developed flow over array rectangular blocks representing finite heat sources on parallel plate using the cooling fluid as air.

Utilization of CFD as thermal prediction tool was employed by Plotnik and Anderson [13] and Tucker and Paul [12] as part of design for heat transfer enhancement in electronic devices. The laminar and the turbulent forced convective flows over two sequentially heated blocks mounted on one principal wall of a channel were experimentally and numerically studied by Chen and Wang [11]. Hong and Yuan [10] proved that a constant and uniform heat transfer coefficient across the whole package was inadequate in the accurate prediction of thermal stresses, due to the significant effect of local temperature distribution resulted from the variation of local heat transfer coefficient. Thus, they demonstrated the importance of considering the conjugate problem for electronic packages. Jayakanthan *et al.* [17] carried out simulations of conjugate heat transfer associated with single and two packages mounted on printed circuit board (PCB) which was situated in a wind tunnel, using FLUENT^{TM} for various flow conditions. This work was numerical investigation of heat transfer in plastic leaded chip carrier continued by Huat [19] who simulated multiple chips using a 2D model. Hung and Fu [10] designed a two-dimensional model for numerical prediction of viscous laminar flow, mixed convection and conjugated heat transfer between parallel plates with uniform block heat source and with opening on the integrated circuit board. The interest in the determination of junction temperature and thermal resistance continued to grow as is evident from the works of Tso *et al.* [14], Young and Vafai [15], and Kim and Kim [16].

In year 2007, the development of electronic industries increase rapidly because development of electronic packaging and nanotechnology. Yusof *et al.* [24] has studied the PLCC packaging by using 2 PLCC in the PLCC packaging. After that, the studied about electronic packaging about PLCC has been improved by Mazlan *et al.*. Accordingly, the present study is focused on simulations of the effect between PLCC packages by using several inlet air velocities with different chip powers. Factors affecting the chip temperature such as coolant velocity, chip power and gap between PLCC are studied and presented.

2.2 Description of Model:

The model used in this simulation consists of a wind tunnel which encompasses the whole computational domain with a motherboard and 2 PLCC. The plan view of the simulation setup for 2 PLCC packages are shown in Figure 1. The motherboard (PCB) is set up 12 cm from the inlet of wind tunnel to make sure that the flow is fully developed when it reaches the outlet of the wind tunnel. The 4 PLCC packages, each having 2 cm × 2 cm face were mounted with three types differences of gaps between PLCC in a symmetrical manner as show in Figure 1. The setup is kept at a height of 7 cm from the bottom surface of the wind tunnel. The motherboard thickness is 0.015 cm and the thickness of chips is 0.3 cm each.

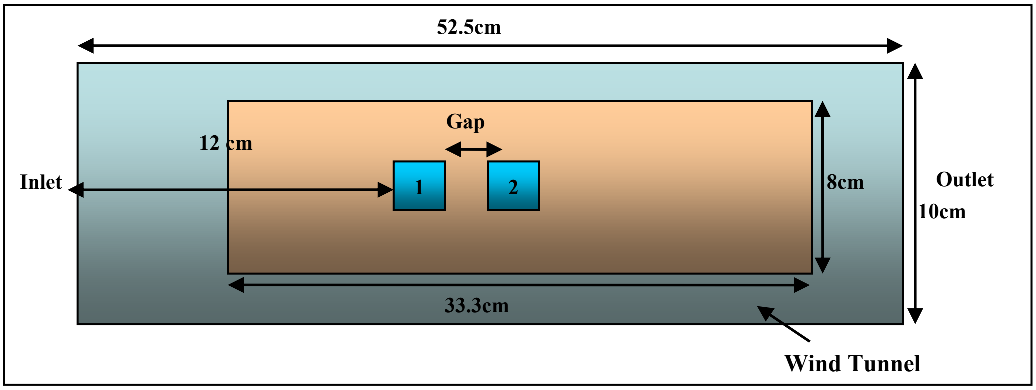


Fig. 1: Simulation Setup for 2 PLCC Packages.

Table 1: Dimension of Components Used in Simulation.

Component	Quantity	Size (cm^3)
Wind tunnel	1	52.5 cm × 10 cm × 10 cm
Motherboard	1	33.3 cm × 0.15 cm × 8 cm
Chip	2	2 cm × 0.3 cm × 2 cm
Gap	3	0 cm, 1.5 cm and 3.0 cm

RESULTS AND DISCUSION

The results are presented in terms of average junction temperature and thermal resistance for the packages under different operating conditions. The results of PLCC are comparable betweenthree types of gap where 3-D analysis of the heat and fluid flow are similar and having same model dimensions. The effect of gaps enableto control and at the same time was able to decrease junction temperature for each PLCC packages with different values of input velocity.

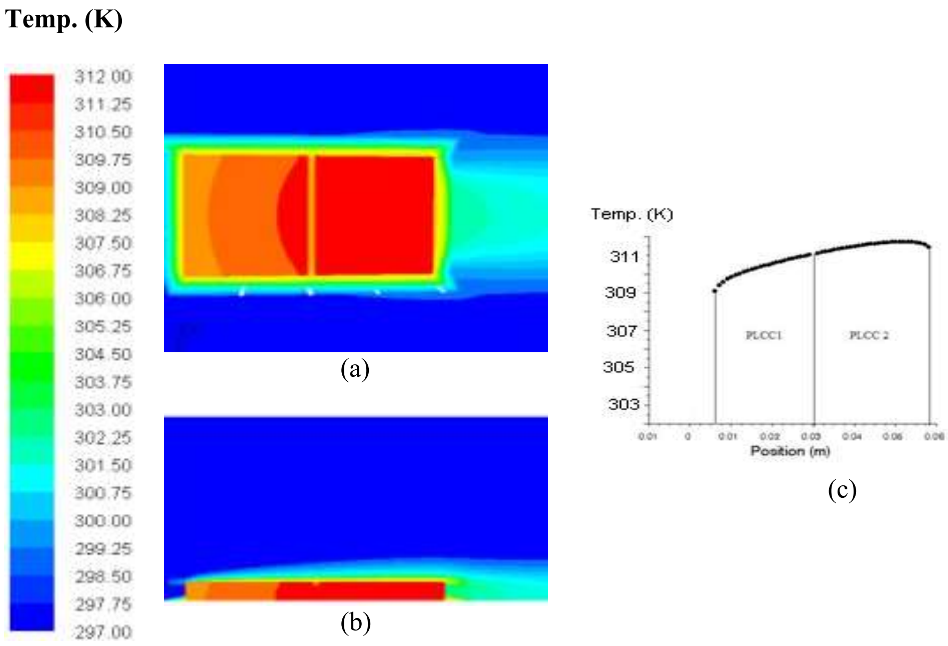


Fig. 2: Contour of the Junction Temperature of the PLCC at Reynolds number 177 for the power of 0.5 W for a distance of 0 cm,
(a) The contour of the top view, (b) contour side view, (c) plot of temperature versus position

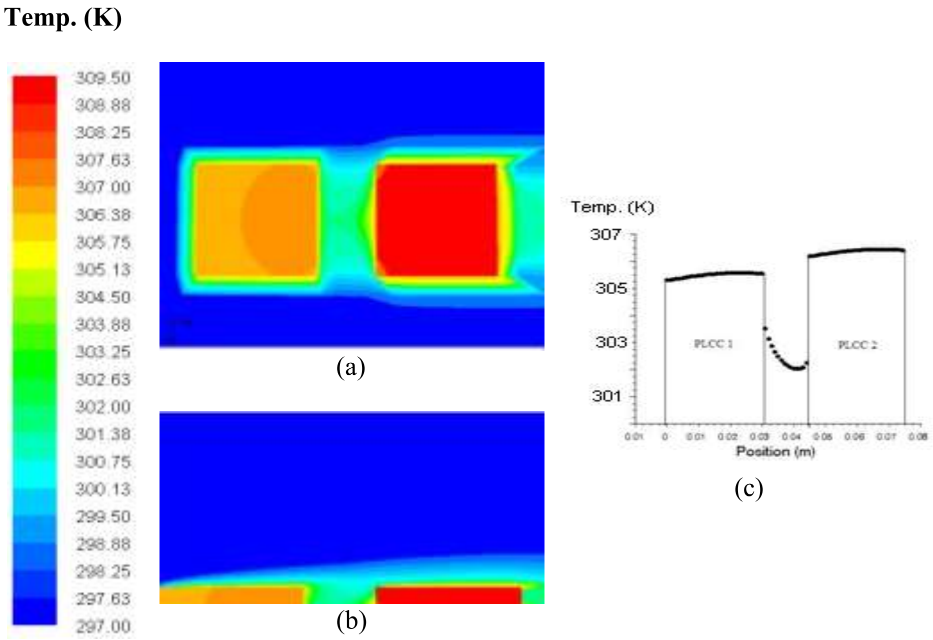
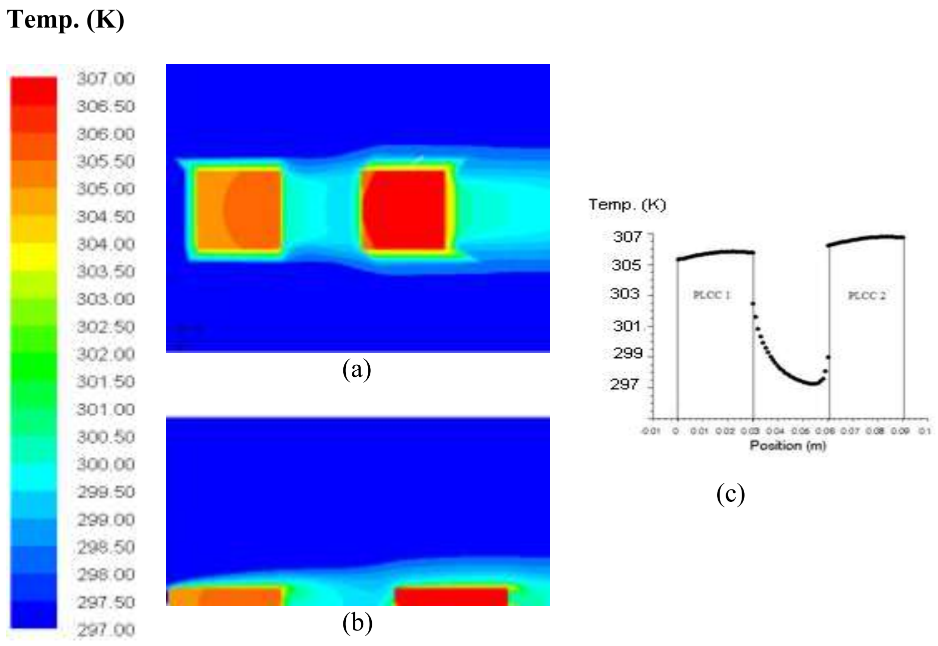


Fig. 3: Contour of Junction Temperature of the PLCC at Reynolds number 177 for the power of 0.5 W for a distance of 1.5 cm,
(a) The contour of the top view, (b) contour side view, (c) plot of temperature versus position



(a)

(b)

(c)

Fig. 4: Contour of the Junction Temperature of the PLCC at Reynolds number 177 for the power of 0.5 W for a distance of 3 cm,
(a) The contour of the top view, (b) contour side view, (c) plot of temperature versus position

3.1 The Effect of gap between PLCCon average Junction Temperature by Using CFD Software:

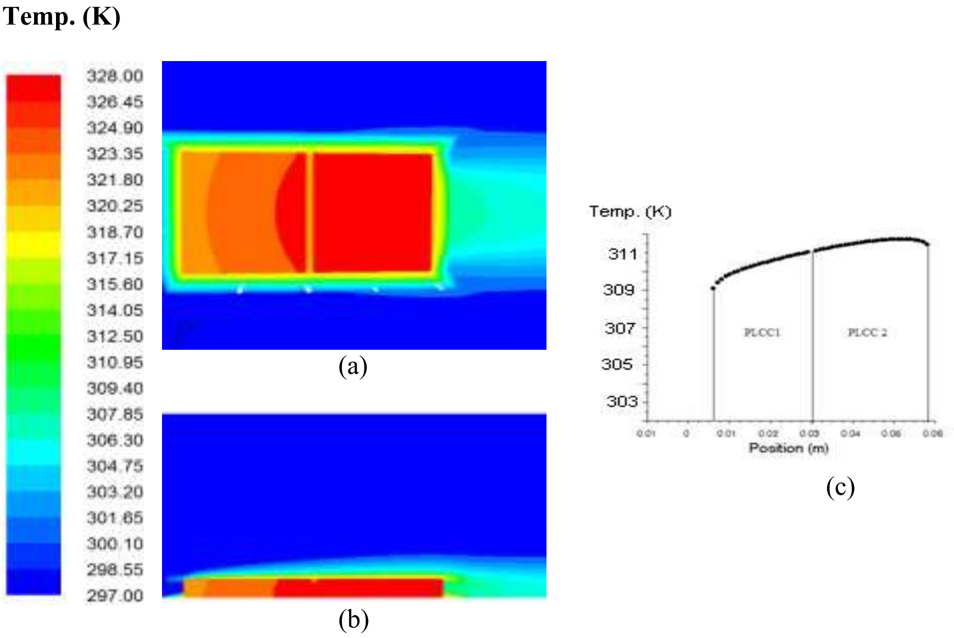
3.1.1 Chip Power 0.5W:

The effect of gaps between PLCC proves to be an effective method to reduce the junction temperature for all PLCCs. The result above has shown the contour of junction temperature between the PLCC using different gaps. The gap between PLCC at 3.0 cm was able to reduce the junction temperature of the PLCC 20.54 % compare with the gap at 0 cm. Gap 3.0 cm between PLCC has the lowest junction compared to the others because the heat can disperse more easily without any disruption from other PLCC due to the limit space. The same parameters were used in this simulation, where the air inlet velocity used starts from 0.01 m/s until 2 m/s.

Figure 2-5 summarizes the junction temperature for all air inlet velocities and differences of gap between the PLCC. It shows the differences between junction temperatures at 2 PLCCs using the gap between PLCCs at 0 cm, 1.5 cm and 3.0 cm at air inlet velocities 0.01 m/s to 2 m/s. The maximum percentage of temperature difference between gap 0 cm and 3.0 cm is 20.54% and the maximum temperature for the PLCC is 38.84 ºC at gap 0 cm. These three types of gap have the same pattern where the increasing chip power and in the decreasing gap between the PLCC will increase the junction temperature. The gap between the PLCC at 3.0 cm has the lowest junction temperature because the heat transfer between the PLCC has the least effect caused by the distance. The distance 3.0 cm is the ideal distance because the further increase of the gap between the PLCC does not carry much effect and it will only reduce the junction temperature to be less than 2%. The gap between the PLCC is unable to consume more space due to the space being very limited in electronic components.

3.1.2 Chip Power 1 W:

The result below showed the contour of junction temperature between the PLCC using different gaps at chip power 1 W. The gap between PLCC at 3.0 cm was able to reduce the junction temperature of the PLCC from 25.47%compare with the gap at 0 cm. Gap 3.0 cm between PLCC has the lowest junction compared to the others because the heat can disperse more easily without any disruption from other PLCC due to the limit space. The same parameters were used in this simulation, where the air inlet velocity used starts from 0.01 m/s until 2 m/s. The chip power for the PLCC used is 1 W differs from previous ones.

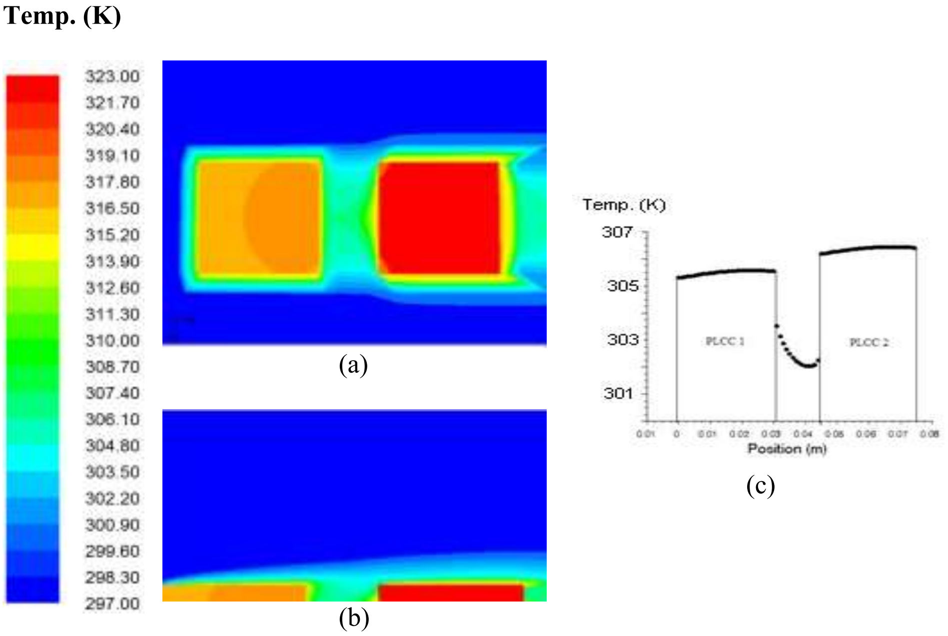


(a)

(b)

(c)

Fig. 6: Contour of the Junction Temperature of the PLCC at Reynolds number 177 for the power of 1 W for a distance of 0 cm,
(a) The contour of the top view, (b) contour side view, (c) plot of temperature versus position

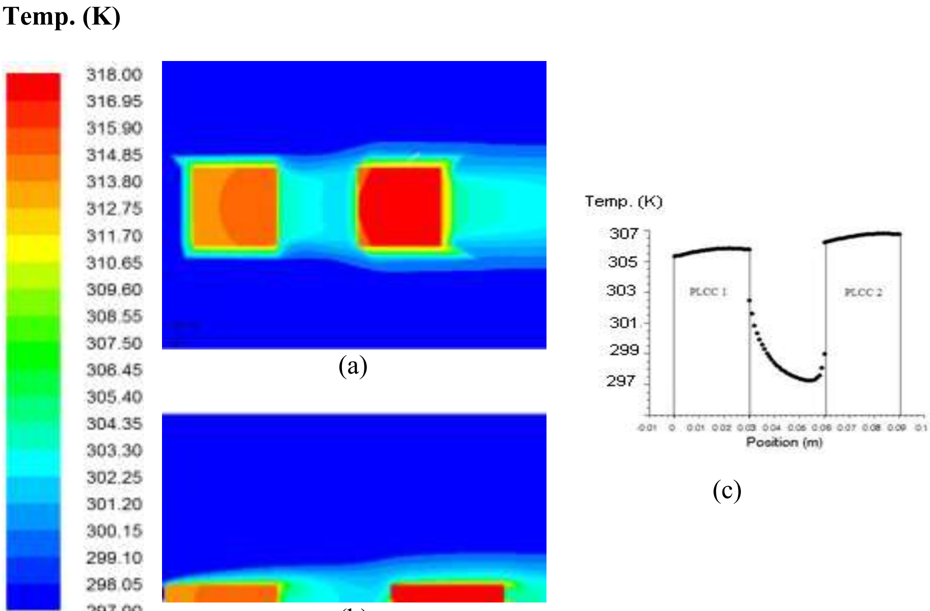


(a)

(b)

(c)

Fig. 7: Contour of Junction Temperature of the PLCC at Reynolds number 177 for the power of 1 W for a distance of 1.5 cm,
(a) The contour of the top view, (b) contour side view, (c) plot of temperature versus position



(a)

(b)

(c)

Fig. 8: Contour of the Junction Temperature of the PLCC at Reynolds number 177 for the power of 1 W for a distance of 3 cm,
(a) The contour of the top view, (b) contour side view, (c) plot of temperature versus position

Conclusion:

From the results above, it shown that the junction temperature of PLCCsdecreases with increasegap between PLCC. The maximum percentage of temperature difference between gap 0 cm and 3.0 cm is 20.54% and the maximum temperature for the PLCC is 38.84 ºC at gap 0 cm. These three types of gap have the same pattern where the increasing chip power and in the decreasing gap between the PLCC will increase the junction temperature. The gap between the PLCC at 3.0 cm has the lowest junction temperature because the heat transfer between the PLCC has the least effect caused by the distance. The distance 3.0 cm is the ideal distance because the further increase of the gap between the PLCC does not carry much effect and it will only reduce the junction temperature to be less than 2%. The gap between the PLCC is unable to consume more space due to the space being very limited in electronic components.

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