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Development of Nano-Material (Nano-Silver) in Electronic Components Application

[1,2,3]M. Mazlan, [2]Anizah Kalam, [2]Abdullah, N.R., [2]Huck-Soo Loo, [3]A.M. Mustafa Al Bakri, [4]M.S. Abdul Aziz, [4]C.Y. Khor, [5]Mohammad Amizi A., [1]Mohd Sukhairi, M.R.

[1]*Faculty of Earth Science, University Malaysia Kelantan Campus Jeli, 17600Jeli Kelantan, Malaysia*
[2]*Faculty of Mechanical Engineering, UiTM Shah Alam, 40000 Shah Alam, Selangor, Malaysia*
[3]*Center of Excellence Geopolymer & Green Technology (CEGeoGTech) School of Materials Engineering University Malaysia Perlis*
[4]*School of Mechanical and Aerospace Engineering, Engineering Campus, University Sains Malaysia, 14300 Nibong Tebal, Penang, Malaysia*
[5]*Faculty of Agro-Based Industry, University Malaysia Kelantan Campus Jeli, 17600 Jeli Kelantan, Malaysia*

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A B S T R A C T

This paper presents the development of nano-material in electronic components especially in Plastic Leaded Chip Carrier (PLCC) application. The effect of nano-material in Plastic Leaded Chip Carrier (PLCC)will improve thermal resistance as well thermal performance in electronic application. This research is using three dimensional numerical analysis of heat and fluid flow in computer and3D model of microprocessors is built using GAMBIT and simulated using FLUENT software. The study was made for severalmicroprocessors arranged in line under different types of material, inlet velocities and package (chip) powers. The results are presented in terms of average junction temperature and thermal resistance of each package. The junction temperature is been observed and it was found that the junction temperature of the microprocessors is not exceed 70º C. It also found that the application of nano-material in PLCC play important rolesto control and manage the junction temperature. The strength of CFD software in handling heat transfer problems is proved to be excellent.

INTRODUCTION

Traditional electronic circuits are built by etching individual components into silicon wafers [1]. The commercialization of integrated circuits (IC) and the creation of the microelectronics industry began in 1965 using the silicon processing technology [5]. Over time, there is an ever-increasing progress in the technology being used and, in parallel, a progressive reduction in the size of circuits. Such rapid technological progress was first predicted in 1965 by Gordon Moore in the now famous 'Moore's Law', which states that the integrated circuit density and performance would double every 18 months. This has broadly held true, as the improvements are being brought about by reduced transistor dimensions, increased transistor counts and increased operating frequencies [3].

Circuits have reduced in size over the years to such an extent that current generations of chips may carry circuits only 65 nm wide and more than a million transistors on a single piece of silicon a few millimeters across [9]. The field effect transistor (FET) was first scaled below 100 nm in the year 2000, inaugurating the era of silicon nano-electronics (Gargini, 2004). The term 'nano-electronics' (or referring to the circuit dimension that is less than 100 nm) can now be used instead of the 'microelectronics'. Presently, 65nm and 90nm process technology is being used to manufacture chips (see list of products below). According to the company Intel, the next two process generations, 45 nm and 32 nm, are due to be produced in 2007 and 2009 respectively. Intel is now producing more than half of its mobile, desktop and server microprocessors using 65 nm process technologies [6]. While the manufacture of chips described above uses nanotechnology, it does not use nano-materials in the sense of free or bound nano-particles. However, these nano-materials are also being used in

Corresponding Author: M. Mazlan, Faculty of Earth Science, University Malaysia Kelantan Campus Jeli, 17600Jeli Kelantan, Malaysia
E-mail: mazlan.m@umk.edu.my

electronics. Some of the most common nano-materials being investigated and used are carbon nano-tubes, quantum dots, and nano-silver particles [2].

2.0 Method:

2.1 Experimental Procedures on PLCC Setup:

In the experiments conducted, the layout of the apparatus was arranged as the layout of the simulation to ensure the effectiveness and accuracy of results. The arrangement of the apparatus has been developed to measure the temperature distribution in each PLCC for the three types of layout brackets to PLCC packages for 4 PLCCs. The arrangement of the apparatus is shown in figure 2.1 and figure 2.2. The figures show the arrangement of the specimens in the specified position as the experiment was carried out. During the experiments, the specimen was placed near the mini wind tunnel to facilitate the experiments performed. The measurement of the mini wind tunnel is 1.5 m x 1.5 m x 1.5 m and is used during the test to provide air flow to the site of the experiment.

The mini wind tunnel developed by Fazli [4] is used to supply the turbulent flow regime. Later on, the mini wind tunnel is developed and modified by Sharipudin [8]. A convergent nozzle made of aluminium is used to supply air flow to the specimen. Meanwhile, a honeycomb is placed in front of the airflow to ensure that the airflow moves in a straight line. In order to improve the air flow profile, the air barrier is used. Digital transformer is used to control a three-phase axial fan which is used to control the air velocity. Mini wind tunnel is capable of supplying air velocity of 15 m/s. The value of the air velocity readings were measured using a digital flow meter. In this study, the wind velocity values used are from 0.01 m/s to 2 m/s.

In this experiment, the PLCC had been replaced with stainless steel heater caused by the difficulty of supplying electricity to a single PLCC. The PLCC used is rectangular and its dimensions are 3.0 cm x PLCC 3.0 cm x 0.3 cm, more or less similar to the shape and dimensions of the real PLCC. AC current power supply was used in the PLCC for controlling power supply to the PLCC. Power supplied to the PLCC is 0.5 W, 1.0 W and 2.0 W. From experimental observations, a very high temperature in the PLCC causes heat loss through the platform. This phenomenon is causing the error between simulated and experimental results to increase. Figure 2.2 show the schematic diagram of the apparatus set up for the PLCC layout. In addition to the different strengths of the electrical power, this study also investigates the effect of wind velocity and type in a different layout of the heat transfer coefficient.

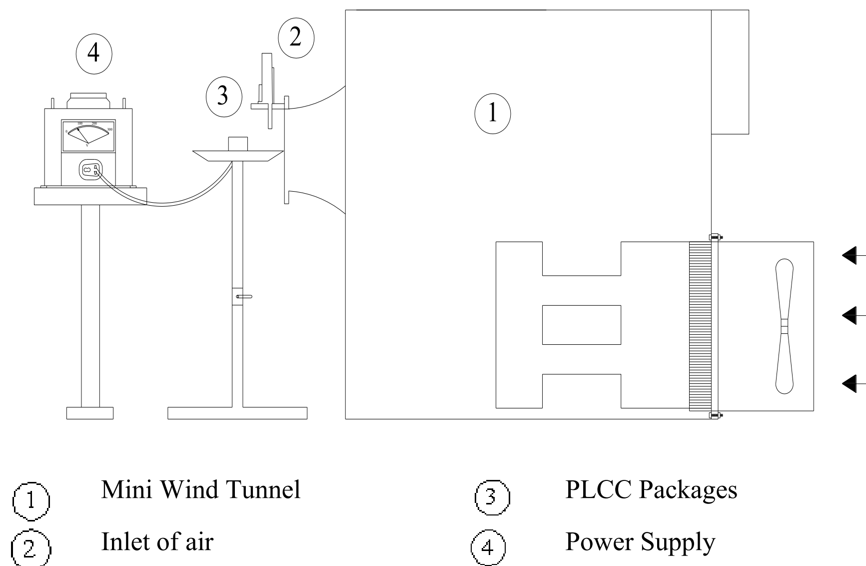

Fig. 2.1: Schematic diagrams for the experimental setup.

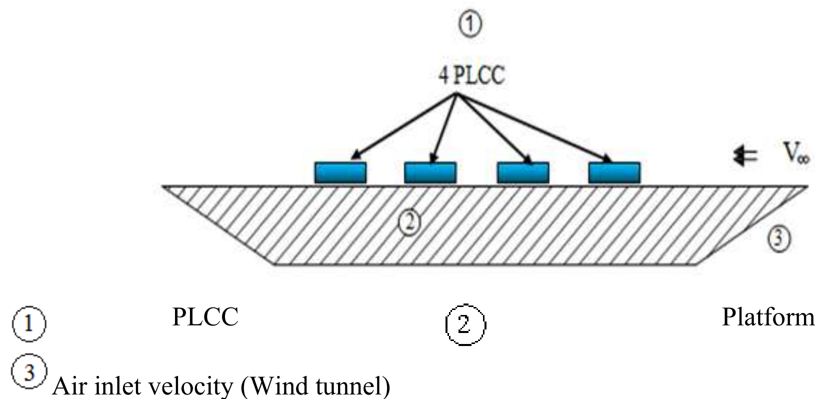

Fig. 2.2: Schematic diagram for 4 PLCCs at 45° platform.

2.2 Simulation Procedures on PLCC Setup:

It was one of the most important tasks in numerical modeling to choose the types of grids to be employed, as they determine the effectiveness of the solution in terms of the computational cost and solution accuracy. CFD simulations with structured grids might give faster solutions compared to unstructured grids, but it is usually not possible to generate structured grids for complex geometries or for CFD models with complicated movement. Structured grids yield more accurate results in most cases, but this is not possible for complex and dynamic cases. Alternatively, a hybrid mesh may be used for such cases so as to improve the mesh quality. The quality of the mesh plays a significant role in the accuracy and stability of the numerical computation.

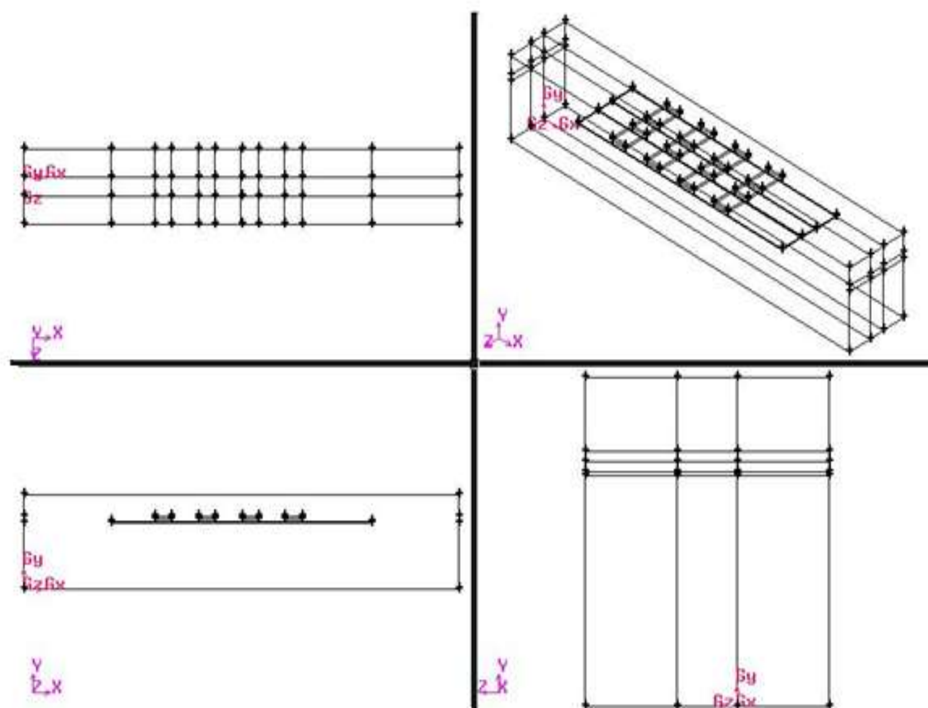

Fig. 2.3: The computational model for four PLCC packages.

The generated model is ready to be meshed. Three dimensional structured meshes are used for the flow simulation in the four packages. The three-dimension structure mesh (hexagonal) has been created at all sections in the simulation as shown in Figure 3.17. The size of the grid element is set according to the interval size where a small interval size will result in finer meshing. The grid size are 200x40x52 which is corresponding to the number in x, y and z axis or also known as i, j and k axis. Total elements of the model are 416,000 nodes.

RESULTS AND DISCUSION

The results are presented in terms of average junction temperature and thermal resistance for the packages under different operating conditions. The results of PLCC are comparable betweentwo types of material usedwhere 3-D analysis of the heat and fluid flow are similar and having same model dimensions. The effect of material in PLCCenableto control and at the same time was able to decrease junction temperature for each PLCC packages with different values of input velocity.

3.1 The Effect of material applied in PLCCin term of average Junction Temperature by Using CFD Software:

3.1.1 Chip Power 0.5W:

The aim of this study is to show and study the effect of material of PLCC. The need to improve the thermal management is very important to ensure that the electronic components' temperature does not exceed 70 ºC. The electronic components that exceed 70 ºC will tend to overheat and cause damage to the components. Figure 3.1 shows the contour of the total temperature for 4 PLCCs at 0.5W for velocity 0.1 until 2 m/s. Figure3.1 and Figure 3.2 shows the tabular and graphical representations respectively.

3.1.2 Chip Power 1 W:

The power of the chip has been increased from0.5 W to 1 W in order the see the differences and changes of the junction temperature of the PLCC. The same air inlet velocity had been used in this simulation starting from 0.01 m/s until 2 m/s. Figure 3.3 and 3.4 below shows the contours of the junction temperature for 2 PLCCs at 1 W using the air inlet velocity from 0.01 m/s to 2 m/s.

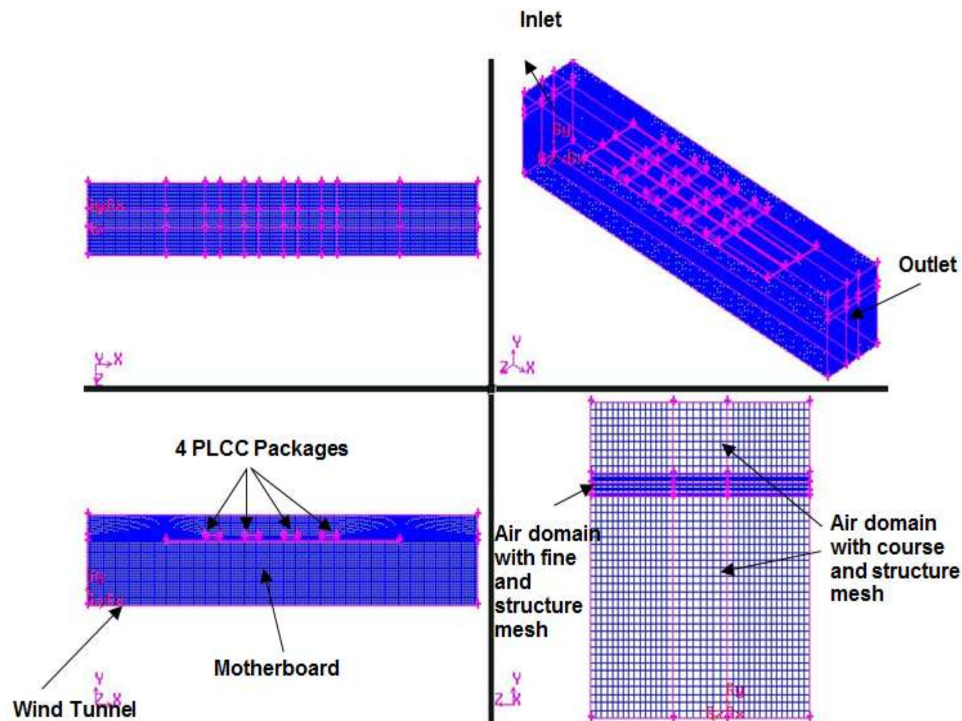

Fig. 2.4: Computational domain of 3-D model and volume mesh of four PLCC Packages.

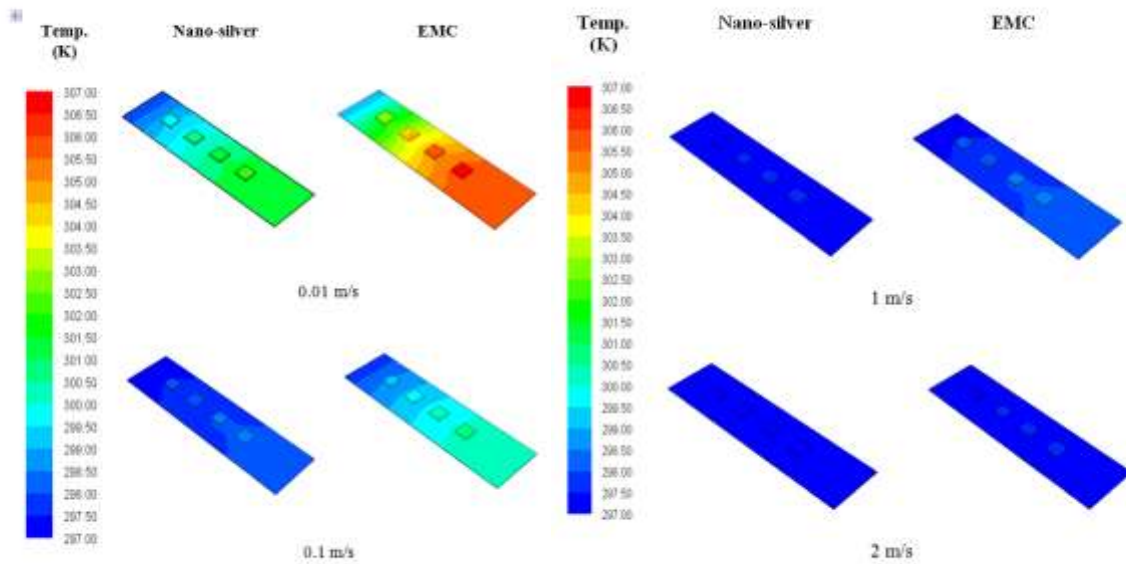

Fig. 3.1: Contours of the junction temperature (K) for 4 PLCCs at 0.5 W for 0.01 m/s, 0.1m/s, 1 m/s and 2 m/s for nano-silver and EMC material.

3.1.2 Chip Power 2 W:

Finally, the power of the chip has been increased from1 W to 2 W in order the see the differences and changes of the junction temperature of the PLCC. The same air inlet velocity has been used in this simulation starting from 0.01 m/s until 2 m/s. Figure 3.5 and 3.6 below shows the contours of the junction temperature for 2 PLCCs at 2 W using the air inlet velocity from 0.01 m/s to 2 m/s.

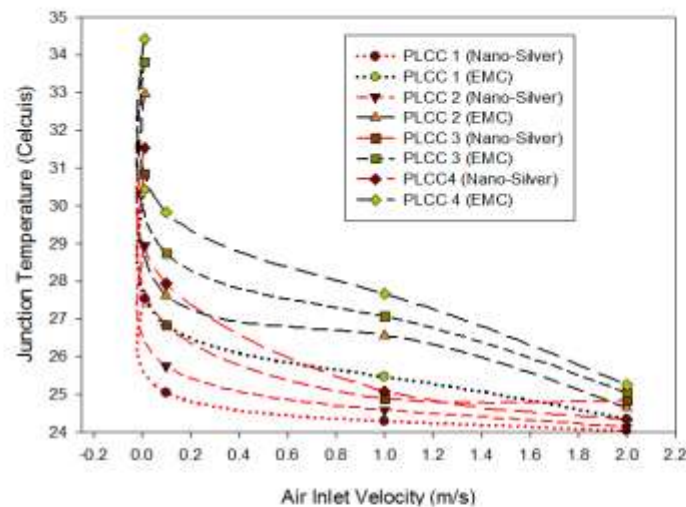

Fig. 3.2: The Comparison of Junction Temperatures for 4 PLCC and 0.5W between Nano-Silver and EMC.

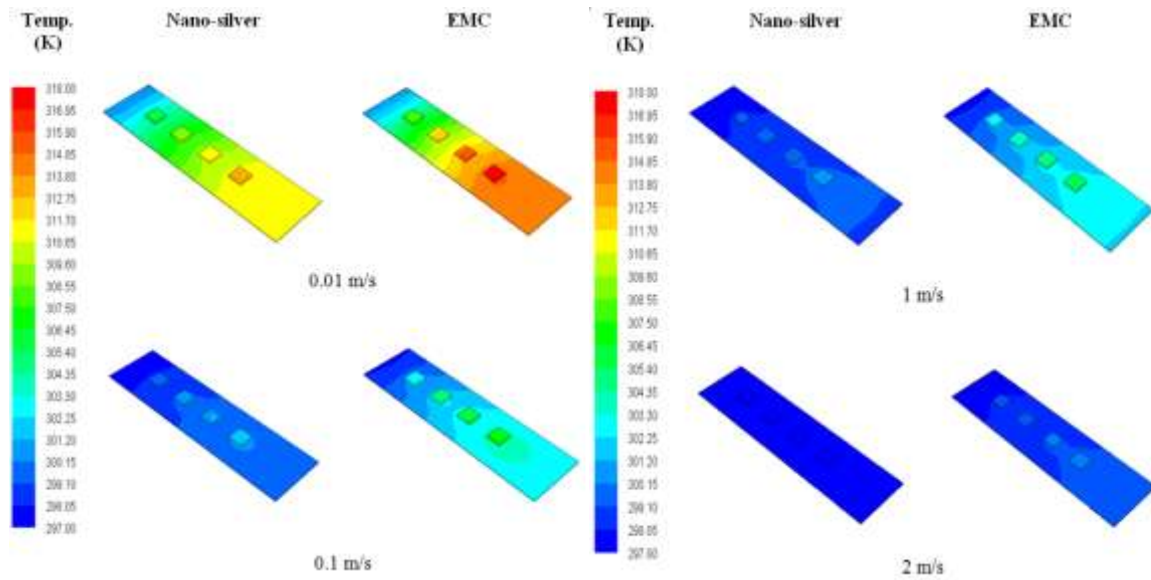

Fig. 3.3: Contours of the junction temperature (K) for 4 PLCCs at 1 W for 0.01 m/s, 0.1m/s, 1 m/s and 2 m/s for nano-silver and EMC material

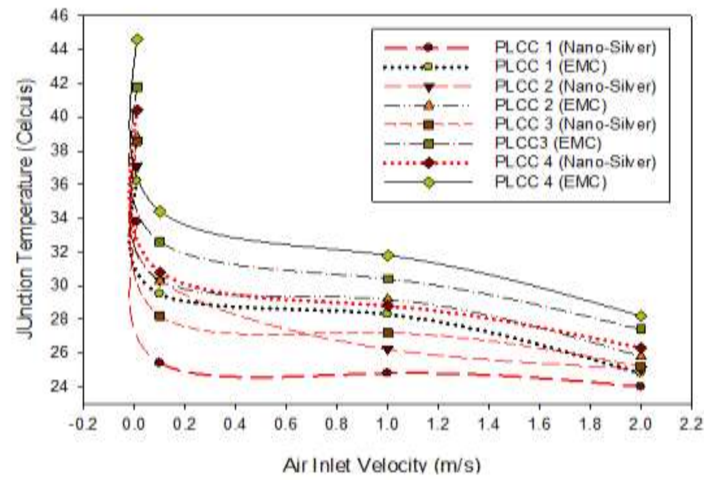

Fig. 3.4: The Comparison of Junction Temperatures for 4 PLCC and 1 W between Nano-Silver and EMC.

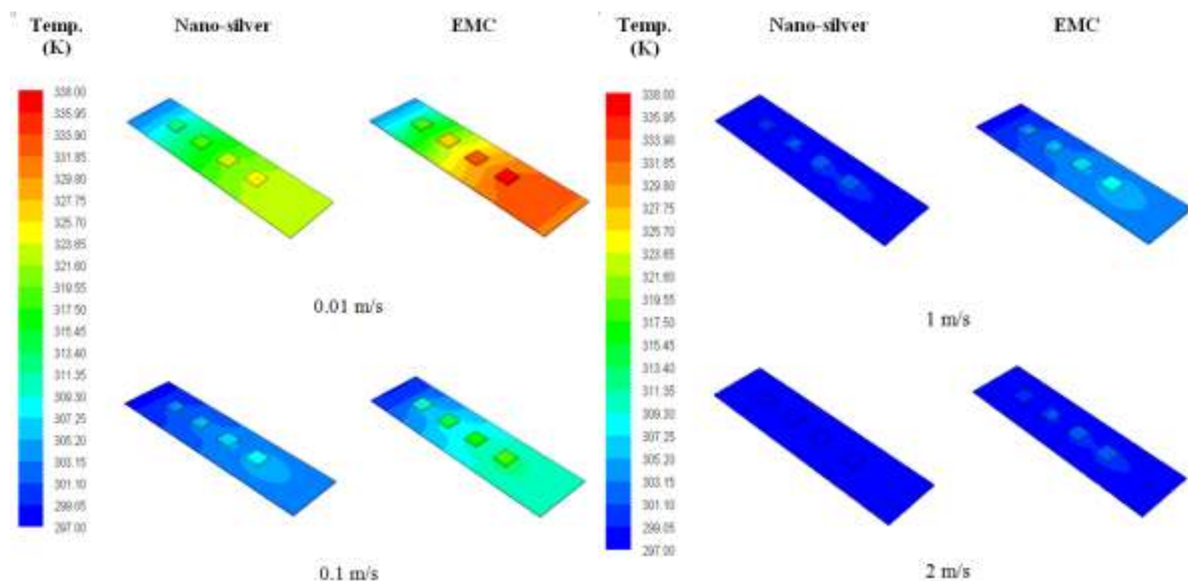

Fig. 3.5: Contours of the junction temperature (K) for 4 PLCCs at 2 W for 0.01 m/s, 0.1m/s, 1 m/s and 2 m/s for nano-silver and EMC material

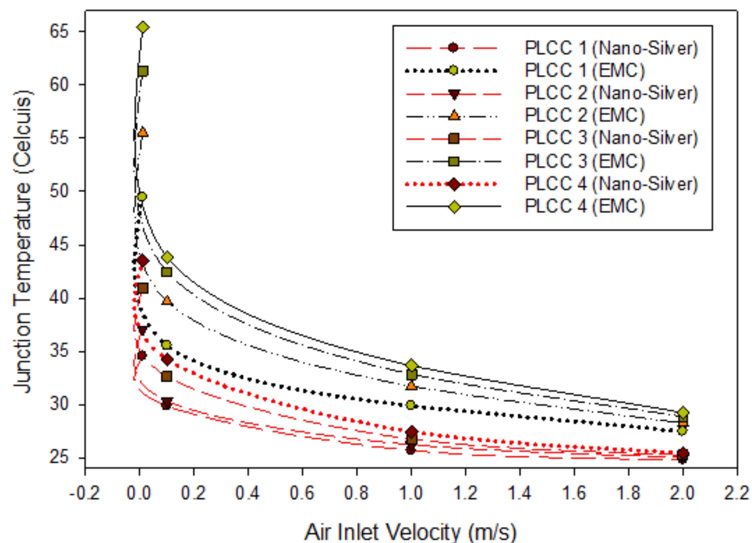

Fig. 3.6: The Comparison of Junction Temperatures for 4 PLCC and 2W between Nano-Silver and EMC.

Conclusion:

From the results above, the differences between the junctions temperatures at all PLCCs by using the EMC and nano-silver at 2 W are shown. The maximum percentage of differences between the EMC and nano-silver is 33.46% and the maximum temperature is 65.42 ºC. The differences between the EMC and nano-silver at PLCC 1 are 30.18%, 15.96%, 14.06% and 9.69% respectively. Meanwhile, the differences at PLCC 2 are 33.21%, 23.58%, 17.34% and 11.40% respectively. For PLCC 3, the differences between the junction temperatures between the EMC and nano-silver are 33.27%, 23.14%, 18.57% and 12.51% respectively. Finally, at PLCC 4 the differences between the EMC and nano-silver in terms of the junction temperature are 33.46%, 21.86%, 18.45% and 13.00% respectively.

From the results above, it has been shown that the junction temperature for all PLCCs increases due to the increase in the chip power from 1 W to 2 W. The maximum temperatures of the PLCC also rise to 65.42 ºC from 44.60 ºC. The PLCC made of the nano-silver was able to reduce the junction temperature more than 30% in comparison with the EMC.

The results have further shown that the junction temperature for the PLCC made of nano-silver has less value of junction temperature compared to the epoxy moulding compound (EMC) because the properties and thermal conductivity of nano-silver perform better than the epoxy moulding compound (EMC). Besides that, all figures show that the temperature distribution is not uniform at all PLCCs because of the fact that the heat dissipated and dispersed during the air flow through the PLCC. Generally, the results obtained show that the temperature at the front of the PLCC is lower than the PLCC in the back. This phenomenon is caused by the wind flow that will go through the front side of the PLCC first and then the wind flow will travel to the next PLCC. As a result, the PLCC's junction temperature at the back is higher than the PLCC in the front because of the wind resistance at the front side of the PLCC will reduce the air inlet velocity.

The above results show that the junction temperature of each chip decreases with the increase in the inlet velocity, at a constant chip power. The junction temperature for PLCC 1 is the lowest compared to the other packages, whereas PLCC 4 has the highest junction temperature. This phenomenon happens due to the flow resistance that is present as the air passes over successive PLCC packages. In the simulation model, the arrangement of the packages begins with the PLCC 1 located in front of the motherboard followed by PLCC 2, 3 and 4. This makes the inlet air velocity minimized for PLCC 4 and hence the maximum junction temperature is obtained.

A similar trend was observed in relation to the average junction temperature and velocity at chip powers, 1W and 2W but the temperatures were increasing with the increase of the chip power for all inlet velocities. Figure 4.11 show the tabular illustrations of the increase of the junction temperature with chip power at all inlet velocities for 4 PLCC. The increased temperature at higher chip powers may be attributed to the higher rate of heat generation. Nonetheless, this raise in temperature could be controlled at higher velocities. Here, an inlet velocity of minimum 2 m/s is acceptable at chip power 2W, 1m/s is for 1W and even lesser for 0.5W.

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