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DS89C450
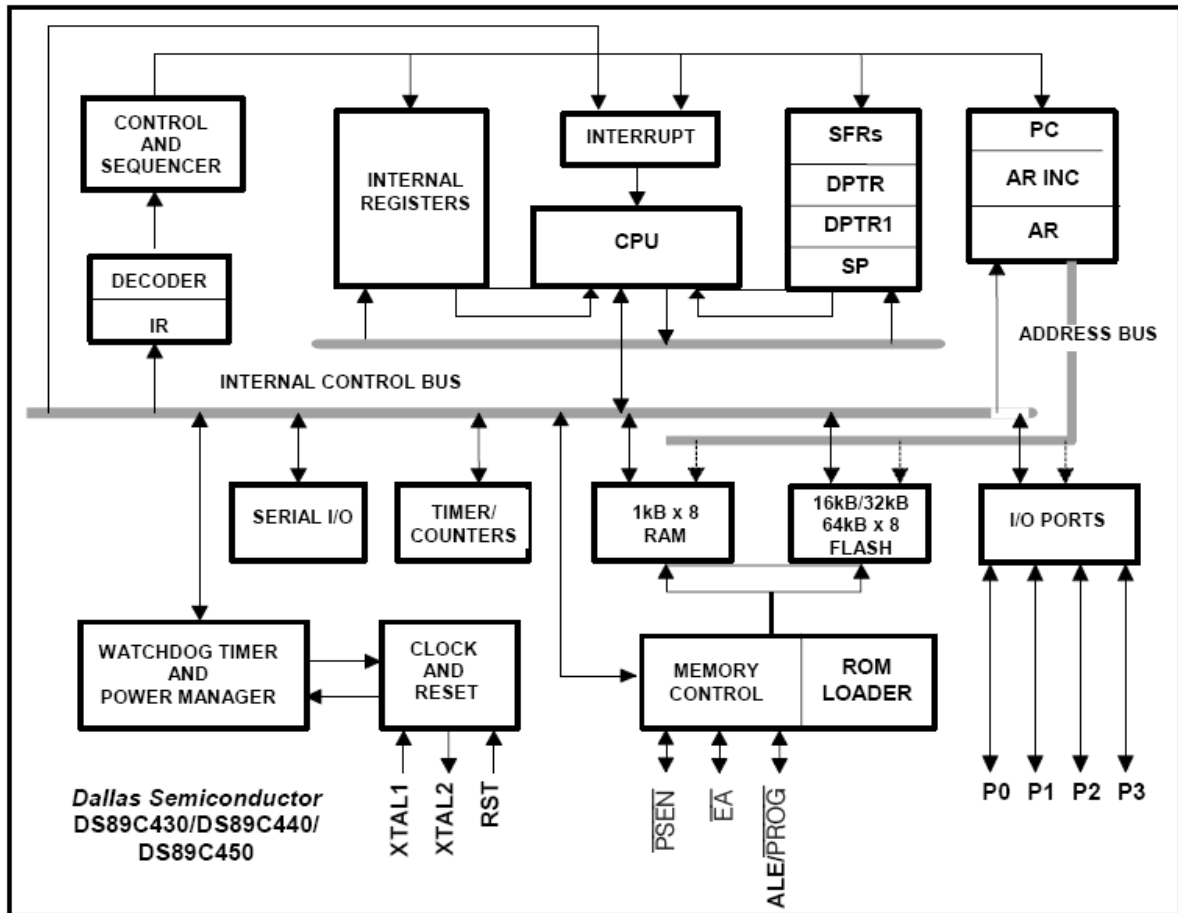## Ultra-High-Speed Flash Microcontrollers

MAXIM

FEATURES

- **High-Speed 8051 Architecture**
  One Clock-Per-Machine Cycle
  DC to 33MHz Operation
  Single Cycle Instruction in 30ns
  Optional Variable Length MOVX to Access
      Fast/Slow Peripherals
  Dual Data Pointers with Automatic
      Increment/Decrement and Toggle Select
  Supports Four Paged Memory-Access Modes

- **On-Chip Memory**
  16kB/32kB/64kB Flash Memory
  In-Application Programmable
  In-System Programmable Through Serial Port
  1kB SRAM for MOVX

- **80C52 Compatible**
  8051 Pin and Instruction Set Compatible
  Four Bidirectional, 8-Bit I/O Ports
  Three 16-Bit Timer Counters
  256 Bytes Scratchpad RAM

- **Power-Management Mode**
  Programmable Clock Divider
  Automatic Hardware and Software Exit

- **ROMSIZE Feature**
  Selects Internal Program Memory Size from
      0 to 64kB
  Allows Access to Entire External Memory Map
  Dynamically Adjustable by Software

- **Peripheral Features**
  Two Full-Duplex Serial Ports
  Programmable Watchdog Timer
  13 Interrupt Sources (Six External)
  Five Levels of Interrupt Priority
  Power-Fail Reset
  Early Warning Power-Fail Interrupt
  Electromagnetic Interference (EMI) Reduction

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	33MHz		VARIABLE		UNITS
			MIN	MAX	MIN	MAX	
Clock Cycle Time	t_{XLXL}	SM2 = 0	360		$12t_{CLCL}$		ns
		SM2 = 1	120		$4t_{CLCL}$		ns
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0	200		$10t_{CLCL} - 100$		ns
		SM2 = 1	40		$3t_{CLCL} - 10$		ns
Output Data Hold to Clock Rising	t_{XHQX}	SM2 = 0	50		$2t_{CLCL} - 10$		ns
		SM2 = 1	20		$t_{CLCL} - 100$		
Input Data Hold After Clock Rising	t_{XHDX}	SM2 = 0	0		0		ns
		SM2 = 1	0		0		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0		200		$10t_{CLCL} - 100$	ns
		SM2 = 1		40		$3t_{CLCL} - 50$	ns

Note: SM2 is the serial port 0 mode bit 2. When serial port 0 is operating in mode 0 (SM0 = SM1 = 0), SM2 determines the number of crystal clocks in a serial port clock cycle.

CONTROL AND SEQUENCER

INTERNAL REGISTERS

INTERRUPT

SFRs
DPTR
DPTR1
SP

PC
AR INC
AR

CPU

DECODER
IR

ADDRESS BUS

INTERNAL CONTROL BUS

SERIAL I/O

TIMER/ COUNTERS

1kB x 8 RAM

16kB/32kB 64kB x 8 FLASH

I/O PORTS

WATCHDOG TIMER AND POWER MANAGER

CLOCK AND RESET

MEMORY CONTROL

ROM LOADER

Dallas Semiconductor
DS89C430/DS89C440/ DS89C450

XTAL1 XTAL2 RST

$\overline{PSEN}$ $\overline{EA}$ ALE/$\overline{PROG}$

P0 P1 P2 P3

DETAILED DESCRIPTION

The DS89C430, DS89C440, and DS89C450 are pin compatible with all three packages of the standard 8051 and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. The three part numbers vary only by the amount of internal flash memory (DS89C430 = 16kB, DS89C440 = 32kB, DS89C450 = 64kB), which can be in-system/in-application programmed from a serial port using ROM-resident or user-defined loader software. For volume deployments, the flash can also be loaded externally using standard commercially available parallel programmers.

Besides greater speed, the DS89C430/DS89C440/DS89C450 include 1kB of data RAM, a second full hardware serial port, seven additional interrupts, two extra levels of interrupt priority, programmable watchdog timer, brownout monitor, and power-fail reset. Dual data pointers (DPTRs) are included to speed up block data-memory moves with further enhancements coming from selectable automatic increment/decrement and toggle select operation. The speed of MOVX data memory access can be adjusted by adding stretch values up to 10 machine cycles for flexibility in selecting external memory and peripherals.

A power management mode consumes significantly lower power by slowing the CPU execution rate from one clock period per cycle to 1024 clock periods per cycle. A selectable switchback feature can automatically cancel this mode to enable normal speed responses to interrupts.

For EMI-sensitive applications, the microcontroller can disable the ALE signal when the processor is not accessing external memory.

Terminology

The term *DS89C430* is used in the remainder of the document to refer to the DS89C430, DS89C440, and DS89C450, unless otherwise specified.

Compatibility

The DS89C430 is a fully static CMOS 8051-compatible microcontroller similar in functional features to the DS87C520, but it offers much higher performance. In most cases, the DS89C430 can drop into an existing socket for the 8xC51 family, immediately improving the operation. While remaining familiar to 8051 family users, the DS89C430 has many new features. In general, software written for existing 8051-based systems works without modification on the DS89C430, with the exception of critical timing routines, as the DS89C430 performs its instructions much faster for any given crystal selection.

The DS89C430 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to 12 clocks-per-cycle operation to keep their timing compatible with a legacy 8051 family systems. However, timers are individually programmable to run at the new one clock per cycle if desired. The DS89C430 provides several new hardware features, described in subsequent sections, implemented by new special-function registers (SFRs).

Performance Overview

Featuring a completely redesigned high-speed 8051-compatible core, the DS89C430 allows operation at a higher clock frequency. This updated core does not have the wasted memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. The same machine cycle takes one clock in the DS89C430. Thus, the fastest instructions execute 12 times faster for the same crystal frequency (and actually 24 times faster for the INC data pointer instruction). It should be noted that this speed improvement is reduced when using external memory access modes that require more than one clock per cycle.

Individual program improvement depends on the instructions used. Speed-sensitive applications would make the most use of instructions that are 12 times faster. However, the sheer number of 12-to-1 improved op codes makes dramatic speed improvements likely for any code. These architectural improvements produce instruction cycle times as low as 30ns. The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The new page modes allow for increased efficiency in external memory accesses.

Instruction Set Summary

All instructions have the same functionality as their 8051 counterparts, including their affect on bits, flags, and other status functions. However, the timing of each instruction is different, in both absolute and relative number of clocks.

For absolute timing of real-time events, the duration of software loops can be calculated using information given in the *Instruction Set* table in the *Ultra-High-Speed Flash Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at a reduced number of clocks per increment to take advantage of faster processor operation.

The relative time of some instructions may be different in the new architecture. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS89C430, the MOVX instruction takes as little as two machine cycles or two oscillator cycles, but the "MOV direct, direct" uses three machine cycles or three oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS89C430 usually uses one machine cycle for each instruction byte and requires one cycle for execution. *The user concerned with precise program timing should examine the timing of each instruction to become familiar with the changes.*

Special-Function Registers (SFRs)

All peripherals and operations that are not explicit instructions in the DS89C430 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, and PSW), data pointers, stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function's status. The SFRs reside in register locations 80h–FFh and are only accessible by direct addressing. SFRs with addresses ending in 0h or 8h are bit addressable.

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All standard SFR locations from the 8051 are duplicated in the DS89C430, and several SFRs have been added for the unique features of the DS89C430. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map, allowing for increased functionality while maintaining complete instruction set compatibility. Table 1 shows the SFRs and their locations. Table 2 specifies the default reset condition for all SFR bits.

Data Pointers

The data pointers (DPTR and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location (on-chip or off-chip) or a memory-mapped peripheral. Two pointers are useful when moving data from one memory area to another, or when using a memory-mapped peripheral for both source and destination addresses. The user can select the active pointer through a dedicated SFR bit (SEL = DPS.0), or can activate an automatic toggling feature for altering the pointer selection (TSL = DPS.5). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

Stack Pointer

The stack pointer denotes the register location at the top of the stack, which is the last used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers.

I/O Ports

The DS89C430 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location and can be written or read. The I/O port has a latch that contains the value written by software.

Counter/Timers

Three 16-bit timer/counters are available in the DS89C430. Each timer is contained in two SFR locations that can be read or written by software. The timers are controlled by other SFRs, described in the *SFR Bit Description* section of the *Ultra-High-Speed Flash Microcontroller User's Guide*.

Serial Ports

The DS89C430 provides two UARTs that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the value contained in the UART. The same address is used for both read and write operations, and the read and write operations are distinguished by the instruction. Its own SFR control register controls each UART.

Table 1. SFR Register Map

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
SP	81h								
DPL	82h								
DPH	83h								
DPL1	84h								
DPH1	85h								
DPS	86h	ID1	ID0	TSL	AID	—	—	—	SEL
PCON	87h	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TL0	8Ah								
TL1	8Bh								
TH0	8Ch								

Table 1. SFR Register Map (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TH1	8Dh								
CKCON	8Eh	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0
P1	90h	P1.7/INT5	P1.6/INT4	P1.5/INT3	P1.4/INT2	P1.3/TXD1	P1.2/RXD1	P1.1/T2EX	P1.0/T2
EXIF	91h	IE5	IE4	IE3	IE2	CKRY	RGMD	RGSL	BGS
CKMOD	96h			T2MH	T1MH	T0MH	—	—	—
SCON0	98h	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0
SBUF0	99h								
ACON	9Dh	PAGEE	PAGES1	PAGES0	—	—	—	—	—
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
SADDR0	A9h								
SADDR1	AAh								
P3	B0h	P3.7/RD	P3.6/WR	P3.5/T1	P3.4/T0	P3.3/INT1	P3.2/INT0	P3.1/TXD0	P3.0/RXD0
IP1	B1h	—	MPS1	MPT2	MPS0	MPT1	MPX1	MPT0	MPX0
IP0	B8h	—	LPS1	LPT2	LPS0	LPT1	LPX1	LPT0	LPX0
SADEN0	B9h								
SADEN1	BAh								
SCON1	C0h	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
SBUF1	C1h								
ROMSIZE	C2h					PRAME	RMS2	RMS1	RMS0
PMR	C4h	CD1	CD0	SWB	CTM	4X/2X	ALEON	DME1	DME0
STATUS	C5h	PIS2	PIS1	PIS0	—	SPTA1	SPRA1	SPTA0	SPRA0
TA	C7h								
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
T2MOD	C9h							T2OE	DCEN
RCAP2L	CAh								
RCAP2H	CBh								
TL2	CCh								
TH2	CDh								
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P
FCNTL	D5h	FBUSY	FERR			FC3	FC2	FC1	FC0
FDATA	D6h								
WDCON	D8h	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
ACC	E0h								
EIE	E8h	—	—	—	EWDI	EX5	EX4	EX3	EX2
B	F0h								
EIP1	F1h	—	—	—	MPWDI	MPX5	MPX4	MPX3	MPX2
EIP0	F8h	—	—	—	LPWDI	LPX5	LPX4	LPX3	LPX2

Note: Shaded bits are timed-access protected.

Table 2. SFR Reset Value

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	80h	1	1	1	1	1	1	1	1
SP	81h	0	0	0	0	0	1	1	1
DPL	82h	0	0	0	0	0	0	0	0
DPH	83h	0	0	0	0	0	0	0	0
DPL1	84h	0	0	0	0	0	0	0	0
DPH1	85h	0	0	0	0	0	0	0	0
DPS	86h	0	0	0	0	0	1	0	0
PCON	87h	0	0	Special	Special	0	0	0	0
TCON	88h	0	0	0	0	0	0	0	0
TMOD	89h	0	0	0	0	0	0	0	0
TL0	8Ah	0	0	0	0	0	0	0	0
TL1	8Bh	0	0	0	0	0	0	0	0
TH0	8Ch	0	0	0	0	0	0	0	0
TH1	8Dh	0	0	0	0	0	0	0	0
CKCON	8Eh	0	0	0	0	0	0	0	1
P1	90h	1	1	1	1	1	1	1	1
EXIF	91h	0	0	0	0	Special	Special	Special	0
CKMOD	96h	1	1	0	0	0	1	1	1
SCON0	98h	0	0	0	0	0	0	0	0
SBUF0	99h	0	0	0	0	0	0	0	0
ACON	9Dh	0	0	0	1	1	1	1	1
P2	A0h	1	1	1	1	1	1	1	1
IE	A8h	0	0	0	0	0	0	0	0
SADDR0	A9h	0	0	0	0	0	0	0	0
SADDR1	AAh	0	0	0	0	0	0	0	0
P3	B0h	1	1	1	1	1	1	1	1
IP1	B1h	1	0	0	0	0	0	0	0
IP0	B8h	1	0	0	0	0	0	0	0
SADEN0	B9h	0	0	0	0	0	0	0	0
SADEN1	BAh	0	0	0	0	0	0	0	0
SCON1	C0h	0	0	0	0	0	0	0	0
SBUF1	C1h	0	0	0	0	0	0	0	0
ROMSIZE	C2h	1	1	1	1	0	1	0	1
PMR	C4h	1	0	0	0	0	0	0	0
STATUS	C5h	0	0	0	1	0	0	0	0
TA	C7h	1	1	1	1	1	1	1	1
T2CON	C8h	0	0	0	0	0	0	0	0
T2MOD	C9h	1	1	1	1	1	1	0	0
RCAP2L	CAh	0	0	0	0	0	0	0	0
RCAP2H	CBh	0	0	0	0	0	0	0	0

Table 2. SFR Reset Value (continued)

REGISTER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TL2	CCh	0	0	0	0	0	0	0	0
TH2	CDh	0	0	0	0	0	0	0	0
PSW	D0h	0	0	0	0	0	0	0	0
FCNTL	D5h	1	0	1	1	0	0	0	0
FDATA	D6h	0	0	0	0	0	0	0	0
WDCON	D8h	0	Special	0	Special	0	Special	Special	0
ACC	E0h	0	0	0	0	0	0	0	0
EIE	E8h	1	1	1	0	0	0	0	0
B	F0h	0	0	0	0	0	0	0	0
EIP1	F1h	1	1	1	0	0	0	0	0
EIP0	F8h	1	1	1	0	0	0	0	0

Note: Consult the *Ultra-High-Speed Flash Microcontroller User's Guide* for more information about the bits marked "Special."

Memory Organization

There are three distinct memory areas in the DS89C430: scratchpad registers, program memory, and data memory. The registers are located on-chip but the program and data memory spaces can be on-chip, off-chip, or both. The DS89C430/DS89C440/DS89C450 have 16kB/32kB/64kB of on-chip program memory, respectively, implemented in flash memory and also have 1kB of on-chip data memory space that can be configured as program space using the PRAME bit in the ROMSIZE feature. The DS89C430 uses a memory-addressing scheme that separates program memory from data memory. The program and data segments can be overlapped since they are accessed in different manners. If the maximum address of on-chip program or data memory is exceeded, the DS89C430 performs an external memory access using the expanded memory bus. The $\overline{PSEN}$ signal goes active low to serve as a chip enable or output enable when performing a code fetch from external program memory. MOVX instructions activate the $\overline{RD}$ or $\overline{WR}$ signal for external MOVX data memory access. The program memory ROMSIZE feature allows software to dynamically configure the maximum address of on-chip program memory. This allows the DS89C430 to act as a bootloader for an external memory. It also enables the use of the overlapping external program spaces. The lower 128 bytes of on-chip flash memory—if ROMSIZE is greater than 0—are used to store reset and interrupt vectors. 256 bytes of on-chip RAM serve as a register area and program stack, which are separated from the data memory.

Memory Configuration

As illustrated in Figure 6, the DS89C430 incorporates two 8kB flash areas for on-chip program memory and 1kB of SRAM for on-chip data memory or a particular range (400–7FF) of "alternate" program memory space. The DS89C440 incorporates two 16kB flash memories and the DS89C450 incorporates two 32kB flash memories. The DS89C430 uses an address scheme that separates program memory from data memory such that the 16-bit address bus can address each memory area up to maximum of 64kB.

Figure 6. Memory Map

INTERNAL MEMORY

INTERNAL REGISTERS

128 Bytes SFR

FF

128 Bytes Indirect Addressing

80
7F

2F
20
1F

Bit Addressable

Bank 3

Bank 2

Bank 1

Bank 0

00

03FF

1K x 8 SRAM

Data OR prog mem addr from 400 - 7FF

0000

3FFF

8K x 8 Flash Memory (Program)

2000

1FFF

8K x 8 Flash Memory (Program)

0000

FFFF

External Program Memory

4000

0000

FFFF

External Data Memory

03FF

0000

68
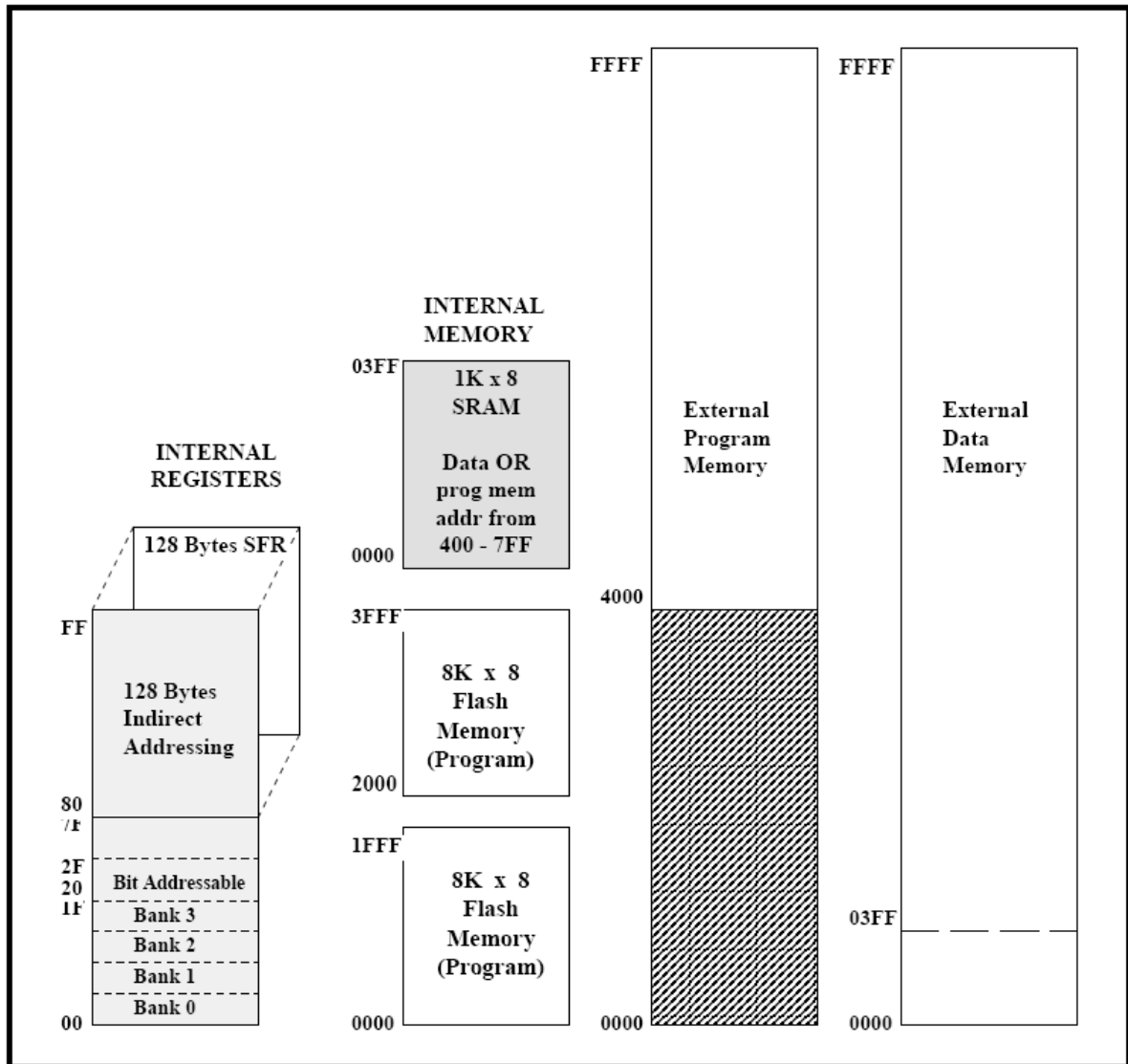
Data Pointer Increment/Decrement and Options

The DS89C430 incorporates a hardware feature to assist applications that require data pointer increment/ decrement. Data pointer increment/decrement bits ID0 and ID1 (DPS.6 and DPS.7) define how the INC DPTR instruction functions in relation to the active DPTR (selected by the SEL bit). Setting ID0 = 1 and SEL = 0 enables the decrement operation for DPTR, and execution of the INC DPTR instruction decrements the DPTR contents by 1. Similarly, setting ID1 = 1 and SEL = 1 enables the decrement operation for DPTR1, and execution of the INC DPTR instruction decrements the DPTR1 contents by 1. With this feature, the user can configure the data pointers to operate in four ways for the INC DPTR instruction:

ID1	ID0	SEL = 0	SEL = 1
0	0	INC DPTR	INC DPTR1
0	1	DEC DPTR	INC DPTR1
1	0	INC DPTR	DEC DPTR1
1	1	DEC DPTR	DEC DPTR1

SEL (DPS.0) bit always selects the active data pointer. The DS89C430 offers a programmable option that allows any instructions related to data pointer to toggle the SEL bit automatically. This option is enabled by setting the toggle-select-enable bit (TSL–DPS.5) to a logic 1. Once enabled, the SEL bit is automatically toggled *after* the execution of one of the following five DPTR-related instructions:

```
INC DPTR
MOV DPTR #data16
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```

The DS89C430 also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 *after* the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent on the setting of the ID1 and ID0 bits. This option is enabled by setting the automatic increment/decrement enable (AID–DPS.4) to a logic 1 and is affected by the following three instructions:

```
MOVC A, @A+DPTR
MOVX A, @DPTR
MOVX @DPTR, A
```
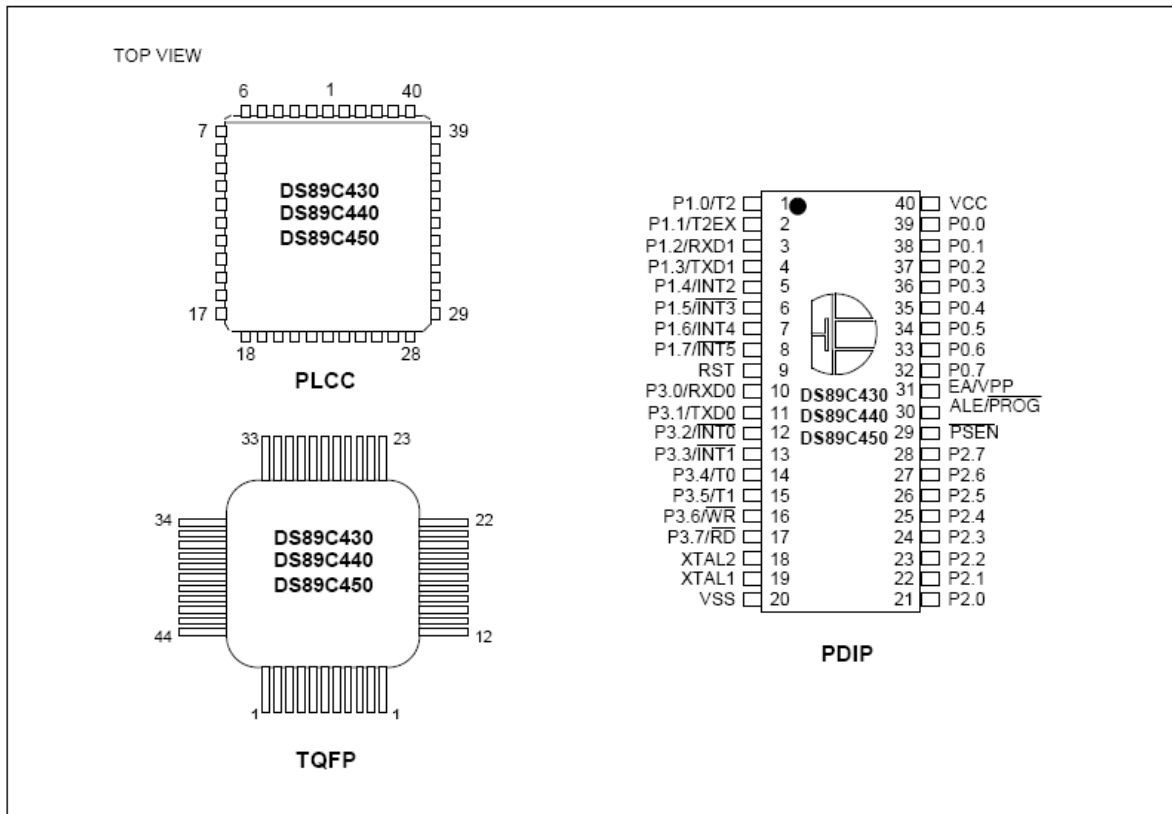
Interrupt Summary

INTERRUPT	VECTOR	NATURAL ORDER	FLAG	ENABLE	PRIORITY CONTROL
Power Fail	33h	0 (Highest)	PFI (WDCON.4)	EPFI(WDCON.5)	N/A
External Interrupt 0	03h	1	IE0 (TCON.1) (Note 1)	EX0 (IE.0)	LPX0 (IP0.0); MPX0 (IP1.0)
Timer 0 Overflow	0Bh	2	TF0 (TCON.5) (Note 2)	ET0 (IE.1)	LPT0 (IP0.1); MPT0 (IP1.1)
External Interrupt 1	13h	3	IE1 (TCON.3) (Note 1)	EX1 (IE.2)	LPX1 (IP0.2); MPX1 (IP1.2)
Timer 1 Overflow	1Bh	4	TF1 (TCON.7) (Note 2)	ET1 (IE.3)	LPT1 (IP0.3); MPT1 (IP1.3)
Serial Port 0	23h	5	RI_0 (SCON0.0); TI_0 (SCON0.1)	ES0 (IE.4)	LPS0 (IP0.4); MPS0 (IP1.4)
Timer 2 Overflow	2Bh	6	TF2 (T2CON.7); EXF2 (T2CON.6)	ET2 (IE.5)	LPT2 (IP0.5); MPT2 (IP1.5)
Serial Port 1	3Bh	7	RI_1 (SCON1.0); TI_1 (SCON1.1)	ES1 (IE.6)	LPS1 (IP0.6); MPS1 (IP1.6)
External Interrupt 2	43h	8	IE2 (EXIF.4)	EX2 (EIE.0)	LPX2 (EIP0.0); MPX2 (EIP1.0)
External Interrupt 3	4Bh	9	IE3 (EXIF.5)	EX3 (EIE.1)	LPX3 (EIP0.1); MPX3 (EIP1.1)
External Interrupt 4	53h	10	IE4 (EXIF.6)	EX4 (EIE.2)	LPX4 (EIP0.2); MPX4 (EIP1.2)
External Interrupt 5	5Bh	11	IE5 (EXIF.7)	EX5 (EIE.3)	LPX5 (EIP0.3); MPX5 (EIP1.3)
Watchdog	63h	12 (Lowest)	WDIF (WDCON.3)	EWDI (EIE.4)	LPWDI (EIP0.4); MPWDI (EIP1.4)

Note 1: If the interrupt is edge triggered, the flag is cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.

Note 2: The flag is cleared automatically by hardware when the service routine is vectored to.

PIN CONFIGURATIONS

TOP VIEW

DS89C430
DS89C440
DS89C450

PLCC

DS89C430
DS89C440
DS89C450

TQFP

P1.0/T2	1	40	VCC
P1.1/T2EX	2	39	P0.0
P1.2/RXD1	3	38	P0.1
P1.3/TXD1	4	37	P0.2
P1.4/INT2	5	36	P0.3
P1.5/INT3	6	35	P0.4
P1.6/INT4	7	34	P0.5
P1.7/INT5	8	33	P0.6
RST	9	32	P0.7
P3.0/RXD0	10	31	EA/VPP
P3.1/TXD0	11	30	ALE/PROG
P3.2/INT0	12	29	PSEN
P3.3/INT1	13	28	P2.7
P3.4/T0	14	27	P2.6
P3.5/T1	15	26	P2.5
P3.6/WR	16	25	P2.4
P3.7/RD	17	24	P2.3
XTAL2	18	23	P2.2
XTAL1	19	22	P2.1
VSS	20	21	P2.0

DS89C430
DS89C440
DS89C450

PDIP

PIN DESCRIPTION

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
40	12, 44	6, 38	V$_{CC}$	+5V
20	1, 22, 23, 34	16, 17, 28, 39	GND	Logic Ground
9	10	4	RST	External Reset. The RST input pin is bidirectional and contains a Schmitt Trigger to recognize external active-high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wire-ORed external reset sources. An RC is not required for power-up, as the device provides this function internally.
19	21	15	XTAL1	Crystal Oscillators. These pins provide support for fundamental-mode parallel-resonant AT-cut crystals. XTAL1 also acts as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
18	20	14	XTAL2	
29	32	26	$\overline{PSEN}$	Program Store Enable. This signal is commonly connected to optional external program memory as a chip enable. $\overline{PSEN}$ provides an active-low pulse and is driven high when external program memory is not being accessed. In one-cycle page mode 1, $\overline{PSEN}$ remains low for consecutive page hits.
30	33	27	ALE/$\overline{PROG}$	Address Latch Enable. This signal functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373-family transparent latch. In default mode, ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. In page mode, the ALE pulse width is altered according to the page mode selection. In traditional 8051 mode, ALE is high when using the EMI reduction mode and during a reset condition. ALE can be enabled by writing ALEON = 1 (PMR.2). Note that ALE operates independently of ALEON during external memory accesses. As an alternate mode, this pin ($\overline{PROG}$) is used to execute the parallel program function.
39	43	37	P0.0 (AD0)	Port 0 (AD0–AD7), I/O. Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function, Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to logic 0, the port transitions to a bidirectional data bus. This bus is used to read external program memory and read/write external RAM or peripherals. When used as a memory bus, the port provides weak pullups for logic 1 outputs. The reset condition of port 0 is tri-state. Pullup resistors are required only when using port 0 as an I/O port.
38	42	36	P0.1 (AD1)	
37	41	35	P0.2 (AD2)	
36	40	34	P0.3 (AD3)	
35	39	33	P0.4 (AD4)	
34	38	32	P0.5 (AD5)	
33	37	31	P0.6 (AD6)	
32	36	30	P0.7 (AD7)	

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
1	2	40	P1.0	Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for timer 2 I/O, new external interrupts, and new serial port 1. The reset condition of port 1 is with all bits at logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C440/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate functions of port 1 are as follows:
2	3	41	P1.1	
3	4	42	P1.2	
4	5	43	P1.3	
5	6	44	P1.4	
6	7	1	P1.5	
7	8	2	P1.6	
8	9	3	P1.7	

PORT	ALTERNATE	FUNCTION
P1.0	T2	External I/O for Timer/Counter2
P1.1	T2EX	Timer 2 Capture/Reload Trigger
P1.2	RXD1	Serial Port 1 Receive
P1.3	TXD1	Serial Port 1 Transmit
P1.4	INT2	External Interrupt 2 (Positive Edge Detect)
P1.5	$\overline{INT3}$	External Interrupt 3 (Negative Edge Detect)
P1.6	INT4	External Interrupt 4 (Positive Edge Detect)
P1.7	$\overline{INT5}$	External Interrupt 5 (Negative Edge Detect)

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
21	24	18	P2.0 (A8)	Port 2 (A8–A15), I/O. Port 2 is an 8-bit, bidirectional I/O port. The reset condition of port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C440/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function, port 2 can function as the MSB of the external address bus when reading external program memory and read/write external RAM or peripherals. In page mode 1, port 2 provides both the MSB and LSB of the external address bus. In page mode 2, it provides the MSB and data.
22	25	19	P2.1 (A9)	
23	26	20	P2.2(A10)	
24	27	21	P2.3(A11)	
25	28	22	P2.4(A12)	
26	29	23	P2.5(A13)	
27	30	24	P2.6(A14)	
28	31	25	P2.7(A15)	
10	11	5	P3.0	Port 3, I/O. Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for external interrupts, serial port 0, timer 0 and 1 inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port overcomes the weak pullup. When software writes a 0 to any port pin, the DS89C430/DS89C440/DS89C450 activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 causes a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of port 3 are as follows:
11	13	7	P3.1	
12	14	8	P3.2	
13	15	9	P3.3	
14	16	10	P3.4	
15	17	11	P3.5	
16	18	12	P3.6	
17	19	13	P3.7	

PORT	ALTERNATE	FUNCTION
P3.0	RXD0	Serial Port 0 Receive
P3.1	TXD0	Serial Port 0 Transmit
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 External Input
P3.5	T1	Timer 1 External Input
P3.6	$\overline{WR}$	External Data Memory Write Strobe
P3.7	$\overline{RD}$	External Data Memory Read Strobe

PIN			NAME	FUNCTION
PDIP	PLCC	TQFP		
31	35	29	$\overline{EA}$	External Access. Allows selection of internal or external program memory. Connect to ground to force the DS89C430/DS89C440/DS89C450 to use an external memory program memory. The internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal flash memory.

DS1307/DS1308 64 X 8 Serial Real Time Clock

FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 56 byte nonvolatile RAM for data storage
- 2-wire serial interface
- Programmable squarewave output signal
- Automatic power-fail detect and switch circuitry
- Consumes less than 500 nA in battery backup mode with oscillator running
- Optional industrial temperature range -40°C to +85°C (IND) available for DS1307 and DS1308
- DS1307 available in 8-pin DIP or SOIC
- DS1308 available in 36-pin SMD BGA (Ball Grid Array)
- DS1308 accuracy is better than ±2 minute/month at 25°C

PIN ASSIGNMENT

```
       ┌───∪───┐
 X1  ┌─┤ 1   8 ├─┐ Vcc
 X2  ┌─┤ 2   7 ├─┐ SQW/OUT
VBAT ┌─┤ 3   6 ├─┐ SCL
 GND ┌─┤ 4   5 ├─┐ SDA
       └───────┘
```
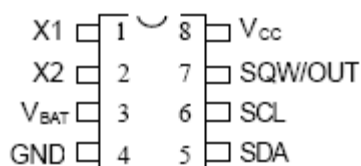
DS1307 8-Pin DIP (300-mil)

PIN DESCRIPTION DS1307/DS1308

V_{CC}	- Primary Power Supply
X1, X2	- 32.768 kHz Crystal Connection
V_{BAT}	- +3 Volt Battery Input
GND	- Ground
SDA	- Serial Data
SCL	- Serial Clock
SQW/OUT	- Square wave/Output Driver

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FAIRCHILD
SEMICONDUCTOR™

MM74C922 16-Key Encoder

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

Pin Assignment for SOIC

ROW Y1	1	20 — V_{CC}
ROW Y2	2	19 — DATA OUT A
ROW Y3	3	18 — DATA OUT B
ROW Y4	4	17 — DATA OUT C
NC	5	16 — DATA OUT D
OSCILLATOR	6	15 — NC
KEYBOUNCE MASK	7	14 — OUTPUT ENABLE
COLUMN X4	8	13 — DATA AVAILABLE
COLUMN X3	9	12 — COLUMN X1
GND	10	11 — COLUMN X2

Top View
MM74C922
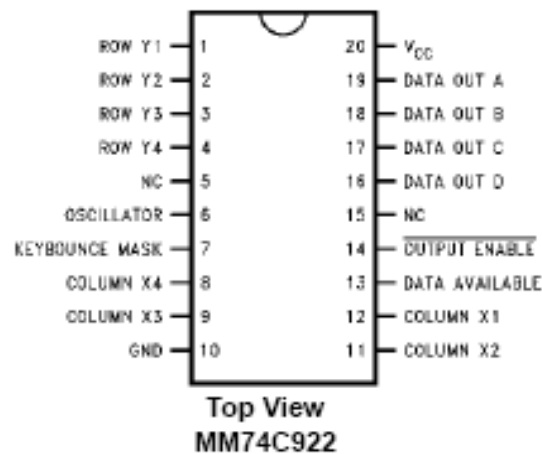
Truth Tables

(Pins 0 through 11)

Switch Position		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4
D													
A	A	0	1	0	1	0	1	0	1	0	1	0	1
T	B	0	0	1	1	0	0	1	1	0	0	1	1
A	C	0	0	0	0	1	1	1	1	0	0	0	0
O	D	0	0	0	0	0	0	0	0	1	1	1	1
U	E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0
T													

(Pins 12 through 19)

Switch Position		12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5(Note 1), X1	17 Y5 (Note 1), X2	18 Y5 (Note 1), X3	19 Y5 (Note 1), X4
D									
A	A	0	1	0	1	0	1	0	1
T	B	0	0	1	1	0	0	1	1
A	C	1	1	1	1	0	0	0	0
O	D	1	1	1	1	0	0	0	0
U	E (Note 1)	0	0	0	0	1	1	1	1
T									

Block Diagram

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MAX232

/MAXIM
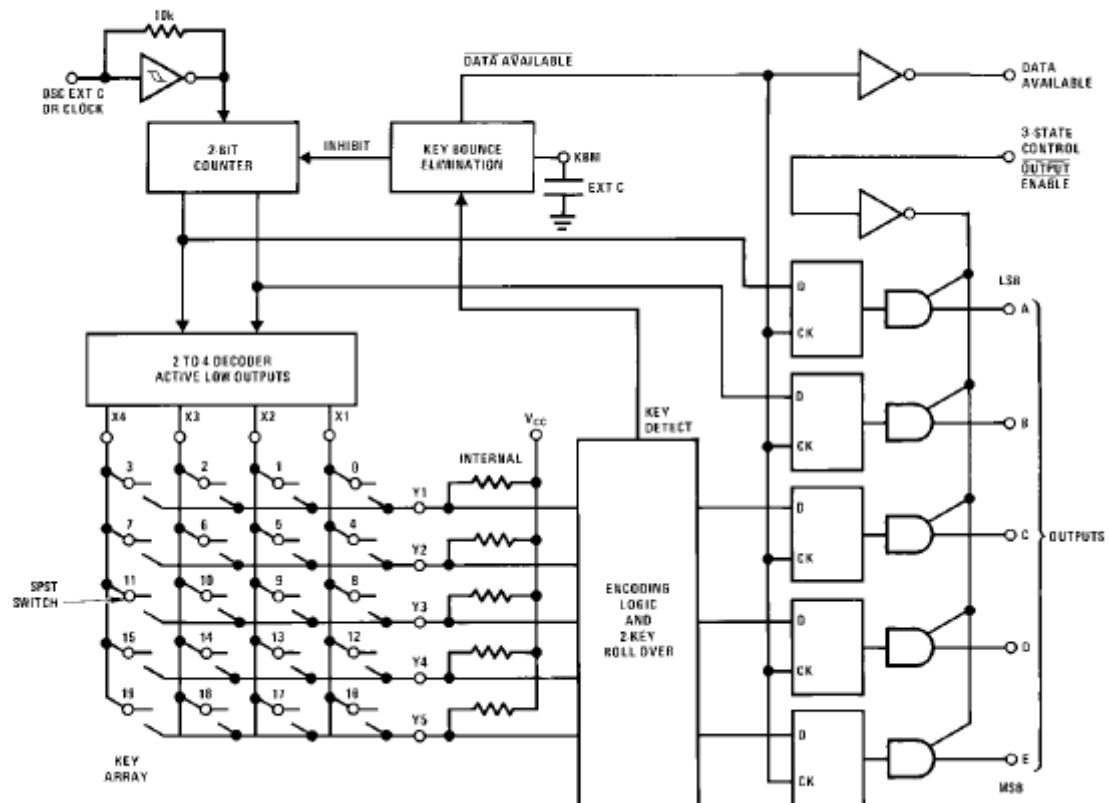
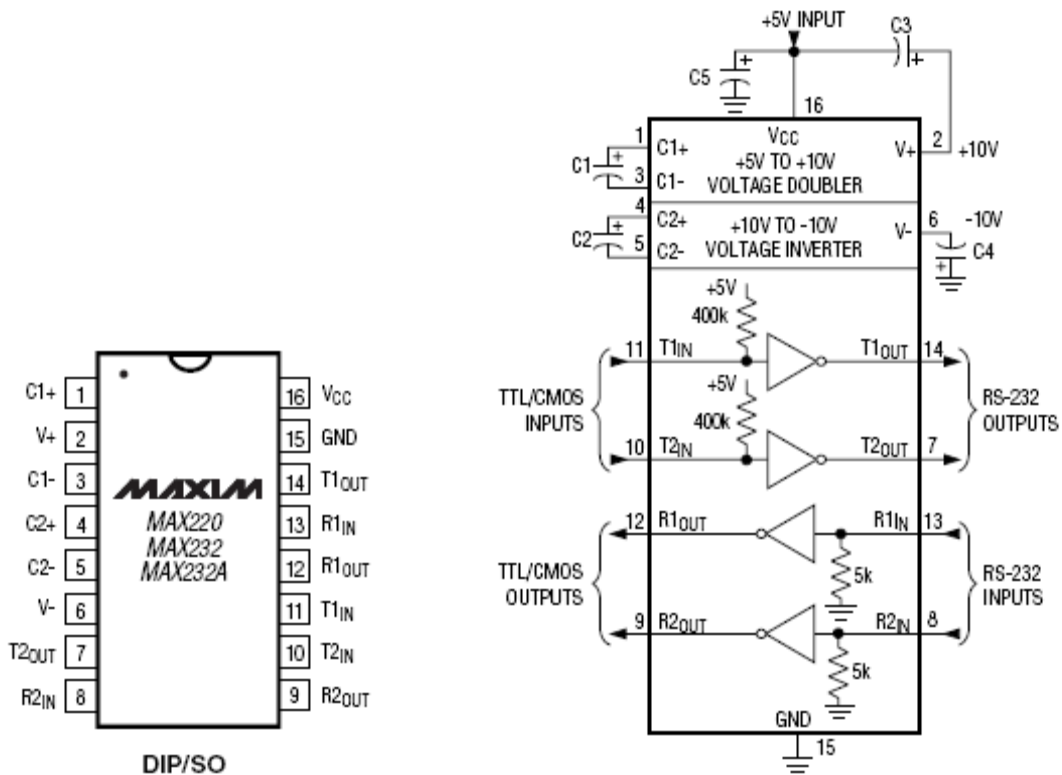## Features

Superior to Bipolar

♦ Operate from Single +5V Power Supply
(+5V and +12V—MAX231/MAX239)

♦ Low-Power Receive Mode in Shutdown
(MAX223/MAX242)

♦ Meet All EIA/TIA-232E and V.28 Specifications

♦ Multiple Drivers and Receivers

♦ 3-State Driver and Receiver Outputs

♦ Open-Line Detection (MAX243)

MAX220/MAX232/MAX232A Pin Configuration and Typical Operating Circuit

Description

The MAX220–MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, particularly applications where ±12V is not available.

These parts are especially useful in battery-powered systems, since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX225, MAX233, MAX235, and MAX245/MAX246/MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	0.1	No	—	120	Ultra-low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1	Yes	—	200	Low-power shutdown
MAX223 (MAX213)	+5	4/5	4	1.0 (0.1)	Yes	✔	120	MAX241 and receivers active in shutdown
MAX225	+5	5/5	0	—	Yes	✔	120	Available in SO
MAX230 (MAX200)	+5	5/0	4	1.0 (0.1)	Yes	—	120	5 drivers with shutdown
MAX231 (MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232 (MAX202)	+5	2/2	4	1.0 (0.1)	No	—	120 (64)	Industry standard
MAX232A	+5	2/2	4	0.1	No	—	200	Higher slew rate, small caps
MAX233 (MAX203)	+5	2/2	0	—	No	—	120	No external caps
MAX233A	+5	2/2	0	—	No	—	200	No external caps, high slew rate
MAX234 (MAX204)	+5	4/0	4	1.0 (0.1)	No	—	120	Replaces 1488
MAX235 (MAX205)	+5	5/5	0	—	Yes	—	120	No external caps
MAX236 (MAX206)	+5	4/3	4	1.0 (0.1)	Yes	—	120	Shutdown, three state
MAX237 (MAX207)	+5	5/3	4	1.0 (0.1)	No	—	120	Complements IBM PC serial port
MAX238 (MAX208)	+5	4/4	4	1.0 (0.1)	No	—	120	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; single-package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes	—	120	DIP or flatpack package
MAX241 (MAX211)	+5	4/5	4	1.0 (0.1)	Yes	—	120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	✔	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	No	—	200	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	No	—	120	High slew rate
MAX245	+5	8/10	0	—	Yes	✔	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	0	—	Yes	✔	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	0	—	Yes	✔	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	4	1.0	Yes	✔	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	Yes	✔	120	Available in quad flatpack package

Input/Output Messages for

FALCOM GPS receiver with SiRFstarIIe-chip-set

1.   NMEA Input/Output Messages

The SiRFstarIIe/LP Evaluation Receiver is capable of outputting data in the NMEA-0183 format as defined by the National Marine Electronics Association (NMEA), Standard for Interfacing Marine Electronic Devices, Version 2.20, January 1, 1997.

1.1   NMEA Output Messages

Table 1 lists each of the NMEA output messages supported by the SiRFstarIIe/LP Evaluation Receiver and a brief description.

table 1   NMEA Output Messages

Option	Description
GGA	Time, position and fix type data.
GLL	Latitude, longitude, UTC time of position fix and status.
GSA	GPS receiver operating mode, satellites used in the position solution, and DOP values.
GSV	The number of GPS satellites in view satellite ID numbers, elevation, azimuth, and SNR values.
MSS	Signal-to-noise ratio, signal strength, frequency, and bit rate from a radio-beacon receiver.
RMC	Time, date, position, course and speed data.
VTG	Course and speed information relative to the ground.

1.1.1 GGA —Global Positioning System Fixed Data

Table 2 contains the values for the following example:

$GPGGA,161229.487,3723.2475,N,12158.3416,W,1,07,1.0,9.0,M, , , ,0000*18

table 2   GGA Data Format

Name	Example	Units	Description
Message ID	$GPGGA		GGA protocol header
UTC Time	161229.487		hhmmss.sss
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	N		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
Position Fix Indicator	1		See table 3
Satellites Used	07		Range 0 to 12
HDOP	1.0		Horizontal Dilution of Precision
MSL Altitude[3]	9.0	meters	
Units	M	meters	
Geoid Separation[1]		meters	
Units	M	meters	
Age of Diff. Corr.		second	Null fields when DGPS is not used
Diff. Ref. Station ID	0000		
Checksum	*18		
<CR> <LF>			End of message termination

table 3   Position Fix Indicator

Value	Description
0	Fix not available or invalid
1	GPS SPS Mode, fix valid
2	Differential GPS, SPS Mode, fix valid
3	GPS PPS Mode, fix valid

1.1.2　GLL—Geographic Position - Latitude/Longitude

Table 4 contains the values for the following example:

$GPGLL,3723.2475,N,12158.3416,W,161229.487,A*2C

table 4　　　　GLL Data Format

Name	Example	Units	Description
Message ID	$GPGLL		GLL protocol header
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	N		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
UTC Position	161229.487		hhmmss.sss
Status	A		A=data valid or V=data not valid
Checksum	*2C		
<CR> <LF>			End of message termination

GSA—GNSS DOP and Active Satellites

Table 5 contains the values for the following example:

$GPGSA,A,3,07,02,26,27,09,04,15, , , , , ,1.8,1.0,1.5*33

table 5　　　　　　GSA Data Format

Name	Example	Units	Description
Message ID	$GPGSA		GSA protocol header
Mode 1	A		See table 6
Mode 2	3		See table 7
Satellite Used[3]	07		Sv on Channel 1
Satellite Used[3]	02		Sv on Channel 2
....			....
Satellite Used[3]			Sv on Channel 12
PDOP	1.8		Position Dilution of Precision
HDOP	1.0		Horizontal Dilution of Precision
VDOP	1.5		Vertical Dilution of Precision
Checksum	*33		
<CR> <LF>			End of message termination

table 6　　　　　　Mode 1

Value	Description
M	Manual - forced to operate in 2D or 3D mode
A	2DAutomatic - allowed to automatically switch 2D/3D

table 7　　　　　　Mode 2

Value	Description
1	Fix Not Available
2	2D
3	3D

1.1.3   GSV—GNSS Satellites in View

Table 8 contains the values for the following example:

$GPGSV,2,1,07,07,79,048,42,02,51,062,43,26,36,256,42,27,27,138,42*71

$GPGSV,2,2,07,09,23,313,42,04,19,159,41,15,12,041,42*41

table 8   GSV Data Format

Name	Example	Units	Description
Message ID	$GPGSV		GSV protocol header
Number of Messages[4]	2		Range 1 to 3
Message Number[4]	1		Range 1 to 3
Satellites in View	07		
Satellite ID	07		Channel 1 (Range 1 to 32)
Elevation	79	degrees	Channel 1 (Maximum 90)
Azimuth	048	degrees	Channel 1 (True, Range 0 to 359)
SNR (C/No)	42	dBHz	Range 0 to 99, null when not tracking
....			....
Satellite ID	27		Channel 4 (Range 1 to 32)
Elevation	27	degrees	Channel 4 (Maximum 90)
Azimuth	138	degrees	Channel 4 (True, Range 0 to 359)
SNR (C/No)	42	dBHz	Range 0 to 99, null when not tracking
Checksum	*71		
<CR> <LF>			End of message termination

1.1.4   MSS—MSK Receiver Signal

Table 9 contains the values for the following example:

$GPMSS,55,27,318.0,100,*66

table 9 MSS Data Format

Name	Example	Units	Description
Message ID	$GPMSS		MSS protocol header
Signal Strength	55	dB	SS of tracked frequency
Signal-to-Noise Ratio	27	dB	SNR of tracked frequency
Beacon Frequency	318.0	kHz	Currently tracked frequency
Beacon Bit Rate	100		bits per second

1.1.5 RMC—Recommended Minimum Specific GNSS Data

Table 10 contains the values for the following example:

$GPRMC,161229.487,A,3723.2475,N,12158.3416,W,0.13,309.62,120598, ,*10

table 10 RMC Data Format

Name	Example	Units	Description
Message ID	$GPRMC		RMC protocol header
UTC Time	161229.487		hhmmss.sss
Status[5]	A		A=data valid or V=data not valid
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	N		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
Speed Over Ground	0.13	knots	
Course Over Ground	309.62	degrees	True
Date	120598		ddmmyy
Magnetic Variation[6]		degrees	E=east or W=west
Checksum	*10		
<CR> <LF>			End of message termination

1.1.6 VTG—Course Over Ground and Ground Speed

Table 11 contains the values for the following example:

$GPVTG,309.62,T, ,M,0.13,N,0.2,K*6E

table 11 VTG Data Format

Name	Example	Units	Description
Message ID	$GPVTG		VTG protocol header
Course	309.62	degrees	Measured heading
Reference	T		True
Course		degrees	Measured heading
Reference	M		Magnetic[7]
Speed	0.13	knots	Measured horizontal speed
Units	N		Knots
Speed	0.2	km/hr	Measured horizontal speed
Units	K		Kilometers per hour
Checksum	*6E		
<CR> <LF>			End of message termination

APPENDIX F: I/O MASSEGE FOR GPS RECEIVER

GPS-Receiver JP7

1.1   General information

The Global Positioning System uses satellite navigation, an entirely new concept in navigation. GPS has become established in many areas, for example, in civil aviation or deep-sea shipping. It is making deep inroads in vehicle manufacturing and before long everyone of us will use it this way or another.

The GPS system is operated by the government of the United States of America, which also has sole responsibility for the accuracy and maintenance of the system. The system is constantly being improved and may entail modifications effecting the accuracy and performance of the GPS equipment.

1.2   Operation/antenna

Operate the GPS receiver with an antenna connected to it and with no obstruction between the receiver and the satellite.

Make absolutely sure that the antenna socket or antenna cable is not shorted as this would render the GPS receiver dysfunctional.

Do not use the receiver with a damaged antenna. Replace a damaged antenna without delay. Use only a manufacturer-approved antenna. Use only the supplied or an approved antenna with your GPS receiver. Antennas from other manufacturers which are not authorized by the supplier can damage the GPS receiver.

Technical modifications and additions may contravene local radio-frequency emission regulations or invalidate the type approval.

FEATURES

- OEM single board 12 channel GPS receiver

- dimensions: 25,4 x 25,4 x 3 mm

- weight: 2,5 g (without shielding)

- operating voltage: 3.3 V DC ±5 %

- power consumption: 220 mW (continuous mode with Low Power chipset)

- temperature range: -40 to +85 °C (operation, transportation and storage)

- protocol: SDI1/SDO1:
  NMEA 9600 baud, Msg.: GLL, GGA, RMC, VTG, GSV, GSA
  8 data bits, no parity, 1 stop bit
  SDI2/SDO2:
  RTCM, 9600 baud

- trickle power mode: The default Mode of FALCOM JP7 is continuous Mode, but the user can set FALCOM JP7 into the Trickle Power Mode via input command message. The FALCOM JP7 enters the trickle power mode corresponding to figure 2 (**800 ms OFF Time and 200 ms ON Time**) as soon as valid GPS data are available. As a result the average power consumption is reduced by approximately 80 % (approximately 150 mW). The settings for the trickle power mode can be modified by using the SiRFstar demo software. For example if the FALCOM JP7 is configured to enter the OnTime mode each 10 s for a duration of 200 ms the average power consumption can be reduced up to approx. 95 % (approx. 15 mW, ca. 4,8 mA at Vcc=3.3 V).
  For more details see chapter 4 "Operating modes".

Normal Operation

In this default implementation of normal mode the JP7 is fully powered and performs the function of signal search, acquisition, measurement and satellite tracking. The amount of time spent in the initial full power is dependent on the start condition that applies the number of satellites for which the ephemeris must be collected and the time to calibrate the RTC as well as the location of the GPS antenna (which it must have an unobstructed view to the sky in order to receive the satellite radio transmissions). When the JP7 has been locked-on to at least four satellites, the receiver is able to calculate its current positions. In this mode the JP7 is fully powered and satellite searching, initial acquisition, initial position calculation and tracking measurements functions are always performed. In order to reduce the start up time of the receiver it is preferable to be connected to an external back up battery, so that the RTC is running during the power interrupt. The backup power is required for retention of SRAM memory and maintaining the Real-Time-Clock. The validity of data stored in SRAM is kept due to RTC keeps running and these data will be needed on the next power up scenario.

Trickle Power Operation

In the Trickle Power mode, power is still applied to the JP7, but the GPS engine is shut off and RF circuits are powered down. The Trickle Power mode provides a method of operating the JP7 in a user programmable duty cycle, consisting of a receiver measurement on time tracking and an interval of position update, thereby reducing the average power consumption over a period of time. The transition into the Trickle Power mode of JP7 can be implemented and configured by using the **Set Operating Mode** command in SiRFdemo. Between two on time tracking periods the JP7 sets itself in the sleep phase in other word into the low power consumption. The transition from sleep mode of JP7 back to the on time tracking is generated through the internal RTC which transmits a wakeup signal to the GPS engine to switch it on as well the RF circuit is powered on. The JP7 is waked up and begins to acquire the on view satellites. In order to reduce the start up time of the receiver for the next power up is preferable to connect an external back up battery, so that the RTC is running during the power interrupt and the required data and the Trickle Mode configuration are kept from previous operation. If the receiver fails to acquire satellites within a given period of time (approx. 150 sec), the receiver sets itself into the sleep phase. The duration of this sleep

phase is approx. 30 sec. After that, the receiver wakes up, reset itself and tries to acquire satellites which are in view. This procedure repeats itself until the initial position computation of GPS receiver is completed.

Hint: After initial turn on or system reset, the JP7 will remain in the full power tracking until a series of Kalman filter navigation solution is obtained, all ephemeris data is collected and the RTC is calibrated prior to transitioning to the low power duty cycle mode.

Push-to-Fix Mode

The Push-to-Fix mode puts the FALCOM JP7 into a background duty cycle which provides a periodic refresh of position, receiver time, ephemeris data and RTC calibration every 30 minutes. The Push-to-Fix mode is similar but executive from Trickle Power mode, meaning that only one mode can be set at a time. In this mode the receiver sets itself into the sleep phase for 29.5 minutes and a full tracking phase for 30 seconds. During the tracking phase the JP7 acquires satellites, computes position and updates ephemeris data as well the RTC is being calibrated.

The transition into the Push-to-Fix mode of JP7 can be implemented and configured by using the **Set Operating Mode** command in SiRFdemo. During the subsequent background cycles or when a user requests a position update (the RESET_N has to be used) a reset is generated and a hot start will be typically performed which may take up to a maximum of 8 seconds. The receiver wakes up, computes its position fix and goes back to the previous sleep phase again.

Hardware interface
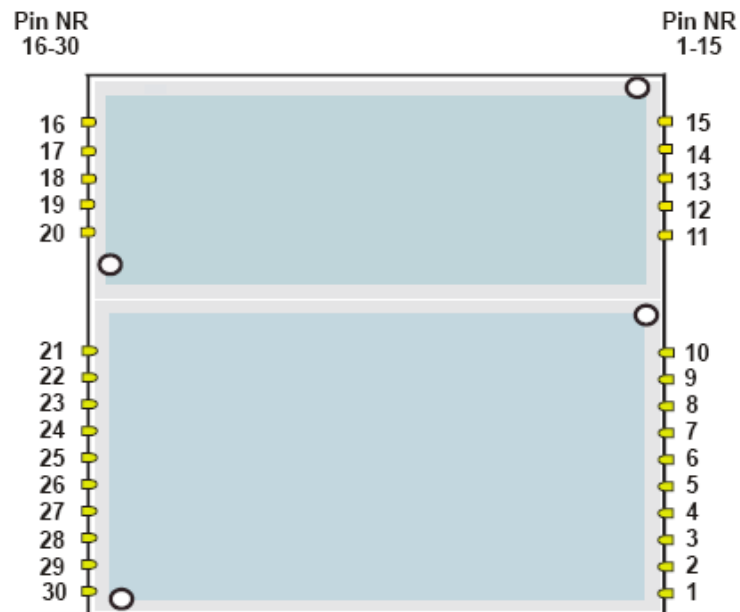
Pin	Name	I/O	Description	Level
1	VCC	I	Supply voltage	3.3 V DC
2	GND		Digital ground	
3	BOOTSELECT	I	Boots in update mode, if high	CMOS
4	SDI1	I	Serial Data Input A	CMOS

5	SDO1	O	Serial Data Output A	CMOS
6	SDO2	O	Serial Data Output B	CMOS
7	SDI2	I	Serial Data Input B	CMOS
8	GPIO3	I/O	See chapter 5.5.4	
9	RF_ON	O	High if RF part on RF chip is on	CMOS
10	GND		Digital ground	
11	RF_GND		Analog ground	
12	RF_GND		Analog ground	
13	RF_GND		Analog ground	
14	RF_GND		Analog ground	
15	RF_GND		Analog ground	
16	RF_GND		Analog ground	
17	RF_IN	I	50 Ohms @ 1.575 GHz	
18	RF_GND		Analog ground	
19	V_ANT	I	Power supply for active antenna	
20	VCC_RF	O	2.85V of RF section	CMOS
21	V_BAT		Power for RTC	+3 V DC ±5%
22	RESET_N	I	Resets the unit if low	CMOS
23	GPIO10	I/O	See chapter 5.5.4	CMOS
24	GPIO6	I/O	See chapter 5.5.4	CMOS
25	GPIO5	I/O	See chapter 5.5.4	CMOS
26	GPIO7	I/O	See chapter 5.5.4	CMOS
27	GPIO0	I/O	See chapter 5.5.4	CMOS
28	GPIO1	I/O	See chapter 5.5.4	CMOS
29	T-MARK	O	One pulse per second	CMOS
30	GND		Digital ground	

RESET_N (Pin 22)   This pin provides an active-low reset input to the board. It causes the board to reset and start searching for satellites. Reset is an optional input and, if not utilized, it may be left open.

T-MARK (Pin 29)   This pin provides 1 pulse per second output from the board, which is synchronized to within 1 microsecond of GPS time. The output is a CMOS level signal.

BOOT_SELECT (Pin 3) Set this Pin to high for programming the flash of the JP7 (for instance updating to a new firmware for the JP7).

SDI1   This is the main receiving channel and is used to receive software commands to the board from SiRFdemo software or from user written software.

SDI2   This is the auxiliary receiving channel and is used to input differential corrections to the board to enable DGPS navigation.

SDO1   This is the main transmitting channel and is used to output navigation and measurement data to SiRFdemo or user written software.

SDO2   For user's application.

VCC (Pin 1)	This is the main DC power supply for 3,3 V powered board JP7.
RF_IN (Pin 17)	Active antennas have an integrated low-noise amplifier. They can be directly connected to this pin (**RF_IN**). If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the correct voltage through pin **V_ANT**. **Caution:** Do not connect or disconnect the antenna when the JP7 is running. **Caution:** The RF_IN is always fed from the input voltage on the V_ANT. Do not use any input voltage on this pin.
V_ANT (Pin 19)	This pin is an input and reserved for an external DC power supply for an active antenna. The antenna bias for an external active antenna can be provided in two way to pin **V_ANT**. In order to use a 3.3 V, 5 V or 12 V active GPS antenna, the **V_ANT** has to be external connected to 3.3 V, 5 V or 12 V power supply respectively. The other possibility is available when you connect the **VCC_RF (pin 20)** output (which provides 2.85 V) to **V_ANT**, so that an antenna with 2.85 V supply voltage can be used. Hint: The input voltage on the **V_ANT** should be chosen in according to the antenna to be used. **Note: The GPS receiver JP7 has to be connected with an active 3 V GPS antenna (max. current of 25 mA). The antenna voltage is provided by the internal power management.**