5-11 GHz CMOS PA with 158.9 ± 41 ps group delay and low power using current-reused technique

Abstract

This paper proposes the design of a low group delay and low power ultra-wideband (UWB)power amplifier (PA) in 0.18 μm CMOS technology. The PA design employs two stages cascade with inductive peaking technique to provide broad bandwidth characteristic and higher gain while gain flatness can be achieved by connecting inter-stage circuit. A common gate current-reusedtechnique is adopted at the first stage amplifier to achieve good input matching, low groupdelay and low power. The simulation results show that the proposed PA design has an average gain of 11.5 dB with flatness of ±0.4 dB from 5-11 GHz, while maintaining bandwidth of 4.2-12.3GHz. An input return loss (S 11) less than -10.4 dB and output return loss (S 22) less than -9.5 dB, respectively are obtained. The PA design achieves excellent phase linearity (i.e., group delayvariation) of ±41 ps and only consuming 17 mW power from 1.2 V supply voltage. A good output 1-dB compression point OP1 dB of 3.7 dBm is obtained. By using this method, the proposed design has low group delay variation and lowest power among the recently reported UWBCMOS PAs applications.