

FPGA Based SPWM Bridge Inverter

¹M. N. Md Isa, ²M.I. Ahmad, ¹Sohiful A.Z. Murad and ¹M. K. Md Arshad

¹School of Microelectronic Engineering

²School of Computer and Communication Engineering

Universiti Malaysia Perlis (UniMAP). Blok A, Kompleks Pusat Pengajian Jejawi 1
Jalan Kangar-Arau, 02600 Jejawi, PERLIS, Malaysia

Abstract: This study presents methodology to generate sinusoidal pulse width modulation (SPWM) signal using Field Programmable Gate Array, FPGA technology. We discussed the unipolar switching scheme and the methodology to generate the signal with the predetermined switching frequencies. Simulation on the designed pulses was conducted using Altera Max Plus II simulation tools. This simulation method was used to get the desired sinusoidal pulse width modulated signal via programming. Designing the best switching frequency for inverter was important in order to get the best approximation of the sinusoidal signal as produced by an ideal inverter. The smoother inverter switching signal, the better output waveform from the inverter and thus produced output signal with less harmonics distortion. Simulation was done before being tested on the FPGA board for the next stage.

Keywords: Sinusoidal pulse width modulation (SPWM), unipolar SPWM, Field programmable gate array (FPGA), verilog, very high speed integrated circuit hardware description language (VHDL), inverter, power electronics

INTRODUCTION

Pulse width modulation (PWM) is widely used in power electronics to digitize the power so that a sequence of alternating voltage pulses can be generated by the on and off of the inverter power transistors. Inverter is defined as a converter that is used to change a dc input voltage to a symmetrical ac output voltage of desired magnitude and frequency^[1]. The output voltage of an ideal inverter is the sinusoidal waveform which could be fixed or variable at a fixed or variable frequency. For the PWM inverter, the harmonics spectrum exists at all odd number of harmonics. The low-pass filter design at the output of the inverter also can be quite difficult. Sinusoidal PWM is as the alternative due to the fewer harmonics introduced and it is widely used method for major AC appliances. The traditional method compares triangle wave which is used as carrier with the sinusoidal wave as the reference signal, whose frequency is the desired output frequency. The fundamental component is useful for any alternating current application.

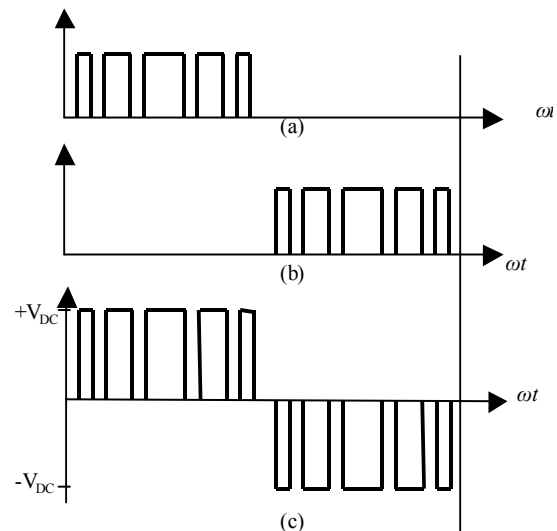


Fig. 1: The switching signals; (a) Channel 1, (b) channel 2 and (c) the expected unipolar SPWM

The switching strategy and the desired Unipolar SPWM output pulse from an inverter is shown in Fig. 1.

Table 1: Predetermined SPWM switching pulses

Time			Duty cycle (Hexadecimal)
t1	032	500 μs	06
t2	064	1000 μs	09
t3	096	1500 μs	0e
t4	0c8	2000 μs	12
t5	0fa	2500 μs	15
t6	12c	3000 μs	19
t7	15e	3500 μs	1b
t8	190	4000 μs	1d
t9	1c2	4500 μs	1e
t10	1f4	5000 μs	1e
t11	226	5500 μs	1e
t12	258	6000 μs	1d
t13	28a	6500 μs	1b
t14	2bc	7000 μs	19
t15	2ee	7500 μs	15
t16	320	8000 μs	12
t17	352	8500 μs	0e
t18	384	9000 μs	09
t19	3b6	9500 μs	06
t20	3e8	10000 μs	00

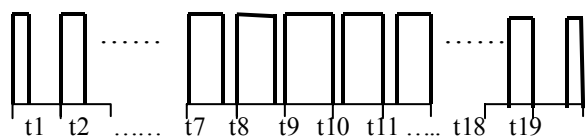


Fig. 2: Graphical view of the switching pulses

Table 2: The switching pulses characteristics.

Switching time	500 μs
Switching frequency	2.0 kHz
Dead time	500 μs
Number of pulses	38

The switching signals as shown in Fig. 1a and 1b are the desired SPWM signal for channel 1 and channel 2 respectively. Each channel is used to control a pair of inverter switches. The resultant output from a bridge inverter is shown in Fig. 1c. Designing switching pulses with high changes flexibility is the challenge in order to get the best approximation of the sinusoidal signal. This study presents the use of FPGA technology to design and implement the switching signals for channel 1 and channel 2 to produce the desired output signal from the bridge inverter. Each channel contributes half cycle of the inverter output waveform as illustrated in Fig. 1. This method eliminates the use of electronics component to generate the switching signals. Changes on the switching signal parameters such as the switching frequencies, the duty ratio and the number of pulses are easily control via verilog or VHDL programming language. The following section describes the method to generate the switching signals.

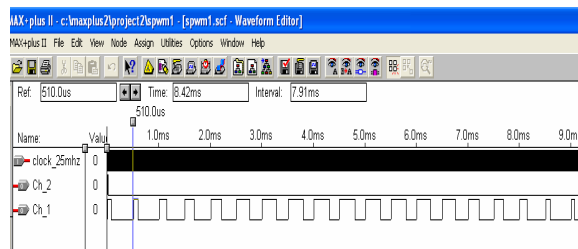


Fig. 3: The SPWM switching pulses from channel 1

Design method: The number of pulses, the switching time and the duty cycle generation are summarized in Table 1. The period for each cycle is fixed at certain calculated value and the duty cycle are then associated with the corresponding duty cycle.

The switching pulse characteristics as shown in Fig. 2 illustrates graphically the design strategy used to generate the single channel SPWM switching pulses. Time t1 represent the time for the predetermined duty cycle as tabulated in Table 1 is loaded. This next cycle is followed by t2 and this cycle continuous until the last cycle, t19. Then the dead time for the channel 1 switching pulse is loaded. The dead time is set as 500 μs which is acceptable for various types of power transistor. Typically, the switching devices consume only a few nanoseconds to operate as a switch. This delay time is necessary to avoid the damage on the inverter circuit during the switching pair transition. This cycle produce half cycle of the inverter output waveform with 19 switching pulses and one dead time. The channel 2 then produces another cycle sequentially. This cycle again produce 19 pulses and one dead time. The total time and for the full cycle is then calculated as follow:

No. of switching pulses = 38 pulses x 500 μs = 19.00ms
 Total time + dead time = 40 pulses x 500 μs = 20.00ms
 Output Frequency = 50.0 Hz.

This approach basically shall produce the desired frequency, duty cycle and the number of pulses. Table 2 summarized all the calculated parameters.

RESULTS

The predetermined switching pulse is then implemented using VHDL programming with Max Plus II environment. The simulation is performed and the result is shown in Fig. 3.

The result shows that the switching pulses generated with only two percent difference from the predetermined switching frequency. The output frequency from the simulation produces 49.02 Hz with the switching frequency of 1.96 kHz.

CONCLUSION

As a conclusion, the design of the switching pulses using FPGA technology shall produce better control signal for inverter switches. The predetermined and pre-calculated switching parameters; frequency, amplitude and duty cycle are easily verified via Altera-Max-plus II simulation tools. In addition, with the high programming flexibility, the design of the switching pulse can be further altered easily without any further changes on the hardware. Therefore, the switching parameters can be determined prior to the hardware implementation. The result shows that the difference is only three percent from the predetermined parameters. It is also proved that the SPWM switching frequency, the number of pulses and the duty cycle generation are flexible. Small differences on the output from the inverter may be acceptable for low and medium power applications such as for an AC motor drive, where the filtering stage is not required^[3]. In some applications such as for designing the uninterruptible power supplies (UPS), high purity sine wave output is required. For this case, the number of pulses can be easily altered via this method to get the best approximation to the desired sinusoidal wave. The waveform can be easily monitored from the waveform simulation tools provided by Max Plus II for future modification before being downloaded into the FPGA board. The successful switching pulses design is then integrated with the inverter circuit to produce the best sinusoidal signal. Higher switching frequency shall be tested and easily monitored using this proposed method. This approach also eliminates the use of more electronic components.

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