AN EFFICIENT MODIFIED BOOTH MULTIPLIER ARCHITECTURE

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An Efficient Modified Booth Multiplier Architecture

by

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AN EFFICIENT MODIFIED BOOTH MULTIPLIER ARCHITECTURE

ABSTRACT

Multiplier plays an important role in today's compute intensive applications such as computer graphics and digital signal processing. This thesis described the design of an Efficient Modified Booth Multiplier Architecture. With the tradeoff between speed and area, the design of the Modified Booth Multiplier focused on high speed with a moderate increase in area. This was achieved by reducing the critical path delay in the basic element of the multiplier circuit. Multiplication is performed by generating the partial product of Modified Booth Encoding (MBE) and accumulating the entire partial product by an adder or compressor. The research began by examining the available encoding schemes used to generate the partial product and 4:2 compressor that are used to accumulate the partial product. The fastest MBE and the most efficient 4:2 compressor has been used to develop the multiplier. The multiplier performance was improved by adapting various methods such as Simplified Sign Extension (SSE) and a proper tree topology. The SSE method eliminated some counter or adders in a partial product row while the tree topology arrangement of the compressors and their interconnection accumulate the partial product. A Gajski's rule had been used to evaluate the performance of the multiplier and the result shows that the new multiplier has reduced delays in producing the output. The new multiplier architecture has reduced delays to almost 2% to 7% compared to other multipliers. The high speed multiplier was then extended to develop a Floating Point (FP) multiplier. The FP multiplier had been successfully designed using Altera Quartus II software and implemented on MAX EPM7182SLC84-7 device. The result showed that the FP multiplier is 38% faster compared to conventional FP multiplier. In term of size, the FP multiplier is 26% bigger than conventional circuit. However the increase in area of the circuit can be tolerated since the aim was to enhance the speed of the FP Multiplier

PENAMBAHBAIKAN SENIBINA PENDARAB BOOTH DIUBAHSUAI

ABSTRAK

Pendarab memainkan peranan penting dalam aplikasi intensif komputer seperti grafik komputer dan pemprosessan isyarat digit. Tesis ini adalah mengenai rekabentuk sebuah Pendarab Booth Diubahsuai yang diubahsuai senibinanya. Dengan faktor penghad seperti kelajuan dan keluasan, rekabentuk Pendarab Booth Diubahsuai ini hanya memberi penekanan kepada kelajuan yang tinggi walaupun peningkatan saiz yang tidak begitu ketara. Pendarab Booth Diubahsuai ini dapat dicapai dengan mengurangkan masa laluan genting dalam litar asas pendarab. Proses pendaraban dapat dilaksanakan dengan menghasilkan Produk Separa Pengekod Booth Diubahsuai (MBE) dan mencampurkan Produk Separa dengan litar penambah atau litar pemampat. Penyelidikan ini telah dimulakan dengan menganalisa pengekodan yang sedia ada bagi menghasilkan Produk Separa dan Pemampat 4:2 yang digunakan untuk mencampurkan Produk Separa. Litar MBE yang berkelajuan paling tinggi dan Pemampat 4:2 yang paling effisien akan digunakan bagi membina litar pendarab. Prestasi pendarab telah diperbaiki dengan menambah beberapa kaedah seperti kaedah Simplified Sign Extension (SSE) dan menggunakan topologi pokok yang sesuai. Kaedah SSE digunakan untuk menghapuskan sebahagian litar penambah atau litar pemampat dalam barisan produk separa manakala topologi pokok adalah susunan penyambungan litar pemampat bagi mencampurkan kesemua produk separa. Peraturan Gajski telah digunakan untuk menilai prestasi litar pendarab dan hasil keputusan menunjukkan pendarab baru mengurangkan masa dalam menghasilkan keluaran. Pendarab baru mengurangkan masa pendaraban diantara 2% hingga 7% berbanding pendarab yang lain. Pendarab berkelajuan tinggi kemudiannya dilanjutkan untuk membangunkan satu pendarab titik terapung (FP). Pendarab FP ini telah berjaya dibina dengan jayanya menggunakan perisian Altera Quartus II dan diimplemntasikan diatas peranti MAX EPM7182SLC84-7. Hasil menunjukkan litar pendarab FP adalah 38% lebih laju berbanding litar pendarab yang biasa. Saiz litar pendarab FP adalah 26% lebih besar berbanding litar biasa. Namun, saiz litar boleh ditoleransi memandangkan matlamat adalah menambahbaik kelajuan pendarab FP.

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ABBREVIATION

CAD – **C**omputer **A**ided **D**esign

FPGA – **F**ield **P**rogrammable **G**ate **A**rray

FP – **F**loating **P**oint

MBE – **M**odified **B**ooth **E**ncoding

MBM – **M**odified **B**ooth **M**ultiplier

PP – **P**artial **P**roduct

SSE – **S**implified **S**ign **E**xtension

Verilog HDL – **Verilog H**ardware **D**escription **L**anguage

VLSI – **V**ery **L**arge **S**cale **I**ntegrated

CHAPTER 1

Background

1.1 Introduction

This chapter started with explaining the background of multiplier. The history of Booth algorithm, compressor and simplified sign extension were described. The objectives and scopes of research were also described in detail. Generally, this chapter reviews the reason to improve the performance of Modified Booth Multiplier.

1.2 Research background

With the constant growth of computer applications such as computer graphic and signal processing, fast arithmetic unit especially multipliers are becoming increasingly important. Advanced VLSI technology has provided the designer the freedom to integrate many complex components, which was not possible in the past. Over the years various high speed multipliers have been proposed and realized (Booth 1951; Sorley 1961; Wallace 1964; Lim 1978; Villeger and Oklobdzija 1993; Hsin-Lei, Chang et al. 2004). Multipliers play an important part in today's digital signal processing (DSP) systems. Examples of their use include implementations of digital filters, discrete Fourier transform, correlations and many others.

In any multiplication algorithm, the operation is decomposed into a partial product generation and partial product summation. Each partial product represents a multiple of the multiplicand to be added to the final result. Previously reported multiplication algorithms mainly focus on rapidly reducing the partial products rows down to the final sums and carries used for the final accumulation. These techniques mostly rely on the circuit optimization and minimization of critical paths (Kang and Gaudiot 2004). Various algorithms for reducing the number of partial product have been proposed. One of the earliest algorithms is Booth algorithm (Booth 1951). Ever since its first introduction, it has been a popular encoding technique used to reduce the number of steps in the multiplication process. The Modified Booth Algorithm performs the encoding in parallel and is widely implemented in fast multiplier design.

In the accumulation part, all partial products must be accumulated to obtain the final result. The accumulation of partial product can be accomplished by using adder or compressor. The arrangement of adder or compressor to accumulate the partial product also affects the delays to produce the final result. A fast tree topology structure such as the Wallace tree can be employed for high speed accumulation.

In 2003, Ercegovac (Ercegovac 2003) proposed simplified sign Extension (SSE) which can speed up addition process. Ever since the SSE method got introduced, it has always been used and developed because it renders the advantage of reducing the adder's block. As a result, the total delay to produce the final result also reduces.

The combination of MBE and adder or compressor will produce a Modified Booth Multiplier (MBM). On top of that, the implementation of proper tree topology and SSE method will enhance the performance of the multiplier. This efficient multiplier has also been extended to the Floating Point (FP) multiplier as a proof of the efficiency of this multiplier.

1.3 Research statement

The limitation in designing a high performance IC or microprocessor was limited by the multiplier latency. In increasing the performance of this device, many researchers modified or improved the performance of their multiplier module. In recent years, various type of multiplier can be implemented in devices, but the most popular multiplier module was Modified Booth Multiplier. Hence, this research is focused on improving the MBM module to speedup the performance of multipliers.

The multiplier consists of two operations namely generating the partial product and accumulating the partial product. In generating the partial product, several types of MBE have been identified and evaluated for the best performance. As a result, the MBE which has the fastest speed up time will then be used to develop the efficient multiplier.

The result of multiplication or final product can be obtained by accumulating the partial product by adder or compressor circuit. In most situations, the compressor is used to generate the final product. This is due to the advantages of compressor when accumulating compared to the adder. Thus, in this study the compressor is used. The compressor has been evaluated and optimized before being implemented in the multiplier.

Generally, in partial product's accumulation process, counter and adder will affect the multiplier performance. In contrast, there are two other criterion that contribute to the same problem. The first criterion is the type of tree topology used during the partial product summation. The next criterion is SSE method. Flynn (Flynn and Oberman 2001) wrote details about the tree topology in their research. This study has verified the tree topology as having better performance. Hence, this work will adapt this tree topology in implementing a high speed multiplier.

The SSE Method currently will improve the total propagation delay in generating the results by eliminating a few adder or counter modules. Indirectly, it will reduce the size of the multiplier. However, there is a problem when implementing the SSE method with the Booth Encoding. The issue is, when the S signal that is generated

by Booth Encoder depends only on y_{i+1}. This study has investigated the issue of designing a high speed multiplier in the context of an entire system.

1.4 Research Objectives

The research work consists of four main objectives:

i. To design an efficient MBE. This MBE can produce a correct partial product when implementing with the SSE method.

ii. To design an efficient compressor to enhance the accumulation process

iii. To design a high performance Modified Booth Multiplier using new MBE and compressor. Further, the SSE method and faster tree structure are to be implemented to further enhance the performance.

iv. To improve the performance of Floating Point Multiplier by utilizing the high performance Modified Booth Multiplier.

1.5 Research Methodologies

The availability of computer-based tools has greatly influenced the design process in a wide variety of design environments. For this project, a set of design methodologies are constructed which is similar to semi custom design technique to meet the research requirement. The flowchart shown in Figure 1 describes a development process. The most obvious requirement for this process is that the system must function properly at each level and must meet an expected level of performance.

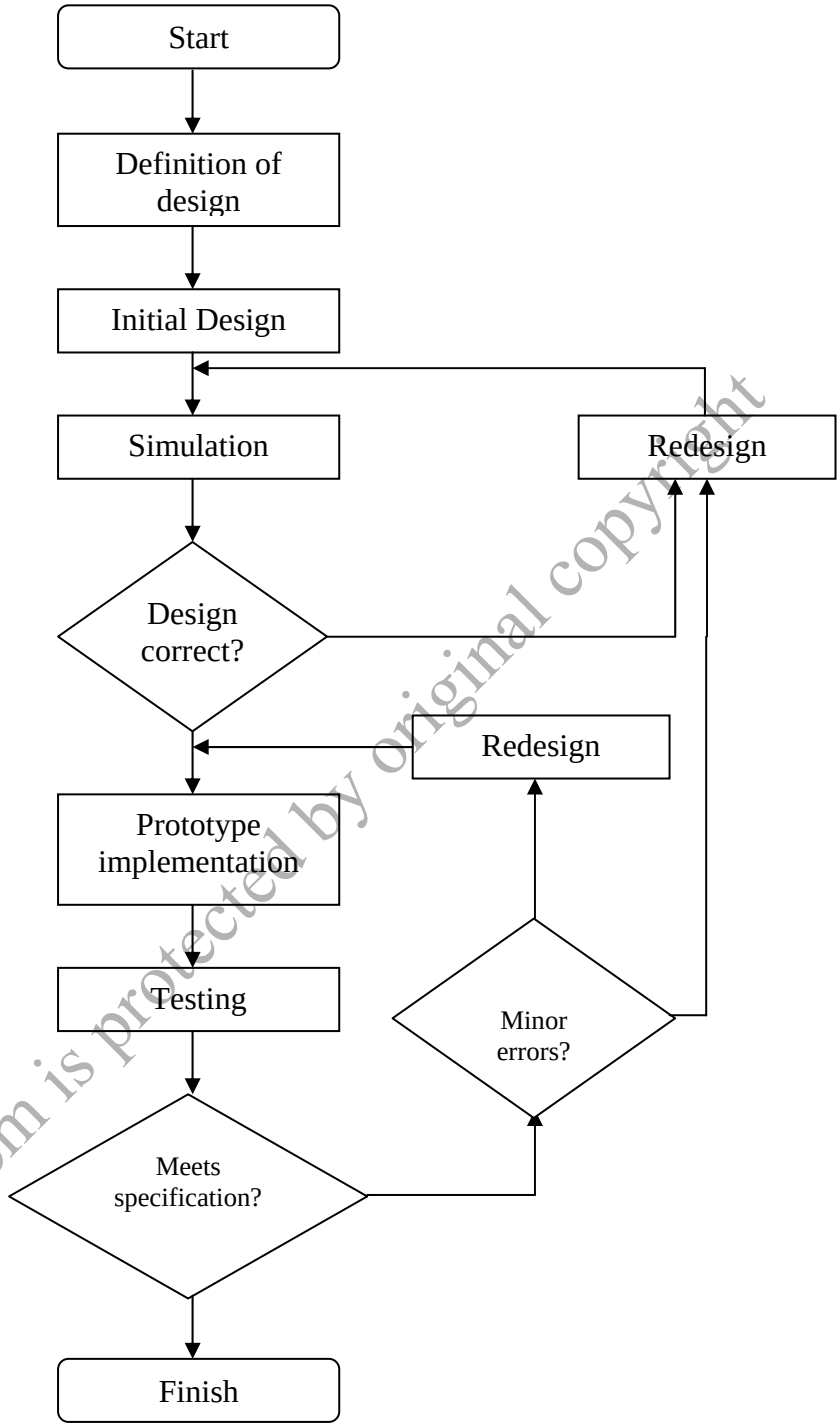

Figure 1.1: The development process.

The process begins with the definition of design specifications. The essential features of the system are identified and an acceptable method of evaluating the implemented features in the final design is established. The specifications must be followed to ensure that the developed system meets the general expectations.

From a complete set of specifications, the system is designed efficiently using schematic entry and Verilog Hardware Description Language (Verilog HDL) codes. After the general structure is established, CAD tool known as Quartus II 6.1 Web Edition is used to simulate the behavior of the system and such simulations are used to determine whether the system meets the required specifications. If errors are found, then appropriate changes are made and the verification of the new design is repeated through simulation.

When the simulation indicates that the design is correct, a complete physical prototype of the product is constructed. For this project, Altera UP2 FPGA board is used as a physical prototype to implement the final design of the system. The prototype is thoroughly tested for conformance according to the specifications. Any minor or major errors occurred in the testing mode must be fixed. In case of major errors, it is necessary to redesign the system and repeat the initial step as explained above. When the prototype passes all the tests, then the system is deemed to be successfully designed.

1.6 Thesis Structure

This thesis consists of seven (7) chapters. Each of the chapter is described as follows:

Chapter 1 describes the problem background, research statement, research scope, research methodologies and thesis structure.

Chapter 2 focuses on outlines the background knowledge required for understanding the previous work related to this project. This chapter also discusses the Modified Booth algorithm, tree topologies and compressor that have been used recently by other researchers. This chapter also describes the Floating Point architecture.

Chapter 3 demonstrates the analysis and simulation of existing MBE and existing compressor. Some of the existing MBE will be analyzed. The result from the analysis will be useful in Chapter 4 when designing a new MBE. Finally, the results will also be compared with several existing design techniques in terms of propagation delay, speed and hardware costs. Also in this chapter, the existing compressor will be analyzed. The design which offers the lowest delay performance and hardware costs will be determined.

Chapter 4 shows how to design the new MBE and new compressor based on the problem discussed in Chapter 3.

Chapter 5 explains the steps in building or constructing a high speed Multiplier by using MBE and compressor which are designed in Chapter 4. The idea of using binary tree adder is to look for the advantages of MBE and compressor compared to existing designs.

Chapter 6 demonstrates how to improve the Floating Point Multiplier. Building FP Multipliers requires development of an efficient MBM and implementing it into FP Multiplier module. The efficient MBM consists of the new MBE and compressor with the SSE method implemented in the accumulation section. Finally, the Wallace tree has also been adopted in this efficient MBM.

Finally yet importantly, Chapter 7 clarifies the results based on objectives. The promising recommendations were given to improve this project in future. The problems occurred during completing this project were also presented.

CHAPTER 2

Literature Review

2.1 Introduction

This chapter presents the multiplication algorithm which focuses on parallel multiplier namely Modified Booth Multiplier. The architecture involved in this multiplier also revealed in order to understand their characteristics. The element of multiplier namely Modified Booth Encoding, compressor, Simplified Sign Extension, reduction tree organizations and Floating Point multiplier in previous study were demonstrated.

2.2 Multiplication Algorithm

Multiplication is a less common operation than addition, but still essential for microprocessors, digital signal processors and graphic engines. The most basic form of multiplication consists of forming the product of two binary numbers. This can be accomplished through the traditional technique taught in primary school, simplified to base 2.

M x N bit multiplication can be viewed as forming N partial product of M bits each, and then summing the appropriately shifted partial product to produce an M + N –

bit result P. Binary multiplication is equivalent to a logical AND operation. Therefore, generating partial products consists of the logical ANDing of the appropriate bits of the multiplier and multiplicand. Each column of partial products must then be added to produce a final result.

The number of partial product also can determine the performance of the multiplication. This number of partial product can be reduced using Modified Booth Encoding (MBE). Therefore Modified Booth Algorithm is better in reducing the circuits. Performance of this circuit will be explored and used

There are many factors that will contribute to the multiplier performance including Modified Booth Encoding design, adder design, Simplified Sign Extension method and reduction tree organizations. This chapter explains more about MBE's architecture, Compressor design adder tree and Simplified Sign Extension. At the end of this chapter, the Floating Point Multiplier will be explained briefly.

2.3 Modified Booth Multiplier Architecture

A Modified Booth Multiplier consists of three distinct components. They are the Booth Encoder, Booth Selector and adder tree. The combination of Booth Encoder and Booth Selector are called Modified Booth Encoding (MBE). The function of MBE circuit is to produce the partial product. The Modified Booth Multiplier will generate only 4 partial products if the multiplication input is 8 bit. Unlike the Shift and ADD or basic multiplier, the total partial product produced is 8 bit if the multiplication input is 8 bit.

The accumulation of all partial products is done in the adder tree circuit. The adder tree circuit contributes the most amount of delay in the multiplier performance. There are a lot of methods that has been implemented in the adder tree circuit to enhance the multiplier performance. In this research, three components were discussed namely the adder or compressor circuit, the adder tree topology and the Simplified Sign Extension (SSE) method. Figure 2.1 shows the high level block diagram of the

Modified Booth Multiplier.

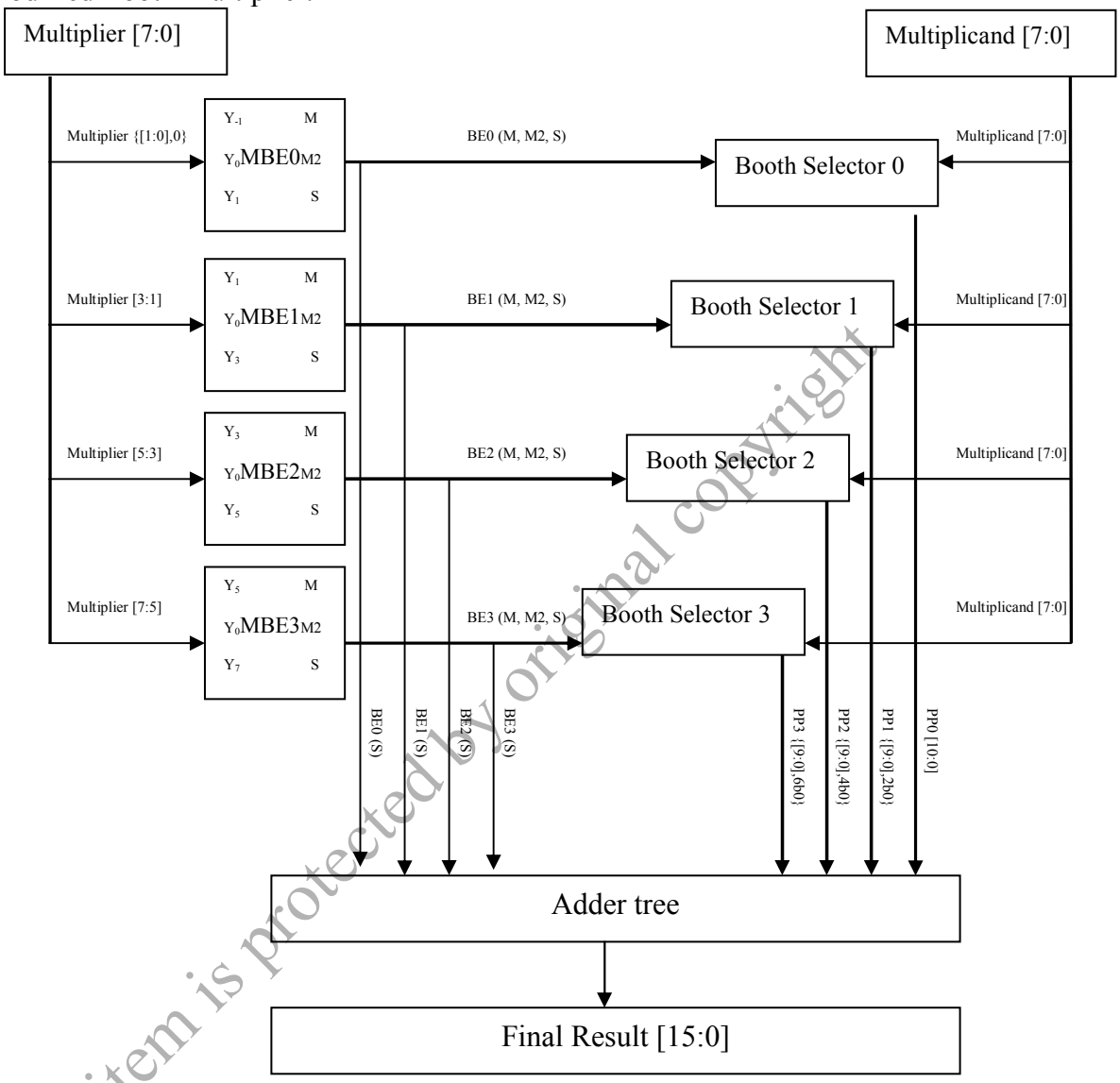

Figure 2.1: Modified Booth Multiplier block diagram

2.4 Modified Booth Encoding

The Modified Booth algorithm was proposed by Macsorley (Macsorley 1961). The basic idea is that, instead of shifting and adding every column of the multiplier term and multiplying by '1' or '0', the multiplier bits are grouped in blocks of three. Grouping starts from the LSB, and the first block only uses two bits of the multiplier (since there is no previous block to overlap).