

## CHAPTER 1

### INTRODUCTION

#### 1.1 Background History

A high speed multiplier is an electronic computing unit used to provide multiplication processes at very high speed by incorporating various types of logics. The most basic form of multiplication consists of forming the product of two unsigned (positive) binary number [1]. This can be accomplished through traditional technique simplified to base 2. For example, the multiplication of two positive 4-bits binary integers,  $12_{10}$  and  $5_{10}$ , proceeds as shown in Figure 1.1.

	1100	Multiplicand
x	0101	Multiplier
	-----	
	1100	] Partial Products
	0000	
	1100	
	0000	
	-----	
	00111100	Product

**Figure 1.1** : Multiplication example

M x N-bit multiplication can be viewed as forming N partial products of M bits each, and then summing the appropriately shifted partial products to produce an M+N-bit result P. Binary multiplications is equivalent to a logical AND operation. Therefore, generating partial products must then be added and, if necessary, any carry values passed to the next column.

## 1.2 High Speed Multiplier

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of following – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier, thus making them suitable for various high speed, low power, and compact VLSI implementation [2].





High speed multiplier can be classified into three general types [5]. The first generates all partial products in parallel and then uses a fast multi-operand adder for their accumulation. This is known as a parallel multiplier. The second, known as a high speed sequential multiplier, generates the partial products sequentially and adds each newly generated product to the previously accumulated partial product. The third is made up of an array of identical cells that generate new partial products and accumulate them simultaneously. Thus, there are no separate circuits for partial product generation and for their accumulation. This is known as an array multiplier.

The speed of the multiplier is determined by both architecture and circuit [6]. The speed can be expressed by the number of the cell delays along the critical path on the architecture level of the multiplier. The cell delay, which is normally the delay of the adder, is determined by the design of the circuit of the cell.

One important complication in the development of efficient multiplier implementations is the multiplication of two's complement signed numbers. The Baugh-Wooley Two's Complement Signed Multiplier is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier logic and allows all the partial products to have positive sign bits [3]. Thus, this project will prove that this type of multiplier is one of the high speed multiplier.

### 1.3 Objective

The objectives of this project are :

-  To do literature review to study high speed multipliers
-  To select the best high speed multiplier
-  To prove that Modified Baugh-Wooley Two's Complement Signed Multiplier is a high speed multiplier
-  To improve the speed performance of Modified Baugh-Wooley Two's Complement Signed Multiplier