8-BITS X 8-BITS MODIFIED BOOTH 1'S COMPLEMENT MULTIPLIER

by

NORAFIZA SALEHAN

Report submitted in partial fulfillment
of the requirements for the degree
of Bachelor of Engineering
(Electronic Enginering)

MAY 2007

ACKNOWLEDGEMENT

I would like to take this opportunity to thank everybody who helped in any way for this project. I would like to express my gratitude and respect to my project supervisor, Madam Norina Idris for her advice, guidance, supervision, patience and understanding throughout this project.

I would like to thank my friends for all their support and friendship and I would like to wish them good luck in their future. To my family especially my parents, for their love, support and encouragement.

Last but not least, to the School of Microelectronic Engineering of Universiti Malaysia Perlis for providing the facilities that enable the success of this project.

PENDARAB 8-BIT X 8- BIT PELENGKAP 2 TERTANDA BAUGH-WOOLEY TERUBAHSUAI

ABSTRAK

Dengan kemajuan dalam teknologi, banyak penyelidik telah cuba dan mencuba mereka bentuk pendarab yang menawarkan samaada – kelajuan yang tinggi, penggunaan kuasa rendah, dan penggunaannya dalam Kamiran Berskala Sangat Besar, oleh itu membuatkan ia sesuai untuk pelbagai penggunaan seperti kelajuan tinggi, kuasa rendah Kamiran Berskala Sangat Besar yang padat. Projek ini memberi tumpuan kepada kelajuan Pendarab 8-Bit x 8-Bit Pelengkap 2 Tertanda Baugh-Wooley Terubahsuai. Tiga cara untuk meningkatkan kelajuan pendarab – mengurangkan bilangan produk-produk separa, menambahkan kelajuan penambahan produk-produk separa dan 'pipelining'. Kelajuan Pendarab 8-Bit x 8-Bit Pelengkap 2 Tertanda Baugh-Wooley Terubahsuai, ditingkatkan dengan mengurangkan produk-produk separa dan kemudian menjumlahkan produk-produk separa ini dengan menggunakan 'Carry Save Adder'. Analisis kelajuan prestasi Pendarab 8-Bit x 8-Bit Pelengkap 2 Tertanda Baugh-Wooley Terubahsuai ini dibuat menggunakan Altera Quartus II . Projek ini membuktikan bahawa Pendarab ' mempunyai prestasi kelajuan yang tinggi dan analisa kelajuan pada EPF10K70.

ABSTRACT

With advances in technology, many researchers have tried and are trying to design multipliers which offers either of following – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier, thus making them suitable for various high speed, low power, and compact VLSI implementation. This project focuses on speed performance of the Modified Baugh-Wooley Two's Complement Signed Multiplier. Three methods to improve speed performance of the multiplier – reduce the number of partial products and accelerate the accumulation have been discussed in literature view. For Modified Baugh-Wooley Two's Complement Signed Multiplier the speed is improved by reducing the partial products and then summing these partial products using Carry Save Adder. The schematic design as well as speed performance analysis of this multiplier is done using Altera's Quartus II Software and speed obtained on EPF10K70.

TABLE OF CONTENTS

Figures No. **Page**

LIST OF FIGURES

LIST OF TABLES