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Appendix A



Appendix A (i) : FA block symbol



Appendix A (ii) : 4-bit CSA



Appendix A (iii): 4-bits RCA



Appendix A (iv): 17-bits RCA

APPENDIX B



Appendix B(i) : Binary to Seven Segment Decoder

	Value at	0 ps 10	1.0 ns 20.	0 ns 30.	0 ns 40.	.0 ns		
Name	20.48 ns	20.475 ns						
🗄 D	H A43C	(A438	<u>х́</u> А43А	A43C	A43E	X A440		
.∎ E	H 7BF7	(78F3	<u>х 7</u> вғ5	7BF7	7BF9	X 7BFB		
⊞ F	H 42FA	(42F6	X 42F8	42FA	42FC	42FE		
±Α	H 0004	(0000	ý 0002	0004	0006	X 0008		
🛨 B	H 335E	(335A	X 335C	335E	3360	3362		
. E	H 853B	8537	× 8539	853B	853D	X 853F		
Couto 1	BO							
Couto2	H1							
Couto3	HO							
🗄 Sum	H C673	C64B	<u>Х С67</u> F	C673	C627	X C61B		
	H 2AAD	(2AB5	X 2AA1	2AAD	2AD9	2AE5		

Appendix C(i) : The functional simulation mode of three levels six operands 16-bits CSA design

		Value at	0 ps 10.	0 ns 20	0 ns 30	.0 na
	Name	20.48 ns		2	0.475 ns	
• 🗉	D	H A43C	(A438	(A43A	X A43C	X A43E
¥ 🛨	E	H 7BF7	(7BF3	(7BF5	78F7	X 78F9
<u>ا</u>	F	H 42FA	42F6	(42F8	42FA	X 42FC
ا	A	H 0004	0000	X 0002	X 0004	X 000e
ا	в	H 335E	((335C	X 335E	X 3360
¥ 🛨	c	H 853B	(8537)	(8539	X 8538	X 853D
2	Couto1	B 0				
2	Couto2	H 1				
۶.	Couto3	H O				
1 🗆	Sum	H C64B	(C64B		
è.	- Sum 15	B 1				
2	-Sum14	B 1				
2	-Sum13	BO				
4	-Sum12	BO				
Þ.	-Sum11	B 0				
2	- Sum 10	B 1				
2	- Sum9	B 1				
2	- Sum8	BO		`		
2	-Sum7	BO				
2	- Sum6	81				
2	- Sum5	80				
-	-Sum4	80				
H	- Sum3	0.0				
H	Sum2	0.1				
-	Suma	D 1				
s m	Court	H 24R5	/	2405		
Η Ξ		112/05	<u> </u>	2003		

Appendix C(ii) : The timing simulation mode of three levels six operands 16-bits CSA design

Name	1	Value at	50	0 ns 60	.0 ns 70	.0 ns
	4	20.46 NS				
🗄 D	1	H A43C	A440	X A442	X A444	X
ΞE		H 7BF7	78F8	7BFD	X 78FF	X
. F		H 42FA	42FE	4300	X 4302	χ
ΞA		H 0004	0008	X 000A	X 000C	χ
🛨 B		H 335E	3362	3364	X 3366	X
ΞC		H 853B	853F	X 8541	X 8543	X
Couto 1	1	BO				
Couto2	2	H1				
Couto3	3	HO			billing and state	
🖃 Sum	1	H C64B	\$\\C653\C673\\\\\\C677_\67\\\\\	73_(67)(C67F)(C677)()(_C67F_)(5673)()()(C673_)(_C67	7E((()(66)())(5)(5)(()(63)()(C62F)(())()(C627)()(C	63B (63 (C66F)50
-Su	um15	B1				
⊢S.	um 14	B1				
⊢s.	um13	BO				
⊢s.	um12	BO				
-su	um11	BO				
-Su	um 10	B1				
-Su	um9	B1				
-SL	um8	BO				
⊢s.	um7	BO				
-Su	um6	B 1				
-Su	um5	BO				
-Su	um4	BO				
⊢S.	um3	B 1				
⊢s.	um2	BO				
-SL	um1	B 1	10	IU	ΙU	
-Su	umo	81			AT 100 00 00 00 00 00 00 00 00 00 00 00 00	
t Cout		H 2AB5	ZAAS X ZAAB XUZZAASX ZAAT XX 3	anau kanasinsky kansisky kansi	AT KANAKAA KAA KOKKOGAK ZACT X ZADA XIX 2	AND THERE
		App	endix C(iii) : The continued tim	ing simulation mode of three levels	s six operands 16-bits CSA design	

	Value at	0 ps 10.	0 ns 20.0) ns	30.	0 ns	40.	Ons		
Name	21.6 ns			21.6	21.6 ns					
🗄 D	H A43C	A438	x A43A x		A43C	(A4	3E)	(A440		
🗄 E	H 7BF7	7BF3	(<mark>7</mark> 8F5)		7BF7	(7B	F9	(7BFB		
🖽 F	H 42FA	42F6	X 42F8 X		42FA	(42	FC	(42FE		
🛨 A	H 0004	0000	x 0002 x		0004	(00	06	0008		
🛨 B	H 335E	(335A	X 335C X		335E	(33	60	3362		
. E C	H 853B	8537	x 8539 x		853B	(85	3D)	(853F		
Couto1	H O									
Couto2	H O									
Couto3	H O									
CLK	BO						,			
🛨 Sum	H 0001	(0000	X 000	01	X 02	25	(<u>C</u> 6	5F	XC673	
🛨 Cout	H 0001	(0001				(<u>2</u> A	B1	2AAD	

Appendix C(iv): The functional simulation mode of modified of three levels six operands 16-bits CSA design

		Value at	0 ps 10	0 ns	20.0 ns		30.0 ns	40.) ns
	Name	21.6 ns				21.6 ns			
(FI)	D	H A43C	(A438	X A43A	Ý	A43C	Ý	A43E	A440
	E	H 7BE7	78F3	78F5		78F7	=\$	78F9	78FB
	F	H 42FA	42F6	42F8		42FA		42FC	42FE
E	A	H 0004	0000	0002	Ŷ	0004		0006	0008
E	в	H 335E	(335A	X 335C		335E	÷,	3360	3362
	c	H 853B	8537	8539	ý	853B	=ý	853D	853F
_	Couto 1	HO							
	Couto2	но							
	Couto3	но							
	CLK	BO							
=	Sum	H 0000		0	0000			0001	0205 02
	-Sum15	BO							
	-Sum14	BO							
	- Sum 13	BO							
	-Sum12	BO							
	-Sum11	BO							
	-Sum10	BO							
	-Sum9	BO				Tpd	\rightarrow		
	-Sum8	B 0		<u> </u>		-ipu			
	-Sum7	BO							
	-Sum6	BO							
	-Sum5	BO							
	-Sum4	B 0							
	-Sum3	BO							
	-Sum2	BO							
	-Sum1	BO							
1	L_Sumo	B 0							
±	Cout	H 0001	<			0001			

Appendix C(vi) : The timing simulation mode of modified three levels six operands 16-bits CSA design

	Value at	0 ps 10.	0 ns 20.	Ons	30.0 ns	40.0 ns				
Name	27.97 ns			27.965	9 ns					
ΞA	H 0004	0000	0002	0004	X 0006	X 0008				
🛨 B	H 335E	335A	335C	335E	3360	3362				
⊞ C	H 853B	8537	8539	853B	x 853D	X 853F				
🗄 D	H A43C	(A438	A43A	A43C	<u>А43</u> Е	X A440				
ΞE	H 7BF7	(78F3	7BF5	7BF7	Х 7ВF9	X 7BFB				
∃ F	H 42FA	42F6	42F8	42FA	42FC	42FE				
🗉 Sum	H 2056E	(1456B	2856B	2056B	2FD6B	1696B				
Cout	H1			j						

Appendix C(vi) : The functional simulation mode waveform of three levels of six operands 16-bits CSA with RCA

	Value at	0 ps 10.	0 ns 20.	0 ns	30.0 ns	40.0 ns
Name	27.97 ns			27.96	9 ns	
TH A	H 0004	0000	0002	0004	Ý 0006	Ý
ΞB	H 335E	335A	335C	335E	X 3360	Ŷ
	H 853B	8537	X 8539	853B	X 853D	Ŷ
. D	H A43C	A438	X A43A	(A43C	X A43E	Ŷ
ΞE	H 7BF7	(78F3	7BF5	(78F7	X 78F9	- X
€ F	H 42FA	42F6	42F8	42FA	42FC	X
🖃 Sum	H 1456B	C	14	568		X3456B X14
Su	BO					
Su	B1					
Su	B 0					
Su	B1					
Su	B0		5 5 5			
Su	80					
Su	BO					
Su	B1				Tpd	
- Sum9	BO					
-Sum8	B1					
-Sum7	80					
Sumb	81					
Sumb	81					
	BU 01					
_ Sum2	80	1				
-Sum1	B1					
	B1					
Cout	H1					_
Cout	B1 H1					

Appendix C(vii) : The timing simulation mode waveform of three levels of six operands 16-bits CSA with RCA



Appendix C(viii) : The continued timing simulation mode waveform of three levels of six operands 16-bits CSA with RCA

	Value at	0 ps 10	.0 ns 20).0 ns	30.0 ns	40.0 ns
Name	21.03 ns			21.025 ns		
			1			
CLK	BO					
ΞA	H 2F3B	2F37	X 2F39	X 2F3B	2F3C) 2F3F
🛨 B	H 5A7F	(5A7B	X 5A7D	X 5A7F	5A81	X 5A83
. C	H 6C26	(6C22	<u>x</u> 6C24	X 6C26	ý 6C28	3 X 6C2A
± D	H C43C	C438	C43A	<u>C43C</u>	C43E	C440
ΞE	H 9BF7	9BF3	<u>у</u> 98F5	<u>%</u> 9ВF7	<u>9</u> 8F9) X 9BFB
∃ Γ	H B2FA	B2F6	B2F8	B2FA	B2FC	C X B2FE
🗄 Sum	H 00005	(<u> </u>	004 <u>(</u> 00	φο5 χ	20005 X	28¢6A (3F90E
Cout	HO					

Appendix C(ix) : The functional simulation mode of modified three levels six operands 16-bits CSA with RCA design

	Value at	0 ps 10	.0 ns 2	0.0 ns	30.	0 ns 40	.0 ns	50.0 ns
Name	21.03 ns			21.025	ōns			
ΞA	H 2F3B	2F37	2F39	X	2F3B	2F3D	2F3F	ý :
ΞB	H 5A7F	5A7B	X 5A7D	X	5A7F	5A81	X 5A83	(!
🗄 C	H 6C26	6C22	<u>6C24</u>	X	6C26	6C28	(6C2A	<u> </u>
ΞD	H C43C	C438	<u>C43A</u>	X	C43C	C43E	X C440	X (
ΞE	H 9BF7	9BF3	98F5	X	9BF7	9BF9	y 9BFB	9
ΞF	H B2FA	B2F6	B2F8	X	B2FA	B2FC	B2FE	X E
CLK	BO							
🗄 Sum	H 00004	000	00		00004	χ 00005	20005	X000 X8X082
Cout	HO	<u> </u>	Tpd					

Appendix C(x): The timing simulation mode of modified of three levels six operands 16-bits CSA with RCA design



NTE3078 & NTE3079 0.56" Single Digit Numeric Display Seven Segment, RHDP

Description:

The NTE3078 (Common Anode) and NTE3079 (Common Cathode) are 0.56 inch (14.2mm) height single digit displays utilizing LED chips which are made from GaAsP on a GaAs substrate.

Features:

- 0.56 Inch (14.2mm) Digit Height
- Low Power Requirement
- Excellent Characters Appearance
- Catagorized for Luminous Intensity
- IC Compatible
- Easy Mounting on PC Board or Socket

<u>Absolute Maximum Ratings:</u> ($T_A = +25^{\circ}C$ unless otherwise specified)

Power Dissipation (Per Segment), P _T	۱W
Peak Forward Current (Per Segment, 1/10 Duty Cycle, 0.1ms Pulse Width), I _F peak 160n	nA
Continuous Forward Current (Per Segment), I _F	nA ′°C
Reverse Voltage (Per Segment), V _R	5V
Operating Temperature Range, Topr –25° to +85	°C
Storage Temperature Range, T _{stg} –25° to +85	°C
Lead Temperatue (During Solder, 1/16" Below Seating Plane, 3sec max), T _L	°C

<u>Electrical/Optical Characteristics</u>: ($T_A = +25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Average Luminous Intensity	l _v	I _F = 10mA	200	500	_	μcd
Peak Emission Wavelength	λ _P	I _F = 20mA	-	655	_	nm
Spectral Line Half–Width	Δ_{λ}	I _F = 20mA	_	24	_	nm
Forward Voltage, Any Segment or D.P.	V _F	I _F = 20mA	_	1.7	2.0	V
Reverse Current, Any Segment or D.P.	I _R	$V_R = 5V$	-	-	100	μΑ
Luminous Intensity Matching Ratio	I _{v-m}	I _F = 20mA	_	_	2:1	

