CHAPTER 1

INTRODUCTION

1.1 Scope

This project consists of several phases; literature review, experimental setup which includes hardware and software setup, experimental and testing and lastly report documentation. Each phase took a certain period of time to be completed. In the early time, literature review has been done to gather useful information. A lot of study needs to be carried out in order to get better understanding and exposure regarding ways to connect Quartes II with Altera Education Kits (UP2 Board) by using Verilog HDL programming language. Follow on that is experimental setup, both hardware and software installations have to be done correctly. After installation, a thorough testing have to be done to assure that both hardware and software are well functioning. Later on, a simple test is conducted to assure the output is tally to the input. Project is started after the calibration is done. Lastly, a report will be written on to present the project.

1.2 Motivation

FPGAs are programmable digital logic chips which can be programmed to do almost any digital function. FPGAs are "fine-grain" devices. That means that they contain a lot (up to 100000) of tiny blocks of logic with flip-flops. FPGAs have special routing

resources to implement efficiently binary counters and arithmetic functions (adders, comparators) and RAM.

FPGAs can contain very large digital designs. The designs can run much faster than design a board with discrete components, since everything runs within the FPGA, on its silicon die. FPGA can be downloaded many times with different functionalities. If a mistake is made in design, just fix the "logic function", re-compile and re-download it. No PCB, solder or component to change.

In this project, FPGA is programmed to perform like a music box in which it contains several sounds and music. A study of the internal function of the FPGA chip is carried out through the experiments.

In order to make the FPGA chip function like music box, a program is written out in Verilog HDL language and downloaded into the FPGA chip. Sounds and music will be written in Verilog HDL language as well.

Furthermore, since theoretical knowledge is learned during lecture times, there is an opportunity to gain more hands-on experiment if the theory learned can be successfully be produced in an application.

1.3 Objectives

The objectives of this project are listed as follow:

- ✓ To design and implement a music box using FPGA. As FPGA is a digital logic chip that can be programmed to do almost any digital function. An effort is carried out to design and make it to perform like a music box.

- ✓ To enhance Verilog HDL programming skills. Since the Verilog HDL programming language is used to program the FPGA to perform like a music box. Programming skill will be sharpened indirectly through this project.

- ✓ To apply theoretical knowledge to produce an application. Theoretical theory may not be the same as the practical; therefore experiment was carried out to study an application.

1.4 Report Outline

This report is comprised of several chapters which devoted to the construction of music box. In this project, we are interested to use FPGA for this purpose. A simple overview of the project, including the scope, motivation and objectives are discussed.

Literature review is discussed in Chapter 2. Detail knowledge of FPGA is presented. Some basic information of UP2 Education Kit is discussed. Besides that, the Verilog HDL and Quartus II software that used in the project will be introduced too.

Chapter 3 presents the experimental setup used in the project. This consists of hardware and software setup. The chapter will described about calibration on both hardware and software setup. This process is carried out to assure the functionality of respective equipment.

Experiment results are devoted in Chapter 4. The results of program for different type of sounds will be tested and evaluated.

Lastly, Chapter 5 will conclude this report with findings, conclusions and recommendation of future work. Commercialization will be discussed in this chapter too.