APPLICATION OF DECOUPLING NETWORKS IN DEADBEAT CONTROLLER FOR HIGH-FREQUENCY LINK INVERTER

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ABSTRACT

Deadbeat is a control method that results in very fast dynamic response. However its application in power electronics converters is somewhat hindered because it is very sensitive towards parameter variations. In an attempt to improve this shortcoming, a modified Deadbeat controller with additional disturbance decoupling networks is introduced. The proposed controller consists of inner current loop, outer voltage loop and a feedforward controller. This scheme is applied to a high-frequency link inverter. A 1kVA prototype inverter is constructed and the performances of the proposed controller are experimentally verified, along with MATLAB-Simulink simulation. The results show that the proposed controller with decoupling networks has very fast dynamic response, and good steady-state response even under severe nonlinear loads.

Keywords: *Bidirectional, Deadbeat Control, HF Transformer, Inverter, Pulse Width Modulation*

1 INTRODUCTION

Closed-loop controller of a power ac to dc converter (inverter) serves two main purposes. Firstly, to synthesise a sinusoidal steady-state output voltage waveform under all loading conditions. Secondly, to ensure high disturbance rejection capability, where the inverter output voltage will return to the desired operating state in shortest time after a disturbance, such as sudden load change during start-up and lost of load.

Proportional-Integral-Derivative (PID) control is the most common controller for industrial inverters [1]. Its popularity is partly due to its simple structure that can be easily implemented in both analogue and digital. However, the conventional PID controller requires much effort in the tuning of controller gains before a dynamically acceptable response is obtained. The tuning is usuallly achieved using "trial and error" method. Generally, the performance of PID controller is somewhat inferior to other control methods.

Hysteresis control [2],[3] is a simple pulse width modulated control method that determines an inverter output voltage instantaneously. It is essentially an analogue control technique. In a two-loop control system (current loop and voltage loop), the basic idea is to control the load current in order to regulate the output voltage. The error between the reference signal and the load current is locked within a fixed hysteresis band using a simple rule. If the error exceeds the upper hysteresis band, the inverter output voltage is switched low; if the error falls below the lower hysteresis band, the inverter output voltage is switched high. Although simple and fast, the control results in large current ripple and variable switching frequency. The latter poses difficulty in designing the low-pass filter and causes excessive stress on the power switches.

Sliding mode control [4],[5] utilises a high speed switching control law to drive the state trajectory of the plant onto a specified surface in the state space, called sliding surface. Thereafter it needs to keep the state trajectory on this surface for all subsequent time. When sliding on the sliding surface, the structure of the system is changed discontinuously according to the instantaneous values of the system states evaluated along the trajectory. Due to the discontinuous change of the system structure, the system is insensitive to parameter variations and external disturbances [6]. The problem with sliding mode control, however, is the difficulty to locate a suitable sliding surface. Moreover it suffers from a phenomenon known as "chattering". In practice, chattering may be caused by the parasitic dynamics of sensors or other feedback components, which are often neglected during the control design process.

The more recent control methods are the fuzzy logic and neural network [7],[8]. They are classified as nonlinear and adaptive control, with robust performance under parameter variations and load disturbances. These features made them suitable for closed-loop control of inverter. As the detailed dynamics of the plant is not needed in the design process, fuzzy logic control possesses inherent robust property [9]. However, it lacks systematic procedures for designing the fuzzy control rules and choosing the membership functions. It depends entirely on practical experiences of the designer.

Artificial neural networks are interconnections of neurons that tend to emulate the human brain [10]. The architectures are generally distributed and constructed from many nonlinear computational nodes operating in parallel. There are weighting elements between the nodes that define the strength of connection between nodes, which are adapted during learning by some optimisation procedure to yield the appropriate input-output map. The performance of neural network nonlinearity depends on the total allowed errors. A smaller error results in better performance. Since neural network has fault tolerance, it provides a robust performance for the system. The main disadvantages of neural network is the requirement for extensive training process that can be very time-consuming.

Deadbeat control is recognised to be one of the most attractive control techniques for power inverters [11]. It is a fully digital method. This control technique places all the

system closed-loop poles at the origin of the z-plane. Hence, it can achieve fast dynamic response with low Total Harmonic Distortion [12]. Although Deadbeat control has a potential to provide fast response, it is also known to be very sensitive towards parameter variations [13]. This is one of the main reasons why it is not widely used in industrial applications.

In this paper, we propose to improve the Deadbeat performance by introducing a correction scheme known as the disturbance decoupling networks. Although the use of such decoupling network is not new [14], its application to regulate the output voltage of a high frequency link inverter appears to be absent in literature. Furthermore, the disturbance decoupling networks are introduced by taking into account the model discretisation effect. As such, the system has good disturbance rejection capability. This makes the system capable of handling critical loads such as rectifier load and triac load.

The paper is organised in the following manner. First, an overview to the plant to be controlled, i.e. the high frequency link inverter is presented. This will be followed by modelling of the plant using state space equations. To the benefit of the readers who are not familiar with Deadbeat method, a brief discussions on its fundamental theory, capability nd limitation is outlined. Then the Deadbeat controller design with decoupling network will be presented. To prove the concept, a 1kVA high frequency link inverter prototype is constructed and the control scheme is applied. Typical results are discussed.

2 PLANT MODELLING

The high frequency link inverter, which is the plant to be controlled, is shown in Figure 1. The topology was first proposed in [15]. The main conversion circuits are the high-frequency PWM bridge, active rectifier and polarity-reversing bridge. The dc voltage, V_{dc} is converted into high-frequency PWM voltage, v_{HF} using the high-frequency PWM bridge. Then, the voltage is isolated and stepped-up using the high-frequency transformer. Next, the voltage is rectified using the active rectifier. The rectified PWM voltage, v_{pwm_rect} is then low-pass filtered, v_{rect} and unfolded to obtain the sinusoidal output voltage, v_o. The key waveforms at the principal conversion stages are shown in Figure 2.

To design a closed-loop controller for the high frequency link inverter, the plant is first modelled using the state-space technique. Referring to Figure 1, it is assumed that V_{dc} is constant. The inverter switching frequency is considered to be high enough compared to the 50Hz modulating frequency. The high-frequency transformer is assumed to be operating in its linear area. As such, the high-frequency PWM bridge and the

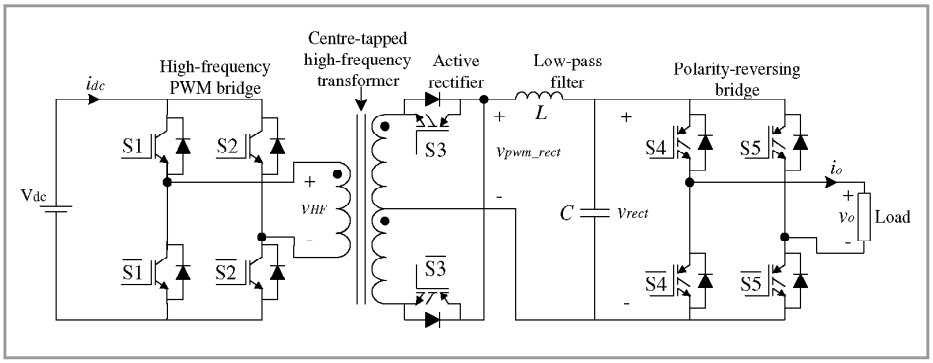


Figure 1: Bidirectional High-Frequency Link inverter

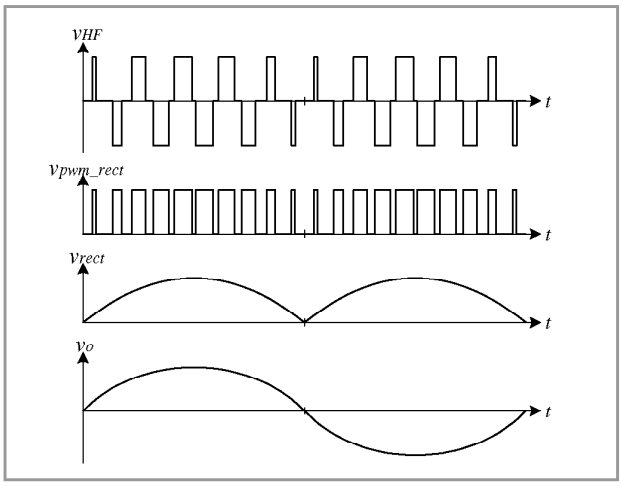


Figure 2: Key waveforms at the principal conversion stages

transformer can be modelled as constant gains. The polarity-reversing bridge is only operated at line-frequency (50Hz), thus its dynamic can be ignored. With these assumptions, the dynamics of the system can be simplified to a *LC* low-pass filter connected to the load. Choosing the filter inductor current, i_L and filter capacitor voltage, v_{rect} as the state variables, the discrete-time state-space equations of the system can be written as:

$$x(k+1) = Ax(k) + Bu(k) + B_d i_{or}(k) \quad (1)$$

$$v_{or}(k) = Cx(k) \quad (2)$$

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} = \begin{bmatrix} \cos(\omega T_s) & -\frac{1}{\omega L}\sin(\omega T_s) \\ \frac{1}{\omega C}\sin(\omega T_s) & \cos(\omega T_s) \end{bmatrix} \quad (3)$$

$$B = \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{\omega L}\sin(\omega T_s) \\ 1-\cos(\omega T_s) \end{bmatrix} \quad (4)$$

$$B_d = \begin{bmatrix} B_{d1} \\ B_{d2} \end{bmatrix} = \begin{bmatrix} 1-\cos(\omega T_s) \\ -\frac{1}{\omega C}\sin(\omega T_s) \end{bmatrix} \quad (5)$$

$$C = [0\ 1] \quad (6)$$

$x(k) = \begin{bmatrix} i_L(k) \\ v_{rect}(k) \end{bmatrix}$ is the state vector,

$\omega = \frac{1}{\sqrt{LC}}$ is the cut-off frequency of the low-pass filter in radian per second, and T_s is the sampling period. Based on the discrete-time equations, the digital model of the system can be represented by the block diagram in Figure 3, where z^{-1} denotes a unit delay.

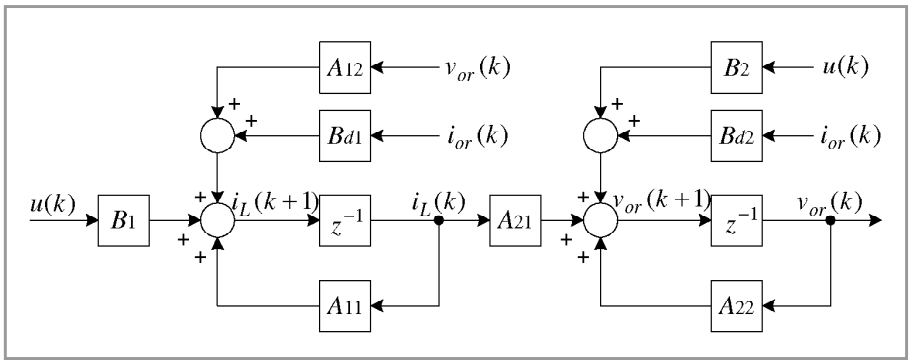


Figure 3: Discrete-time model of the high frequency link inverter

function of the plant, which could include a zero-order hold. The closed-loop transfer function is written as:

$$\frac{Y(z)}{R(z)} = M(z) = \frac{D(z)G(z)}{1+D(z)G(z)} \qquad (9)$$

Solving for D(z) from equation (9) yields:

$$D(z) = \frac{1}{G(z)}\left[\frac{M(z)}{1-M(z)}\right] \qquad (10)$$

3 CONTROLLER DESIGN

3.1 Principle of Deadbeat Control

Deadbeat control exhibits very fast dynamic response for discrete-time control. In Deadbeat control, any nonzero error vector will be driven to zero in at most *n* sampling periods if the magnitude of the scalar control *u(k)* is unbounded, where *n* is the order of the closed-loop system.

In analogue control system, if the closed-loop poles of the system can be moved further towards the left half of the *s*-plane, it can achieve faster dynamic response. Ideally, the poles are to be placed at minus infinity (- ∞). This is usually not realisable as it is impossible to place all the poles at $s = -\infty$. However, this can be realised in digital control system. Through the mapping between *s*-plane and *z*-plane, as shown in Figure 4, the pole at $s = -\infty$ in the *s*-plane is mapped to $z = 0$ in the *z*-plane. The complex variables *s* and *z* are related by:

$$z = e^{sT} \qquad (7)$$

where *T* is the sampling period.

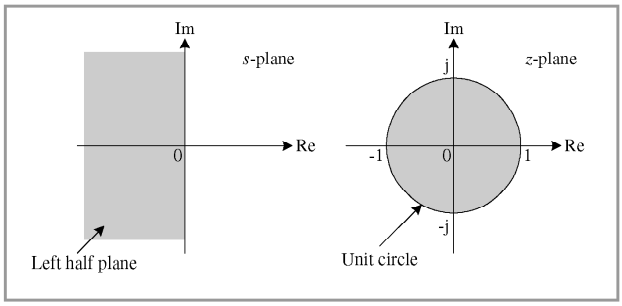


Figure 4: The mapping of s-plane and z-plane

Therefore, if all the closed-loop poles of the digital control system can be located at the origin of the *z*-plane, the fastest dynamic response can be achieved. As such, the discrete-time characteristic equation can be expressed as:

$$z^n = 0 \qquad (8)$$

where *n* is the order of the closed-loop system. This is the so-called Deadbeat control, where the state variables of the system can follow the reference variables without error after the intervals of *n* sampling periods.

Consider a discrete-time control system in Figure 5, where *D(z)* is the Deadbeat controller, and *G(z)* is the transfer

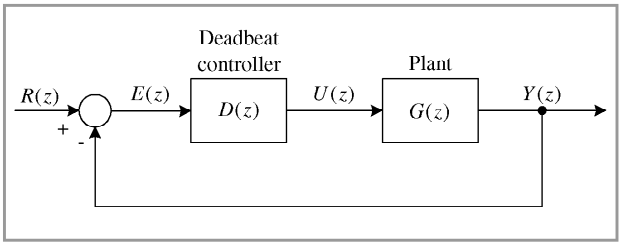


Figure 5: A typical Deadbeat control system

Note that the transfer function of the controller contains the inverse of the uncompensated system's open-loop transfer function, *G(z)*. Hence, the design of Deadbeat controller is to cancel out the poles and zeros of the uncompensated system, replacing it with a polynomial based on *M(z)* so that the desired closed-loop response can be achieved. The general equation of *M(z)* is given as:

$$M(z) = 1-(1-z^{-1})^n F(z) \qquad (11)$$

where *F(z)* is a polynomial of z^{-1}. In practice, the ideal Deadbeat response is hard to be realised, as there might be some uncertainties in the system model. Therefore, the interest is to implement the controller as close to Deadbeat response as possible.

A stability analysis is performed to investigate the robustness of the designed controller against parameter mismatches. As the controller gains are determined based on the cut-off frequency of the low-pass filter, $\omega = \frac{1}{\sqrt{LC}}$, parameter variations of filter inductor and capacitor will degrade the performance of the designed controller. This is due to the shifting of closed-loop poles from the desired value (origin of *z*-plane), thus Deadbeat response is no longer obtained.

Figure 6 depicts the trajectories of the closed-loop pole if the inductor value is increased from 0% to 90%, and decreased from 0% to -50%. As the structure of the outer voltage loop is same as the inner current loop, the trajectories with change of capacitor value are quite similar to that with change of inductor value. Referring to Figure 6, when the value of *L* is changed (maintaining values of other parameters), the pole cancellation is not achieved, thus Deadbeat response is not attained. However, the poles are within the unit circle, so the system is still stable. It is noted that the system is more stable to positive variations, with a reasonably small shifting of pole from the origin of *z*-plane.

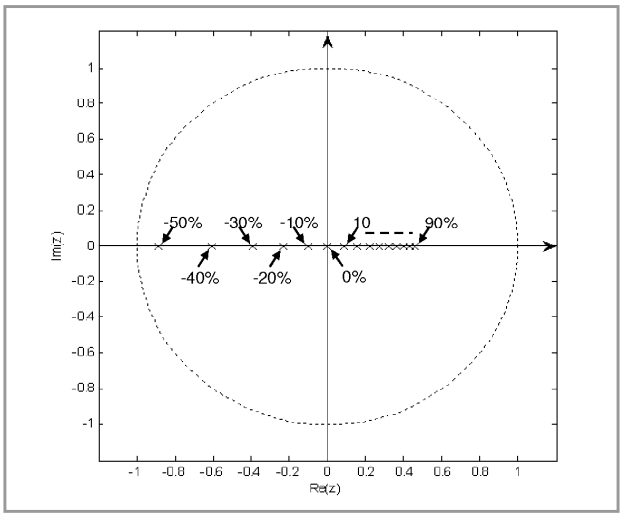


Figure 6: Trajectories of the closed-loop pole with L change

In general, it is pointed out that Deadbeat controller is sensitive to parameter variations [16]. However, the designed controller with inclusion of decoupling networks improves the robustness of the system. Although the dynamic response of the inverter will be degraded due to large parameter mismatches, the system is still stable within acceptable range.

3.2 Deadbeat Control with Decoupling Network

The block diagram proposed Deadbeat controller is illustrated in Figure 7. It consists of inner current loop, outer voltage loop, and a feedforward controller. From the discrete-time model of the plant in Figure 3, it can be seen that there are disturbances terms acting on the inductor current and output voltage. These disturbances are compensated using additional decoupling networks in the following equations:

$$i_d(k) = -\frac{A_{12}}{B_1} v_{or}(k) - \frac{B_{d1}}{B_1} i_{or}(k) \tag{12}$$

$$v_d(k) = -\frac{B_2}{A_{21}} u(k) - \frac{B_{d2}}{A_{21}} i_{or}(k) \tag{13}$$

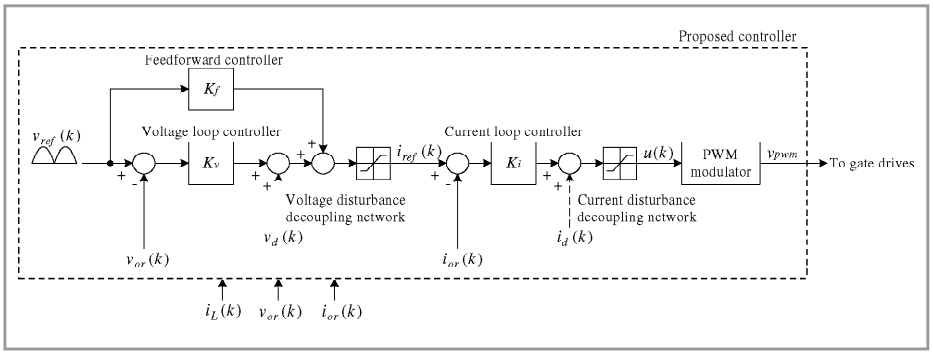


Figure 7: Proposed Deadbeat controller for the high frequency link inverter

3.2.1 Current Loop

Figure 8(a) shows the inner current loop controller. The current disturbance decoupling network is added to compensate the disturbances acting on the inductor current. Cancelling the current disturbance coupling allows a simple gain, K_i to be applied in forming the inner current loop. From Figure 8(a), the current loop control law can be derived:

$$u(k) = k_i [i_{ref}(k) - i_L(k)] + i_d(k) \tag{14}$$

where $u(k)$ is the control signal applied to the PWM modulator, $i_{ref}(k)$ is the inductor current reference generated by the outer voltage loop, and $i_d(k)$ is the current disturbance decoupling network from Equation (12).

Figure 8(b) shows the simplified current loop. The discrete-time closed-loop transfer function of the current loop is:

$$C_i(z) = \frac{i_L(k)}{i_{ref}(k)} = \frac{K_i B_1 z^{-1}}{[K_i B_1 - A_{11}] z^{-1} + 1}$$
$$= \frac{K_i \sin(\omega T_s) z^{-1}}{[K_i \sin(\omega T_s) - \omega L \cos(\omega T_s)] z^{-1} + \omega L} \tag{15}$$

From Equation (15), the characteristic equation of the closed-loop current controller can be written as:

$$z - [A_{11} - K_i B_1] = 0$$
$$z - \left[\cos(\omega T_s) - K_i \frac{1}{\omega L} \sin(\omega T_s)\right] = 0 \tag{16}$$

To achieve Deadbeat response, the current loop gain, K_i is designed as:

$$K_i = \frac{A_{11}}{B_1} = \frac{\omega L \cos(\omega T_s)}{\sin(\omega T_s)} \tag{17}$$

Substituting Equation (17) into Equation (15) yields:

$$i_L(k) = A_{11} z^{-1} i_{ref}(k) = \cos(\omega T_s) z^{-1} i_{ref}(k) \tag{18}$$

When ωT_s is sufficiently small, $\sin(\omega T_s) \approx \omega T_s$ and $\cos(\omega T_s) \approx 1$. Hence, Equation (18) can be written as $i_L(k) = z^{-1} i_{ref}(k)$, which is the Deadbeat response.

3.2.2 Voltage Loop

Figure 9(a) shows the outer voltage loop controller. The voltage disturbance decoupling network is added to compensate the disturbances acting on the output voltage. This will improve the robustness of the system towards load variations. Besides, it also acts as additional current loop command to produce the needed load current without waiting for errors in voltage to occur.

The design of the voltage loop controller is similar to the current loop controller. The voltage loop gain, K_v is applied to achieve Deadbeat response. Referring to Figure 9(a), the voltage loop control law is derived:

$i_{ref}(k) = K_v [v_{ref}(k) - v_{or}(k)] + v_d(k)$

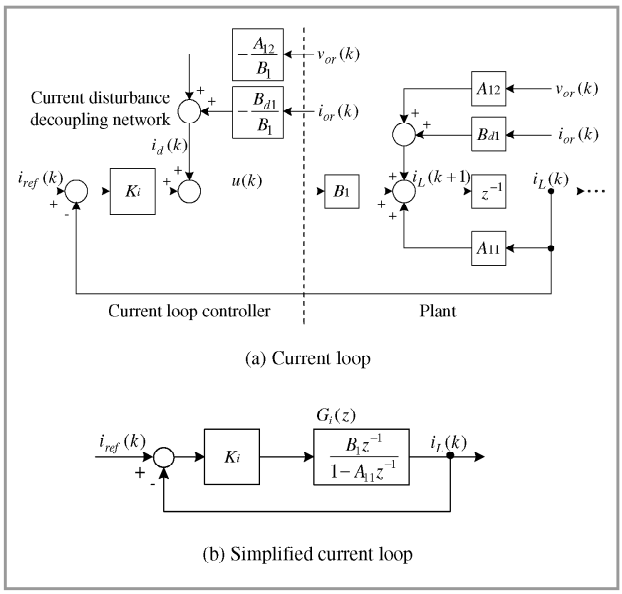


Figure 8: Current loop controller

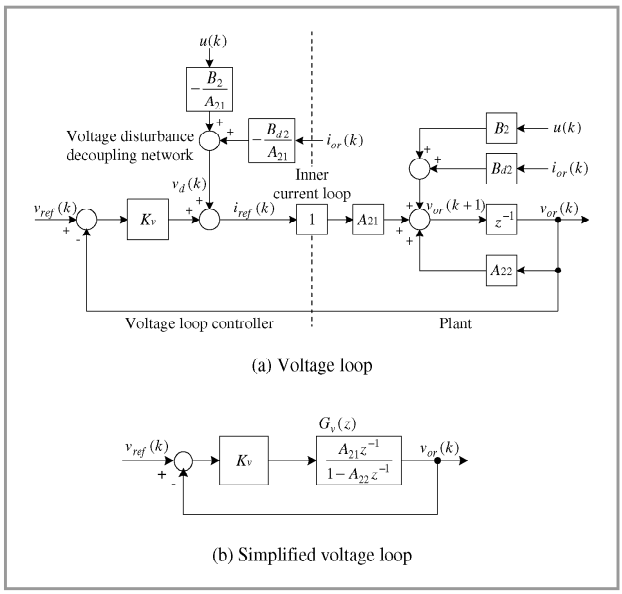


Figure 9: Voltage loop controller

where i_{ref} is the generated current loop command for the inner current loop, $v_{ref}(k)$ is the rectified sinusoidal voltage reference, and is the voltage disturbance decoupling network from Equation (13).

Figure 9(b) shows the simplified voltage loop. It can be noted that the inner current loop is viewed as a constant gain, with the condition of current loop is well designed. The discrete-time closed-loop transfer function of the voltage loop is:

$$C_v(z) = \frac{v_{or}(k)}{v_{ref}(k)} = \frac{K_v A_{21} z^{-1}}{[K_v A_{21} - A_{22}]z^{-1} + 1}$$

$$= \frac{K_v \sin(\omega T_s) z^{-1}}{[K_v \sin(\omega T_s) - \omega C \cos(\omega T_s)]z^{-1} + \omega C} \quad (20)$$

From Equation (20), the characteristic equation of the closed-loop voltage controller can be written as:

$$z - [A_{22} - K_v A_{21}] = 0$$

$$z - \left[\cos(\omega T_s) - K_v \frac{1}{\omega C}\sin(\omega T_s)\right] = 0 \quad (21)$$

Similar to current loop, the voltage loop gain, *Kv* is designed to achieve Deadbeat response:

$$K_v = \frac{A_{22}}{A_{21}} = \frac{\omega C \cos(\omega T_s)}{\sin(\omega T_s)} \quad (22)$$

Substituting Equations (22) into Equation (20) yields:

$$v_{or}(k) = A_{22} z^{-1} v_{ref}(k) = cps\ (\omega T_s) z^{-1} v_{ref}(k) \quad (23)$$

When ωT_s is sufficiently small, Equation (23) can be written as $v_{or}(k) = z^{-1} v_{ref}(k)$, which is the Deadbeat response.

3.2.3 Feedforward Controller

From Equation (23), it can be seen that there is a steady-state error in the output voltage if the value of ωT_s is not sufficiently small. To compensate the steady-state error, a feedforward controller is added to the output of the voltage loop controller. The feedforward controller imposes a gain scheduling effect on the voltage loop controller according to the reference signal. Figure 10 shows the voltage loop with inclusion of feedforward controller.

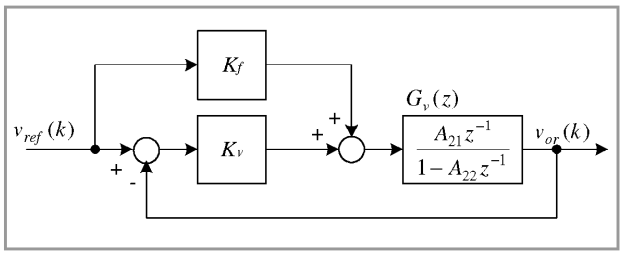


Figure 10: Voltage loop with feedforward controller

Referring to Figure 6, the discrete-time closed-loop transfer function is derived:

$$\frac{v_{or}(k)}{v_{ref}(k)} = \frac{[K_v + K_f]A_{21} z^{-1}}{[K_v A_{21} - A_{22}]z^{-1} + 1}$$

$$= \frac{[K_v + K_f]\sin(\omega T_s) z^{-1}}{[K_v \sin(\omega T_s) - \omega C \cos(\omega T_s)]z^{-1} + \omega C} \quad (24)$$

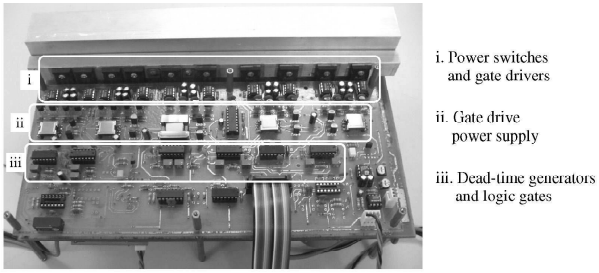
The feedforward gain, Kf is designed as:

$$K_f = \frac{1 - A_{22}}{A_{21}} = \frac{\omega C[1 - \cos(\omega T_s)]}{\sin(\omega T_s)} \quad (25)$$

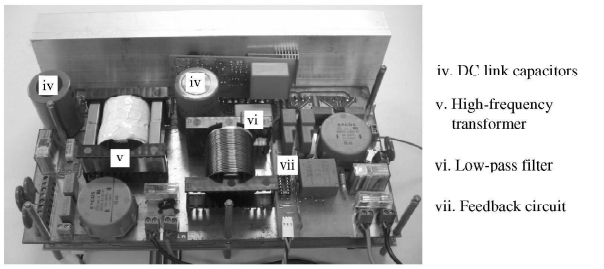
Substituting Equations (22) and (25) into Equation (24), $v_{or}(k) = z v_{ref}(k)$ is obtained, which ensures the Deadbeat response

4 EXPERIMENTAL SET-UP, RESULTS AND DISCUSSION

To prove the workability of the proposed Deadbeat control, a "prove-of concept" 1kVA prototype high frequency link inverter has been constructed. The controller is implemented using the DS1104 Digital Signal Processor from dSPACE. The computation engine is the 64-bit floating-point processor with TMS320F240 Slave DSP. Hall-effect current sensors, HY10-P and voltage sensor, LV25-P are used to sense the feedback signals. The signal conditioning such as noise filtering and signal amplification are performed in software using the DS1104 DSP. As a verification to the practical results, a MATLAB-Simulink simulation is also carried out. Figure 11 shows the photograph of the prototype inverter.



(a)



(b)

Figure 11: Photograph of high frequency link inverter (a) top view – gate drive module (b) bottom view – power circuit module

Table 1 provides the parameters of the prototype inverter. The parameters of the proposed Deadbeat controller are shown in Table 2. The current loop gain (K_i), voltage loop gain (K_v) and feedforward gain (K_f) are designed as described in the previous section.

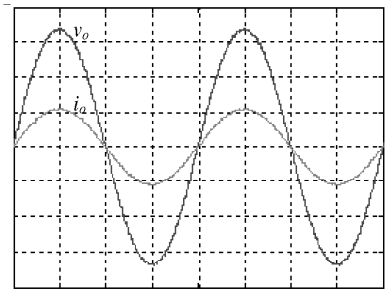
Table 1: Parameters of high frequency link inverter

Parameter	Value
Switching frequency	f_{sw} = 25kHz
Nominal input voltage	V_{dc} = 150V
Rated output voltage	v_o = 240V_{rms}
Rated output frequency	f = 50Hz
Rated output power	P_o = 1kVA
Rated output current	i_o = 4.2A_{rms}
Filter inductor	L = 0.66mH
Filter capacitor	C = 6.8μF
Nominal resistive load	R = 62.5Ω
Inductive load (power factor, pf = 0.7)	R_i = 62.5Ω L_i = 183mH
Nonlinear load (full-bridge rectifier load)	R_d = 500Ω C_d = 470μF

Table 2: Parameters of proposed Deadbeat controller

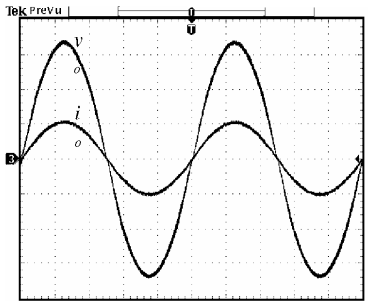
Parameter	Value
Sampling period	T_s = 40μs
Current loop gain	K_i = 14.4910
Voltage loop gain	K_v = 0.1493
Feedforward gain	K_f = 0.0330

Figure 12 shows the Matlab simulation and experimental results of the proposed Deadbeat controller under resistive load. The results are shown side-by side for clarity. The output voltage THD obtained is 1.5%.



Vertical scale: output voltage 100V/div,
output current 5A/div,
Time scale: 5ms/div

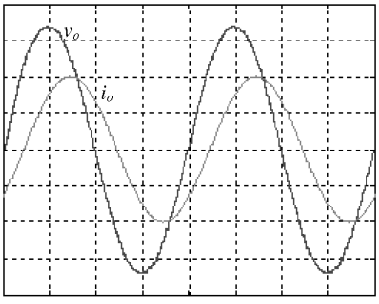
(a)



Vertical scale: output voltage 100V/div,
output current 5A/div,
Time scale: 4ms/div

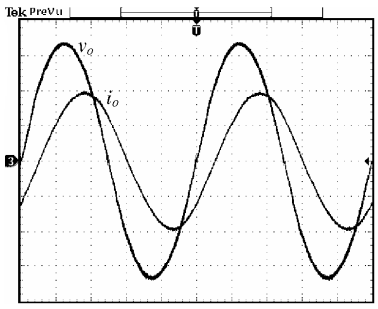
(b)

Figure 12: output waveforms under resistive load (a) simulation (b) experimental



Vertical scale: output voltage 100V/div,
output current 2A/div,
Time scale: 5ms/div

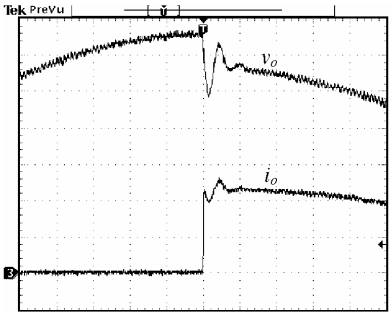
(a)



Vertical scale: output voltage 100V/div,
output current 2A/div,
Time scale: 4ms/div

(b)

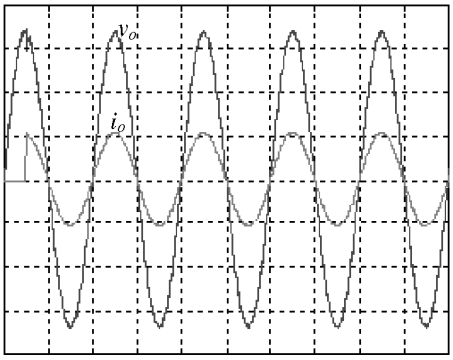
Figure 13: Output waveforms under inductive load (a) simulation (b) experimental



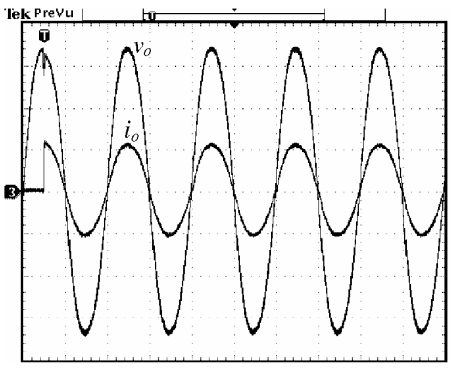
Vertical scale: output voltage 50V/div, output current 2A/div

Time scale: 0.4ms/div

Figure 15: Vertical scale: output voltage 50V/div, output current 2A/div Time scale: 0.4ms/div



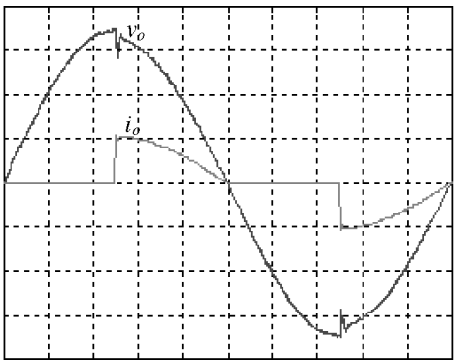
(a)



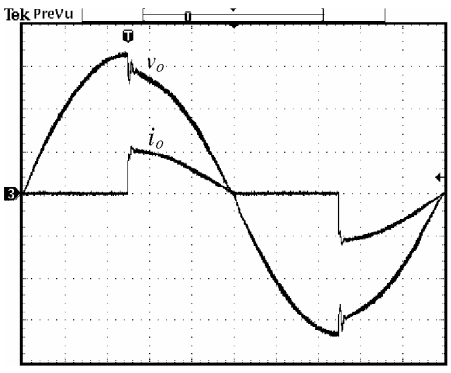
(b)

Vertical scale: output voltage 100V/div, output current 5A/div
Time scale: 10ms/div

Figure 14: Output waveforms under step load change (a) simulation (b) experimental



(a)



(b)

Vertical scale: output voltage 100V/div, output current 5A/div;
Time scale: 2ms/div

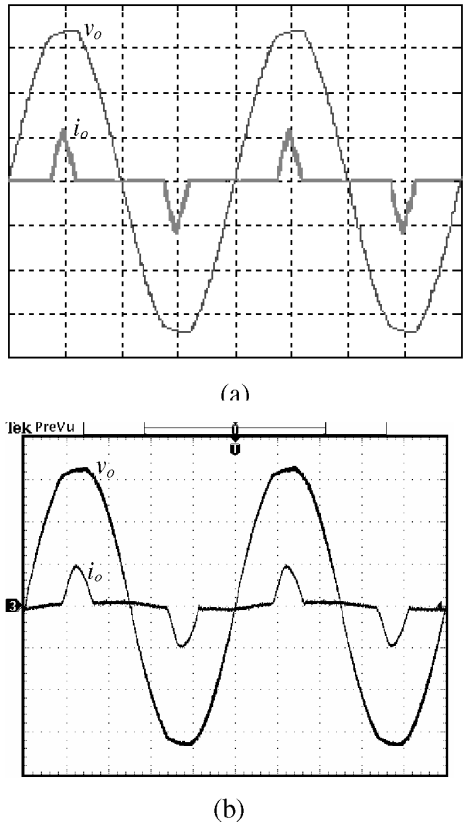
Figure 16: Output waveforms under triac load (a) simulation (b) experimental

Figure 13 shows the simulation and experimental results under inductive load. From the waveform it is clear that the system is capable of carrying bidirectional power flow. The output voltage THD obtained is 2.2%.

Figure 14 shows the output waveforms under a step resistive load change. As can be seen, the simulation and experimental results are in close agreement. The voltage droop caused by the sudden load change can be recovered very quickly. The zoom in view of the output waveforms is shown in Figure 15 It shows that the voltage transient can be reduced to 10% in about 0.32ms.

Figure 16 shows output waveforms of the system under triac load commutated at 90o/270o. It can be seen that the proposed Deadbeat controller exhibits fast dynamic response, and capable of handling cyclic load variations.

To test a worst case loading, the system is connected to a full-bridge rectifier, with a capacitor filter, Cd and resistive load, Rd



Vertical scale: output voltage 100V/div, output current 5A/div;
Time scale: 4ms/div

Figure 17: Output waveforms under rectifier load(a) simulation (b) experimental

of 470mF and 500W respectively. This type of load can be considered to be the most severe type. It causes the intense voltage distortion due to the highly distorted current. Figure 17 shows the steady-state output waveforms under full-bridge rectifier load. As can be seen, the output voltage waveform has good quality without much distortion. This can be attributed to the improved robustness of the system. A low voltage THD of 3.8% is obtained for this system.

CONCLUSION

A Deadbeat controller with disturbance decoupling network for the high frequency link inverter has been proposed. To verify the feasibility of the proposed controller, a 1kVA prototype inverter has been constructed. The experimental results show that the proposed controller exhibits very fast dynamic response towards step load changes. Besides, a sinusoidal voltage waveform with low distortion can be maintained even under highly nonlinear loads. Thus, the robustness of the system towards load variations is improved.

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PROFILES

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