# CHAPTER 4

## RESULTS AND DISCUSSION

The previous chapter has discussed the design development of two stages CMOS operational amplifier. In this chapter, the results are organized as follows:

- Transistor bias summary using test bench circuit.
- The operational amplifier parameters verification.
- The layout of two stage CMOS operational amplifier.
- The DRC (design rules check) and LVS (layout versus schematic) simulation.

After the design has been developed using the procedures as stated in methodology, the next step was to simulate the circuit using more accurate models of the transistor. Figure 4.1 below shows the testbench circuit for the designed CMOS operational amplifier circuit. Testbench circuit is a test circuit for simulation. The testbench circuit below shows the inverting terminal connected to ground and the non-inverting terminal is supplied with zero DC input.

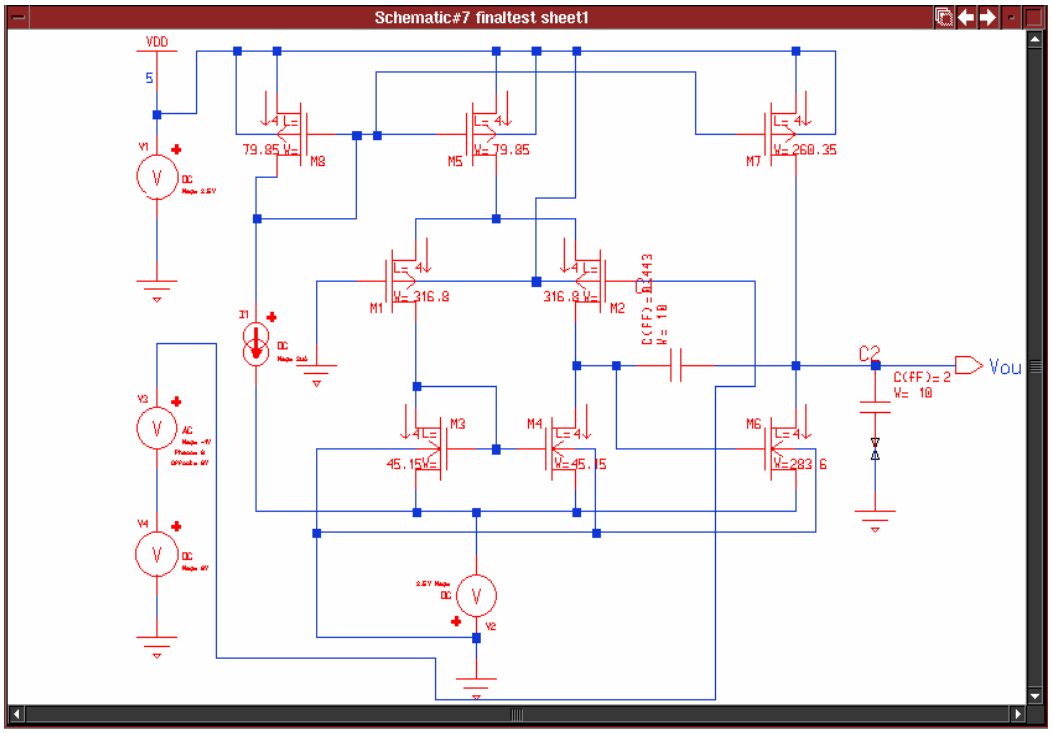


**Figure 4.1:** The testbench circuit for CMOS operational amplifier.

The transistor's width and length was set according to the calculated values. The VDD is 2.5V and VSS is -2.5V. The bias current Ibias is 8µA. The bias current for every transistor's is obtained through DC analysis in Mentor Graphics.

## 4.1 Transistor bias currents simulation.

The DC analysis is done to determine the drain currents of every transistor. Figure 4.2 and Figure 4.3 is the simulation result obtained using the design architecture station employing 0.35um technology in Mentor Graphics. The Xelga simulation viewer is selected for better view. The drain current's of transistor from M1 to M8 is shown in Y tab below.

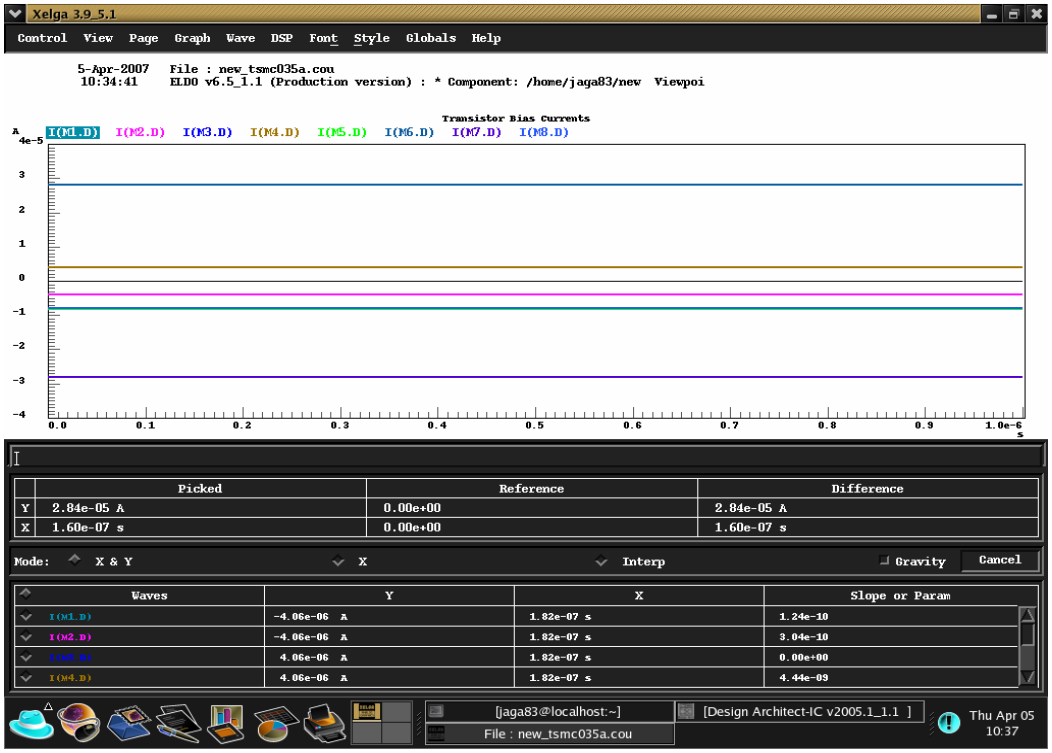


**Figure 4.2:** Output waveform of current I1-I4 from the simulation.

The drain current's of transistor from M to M8 is shown in Y tab below.

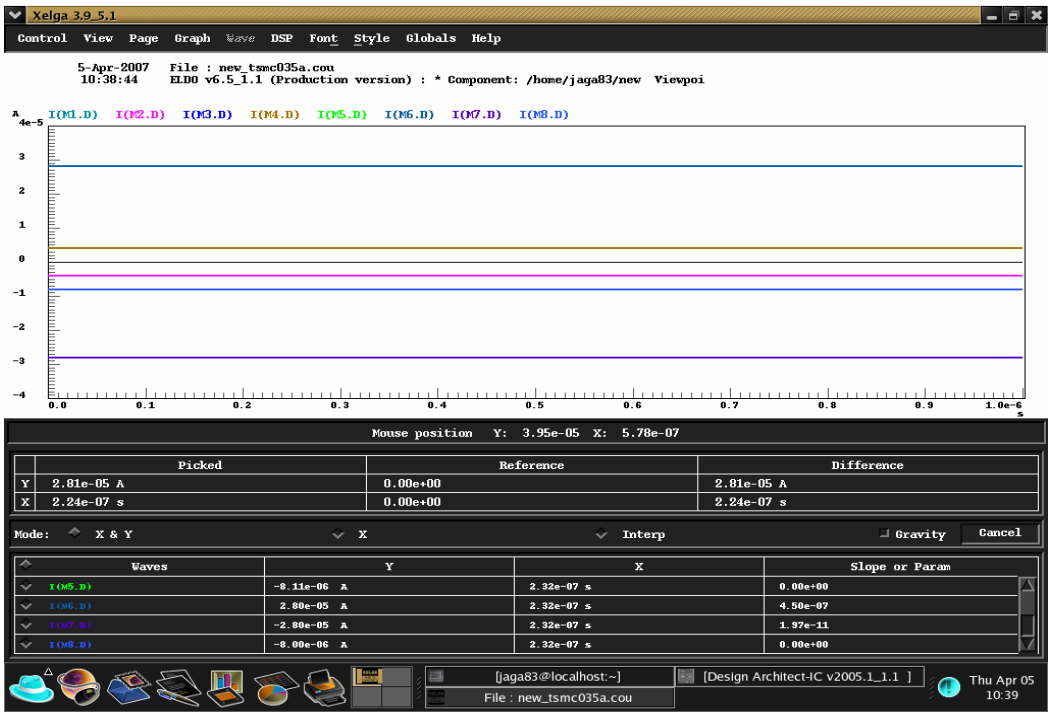


**Figure 4.3:** Output waveform of current I5-I8 from the simulation.

## 4.2 Transistor Bias Summary

**Table 2.0 :** Transistor bias summary.

| Transistor | W/L (um/um) | ID (uA) | VGS (mV) | gm (uA/V) | gds (nA/V) |
|---|---|---|---|---|---|
| M1 | 316.8/4 | 4.06 | 728.637 | 210.163 | 477.05 |
| M2 | 316.8/4 | 4.06 | 728.637 | 210.163 | 477.05 |
| M3 | 45.15/4 | 4.06 | 751.597 | 131.824 | 633.202 |
| M4 | 45.15/4 | 4.06 | 751.597 | 131.824 | 633.202 |
| M5 | 79.85/4 | 8.11 | 798.768 | 149.124 | 940.000 |
| M6 | 283.6/4 | 28.00 | 754.543 | 867.633 | 4387.600 |
| M7 | 260.4/4 | 28.00 | 801.926 | 500.332 | 3290.000 |
| M8 | 79.85/4 | 8.00 | 798.028 | 148.109 | 940.000 |

Table 2.0 above is the transistor bias summary of transistors M1 to M8. Whereby the equation for above parameters are as below:

For pmos,

$$I_D = \frac{1}{2} Kp \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{4.0}$$

For nmos,

$$I_D = \frac{1}{2} Kn \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{4.1}$$

$$gm = \sqrt{2 \times K \times I_D \times \frac{W}{L}} \tag{4.2}$$

$$gds = \lambda \times I_D \tag{4.3}$$

## 4.3 Parameter Verification

Figure 4.4 shows the offset voltage (Vos) of the amplifier. The ideal op-amp produces zero volts out for zero volts in. In practical op-amp, however, a small dc voltage, Vout(error), appears at the output when no differential input voltage is applied. The input offset voltage, Vos, is the differential dc voltage required between the inputs to force the output to zero volts. While Vos need not make Vout exactly zero, it should keep the output in the linear range so that when simulator calculates the bias point for small signal analysis, reasonable results are obtained..

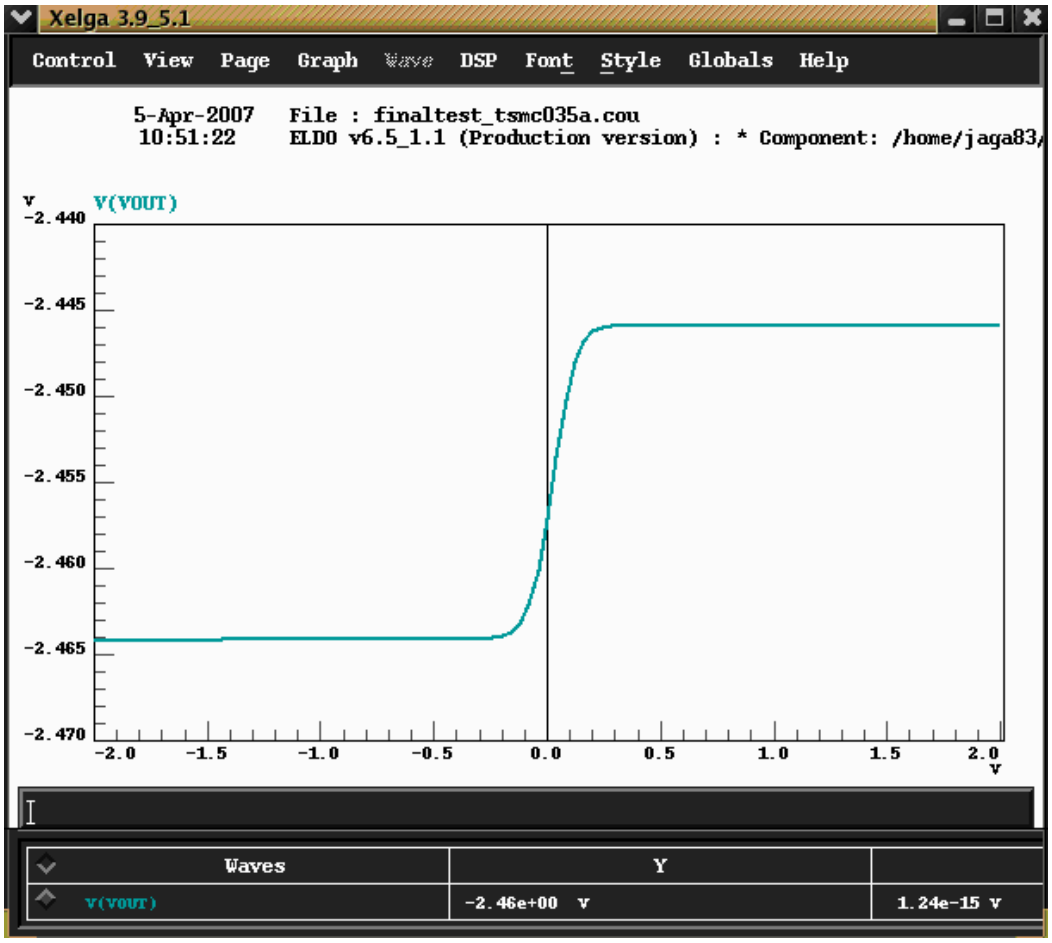


**Figure 4.4:** The input offset voltage Vos.

A course sweep of Vin is made from -2.5 to +2.5 to find the value of Vin, where the output makes the transition from Vss to $V_{DD}$. The value of Vos (offset voltage) is determined as **-2.457mV**.

### 4.3.1 The DC gain.

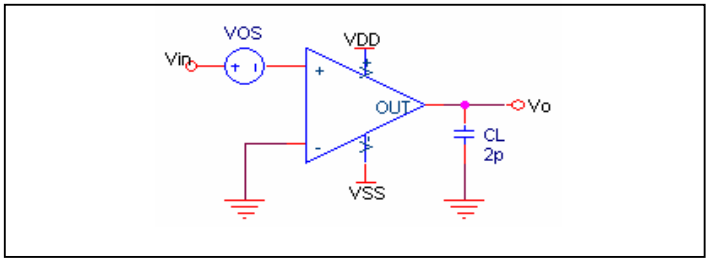


**Figure 4.4.1:** Configuration for the measurement of the open loop gain.

The gain was measured using the configuration shown in Figure 4.4.1, above, because it allows the direct measurement of Vo/Vin at dc. As per calculation,

$$\frac{vo}{vi} = \frac{g_{m2} \times g_{m6}}{(g_{ds2} + g_{ds4}) \times (g_{ds6} + g_{ds7})}$$
$$= \frac{210.163\mu \times 867.633\mu}{(477.05n + 633.202n) \times (4387.6n + 3290n)}$$
$$= 21{,}334.05229$$
$$= 86.58dB$$

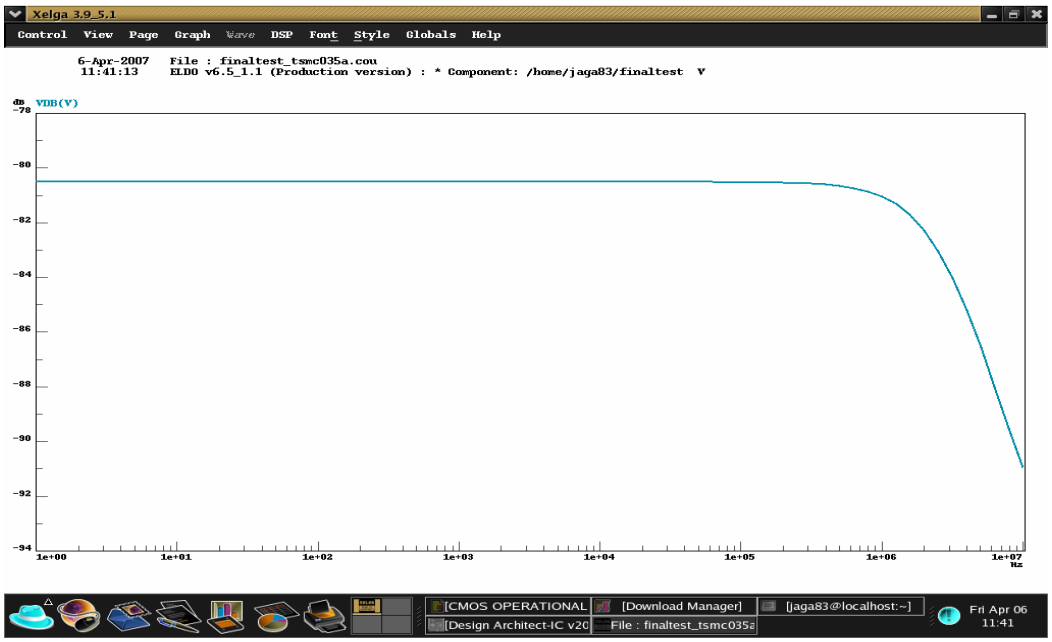


**Figure 4.4.1.0**: DC gain and -3dB frequency of the amplifier.

Figure 4.4.1.0 shows the DC gain is 80.5dB to be exact and frequency of 2MHz.

### 4.3.2 Unity gain frequency (GBW).

The unity gain frequency was not much of a limitation on the design until the final stages, at which point it was necessary to make small modifications to Cc to trade off frequency response for settling time. This resulted in the unity gain frequency of 74.33 MHz.

$$fu = \frac{g_{m2}}{2\pi C_C} = \frac{\sqrt{I_{D5} k_p (\frac{W}{L})_2}}{2\pi C_C} \geq 50MHz$$
$$= \frac{210.163\mu}{2\pi(0.45\text{P})}$$
$$= 74.33MHz$$

### 4.3.3 Output Swing.

The output swing of the device was not a major constraint on the design, but was even less so in simulations than in hand calculations. The difference between hand calculations and simulation was due to the short channel nature of the devices, which caused the $V_{DSAT}$ of the devices to be less than the ($V_{GS}$-$V_{th}$) that long channel theory predicts. This effect was more pronounced in the PMOS devices, which had a smaller $L_{eff}$. The circuit in Figure 4.4.3 was used to measure the output swing of the amplifier.

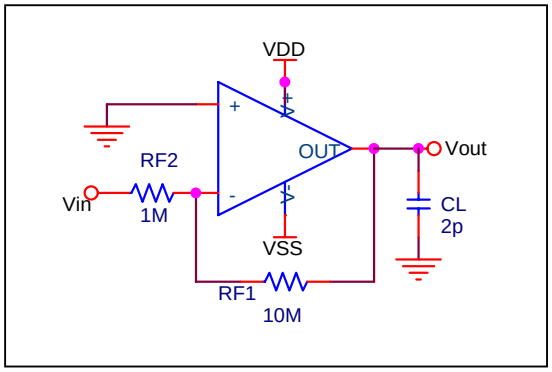


**Figure 4.4.3**: The configuration for the measurement of the output swing.

The positive output voltage swing is given by:

$$Vout^{+} = VDD - |V_{DSAT7}| whereby, |V_{DSAT7}| = \sqrt{\frac{2I_{D7}}{k_p(\frac{W}{L})_7}} \leq 0.3$$

$$Vout^{+} = 2.5 - 0.69$$

$$Vout^{+} = 1.81V$$

The negative output voltage swing is given by:

$$Vout^{-} = VSS - |V_{DSAT6}| whereby, |V_{DSAT6}| = \sqrt{\frac{2I_{D7}}{k_p(\frac{W}{L})_6}} \leq 0.3$$

$$Vout^{-} = -2.5 + 0.69$$

$$Vout^{-} = -1.81V$$

### 4.3.4 Common-Mode Input Range.

In hand calculations, the CMR appeared to be the most limiting constraint for the design, requiring a small value for $I_{D5}$ and large values for $(W/L)_5$ and $(W/L)_2$. In simulations, however, the CMR posed no limit on the design and stayed relatively independent to design changes. The CMR was measured using the circuit in Figure 4.4.4 by sweeping the input voltage from $V_{SS}$ to $V_{DD}$. This configuration was chosen because, in a high gain configuration, the output swing of the amplifier limits the linearity of the circuit.

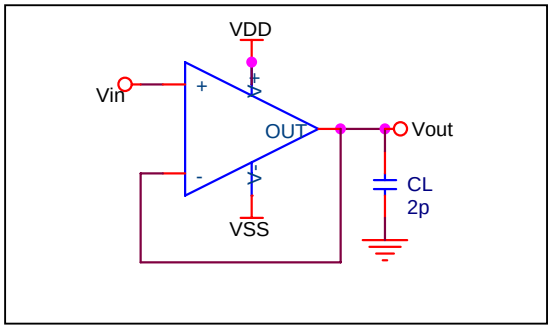


**Figure 4.4.4:** The configuration for the measurement of the CMR.

The negative common mode input range is given by:

$$CMR^{-} = VSS + V_{GS3} + |V_{DSAT1}| - |V_{GS1}| = \sqrt{\frac{I_{D5}}{k_n(\frac{W}{L})_3}} \leq 0.75V$$

$$CMR^{-} = -1.83V$$

The positive common mode input range is given by:

$$CMR^{+} = VDD - |V_{DSAT5}| + |V_{GS2}| = \sqrt{\frac{2I_{D5}}{k_p(\frac{W}{L})_5}} + \sqrt{\frac{I_{D5}}{k_p(\frac{W}{L})_2}} + Vto \leq 0.75$$

$$CMR^{+} = 1.08V$$

### 4.3.5 Power Dissipation

Figure 4.4.5 below shows the configuration for the measurement of the open loop power dissipation.

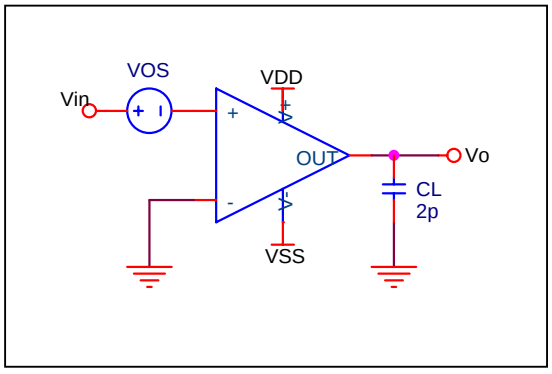


**Figure 4.4.5:** Circuit for the measurement of the open loop power.

(ID8 + ID5 + ID7)*(VDD-VSS) ≤ 250uW, or, (ID8 + ID5 + ID7) ≤ 50uA

=200µW

## 4.4 The Design Performance

**Table 3.0** : Comparison between design objective and simulated values.

| **Parameter** | **Design Objective** | **Simulated Performance** |
|---|---|---|
| DC Gain | 85 dB or more | 80.5dB |
| Common Mode Input Range: Positive | 1.75 V or more | 1.08 V |
| Negative | -1.75 V or less | -1.83 V |
| Output Swing: Positive | 2.2 V or more | 1.81 V |
| Negative | -2.2 V or less | -1.81 V |
| Power Dissipation | 250uW or less | 200uW |
| Unity Gain Frequency | 50 MHz | 74.33MHz |

## 4.5 Layout

Figure 4.7 shows the layout of CMOS operational amplifier. The layout is practiced in Mentor Graphics IC Station. After the layout has been drawn, DRC (design rule check) and LVS (layout versus schematics) simulation was done.

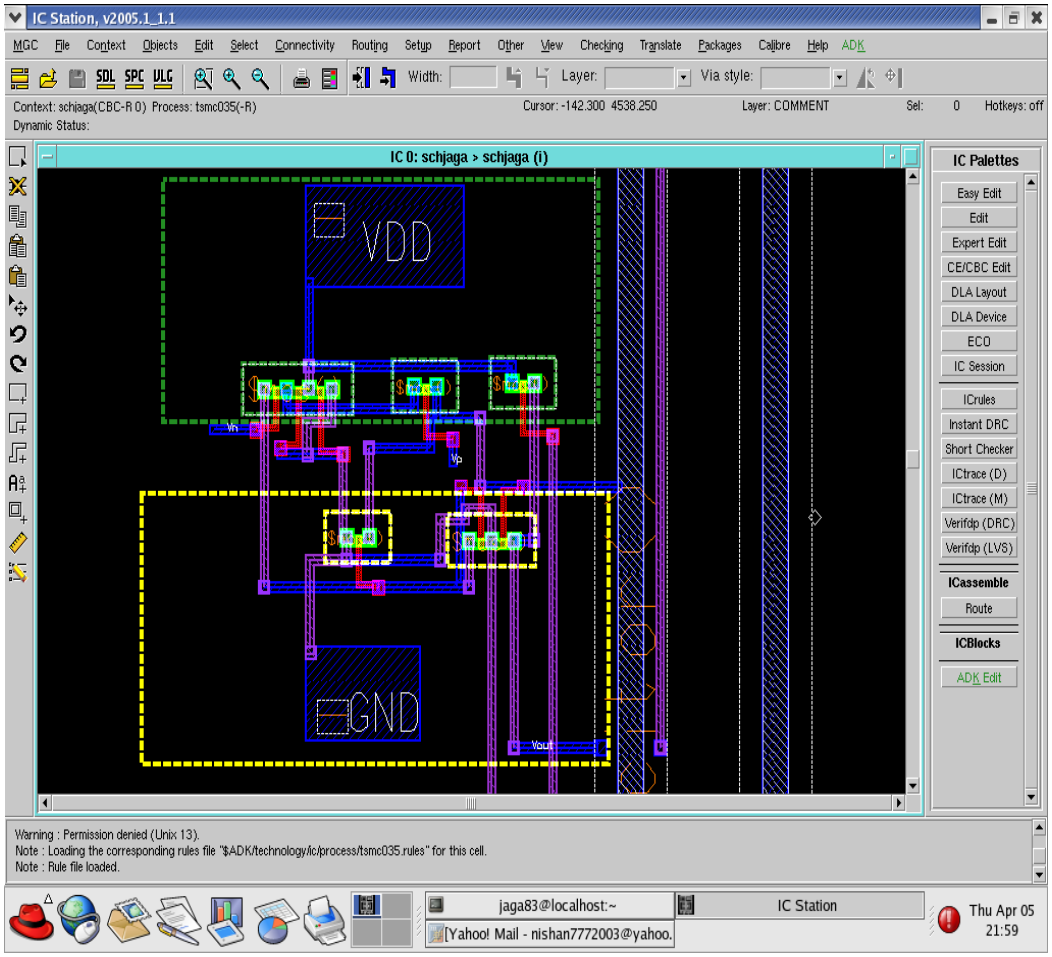


**Figure 4.7:** Layout for designed CMOS op-amp.

## 4.6 DRC AND LVS

Figure 4.8 above shows the DRC (design rule check) simulation results. Initially there was 35 DRC errors, such as metal to poly distance error, overlaps, contact to poly errors, p-well n n-well errors. Figure 4.9 shows the LVS (layout versus

schematic) simulation results. Initially there was 17 errors, such as missing gate, missing instance and missing ports. All the errors then cleared patiently at last.

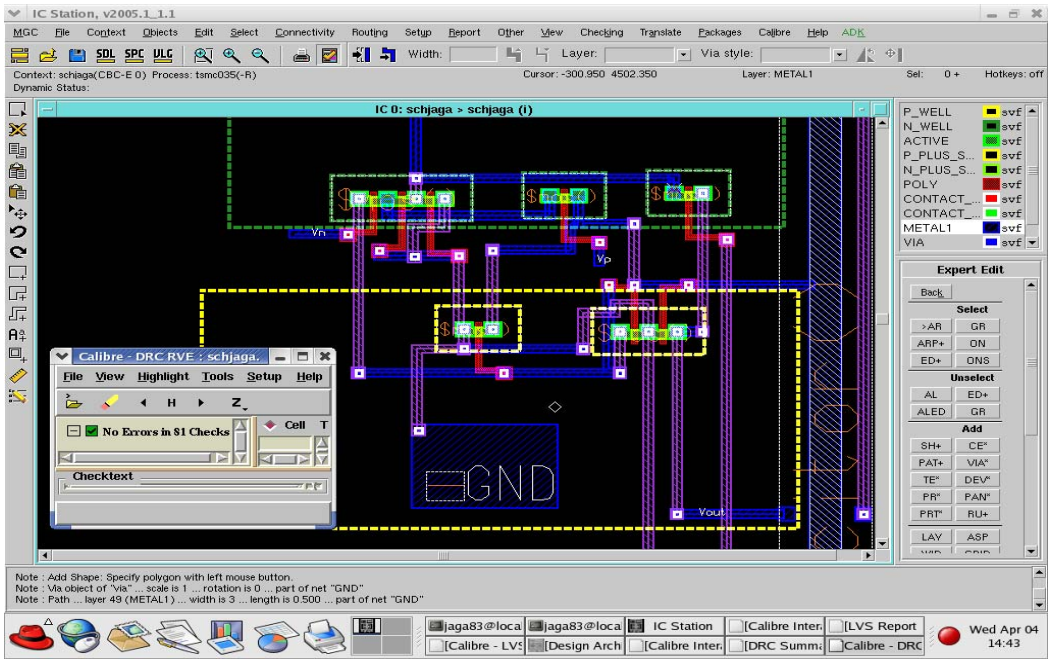


**Figure 4.8:** DRC (design rule check).

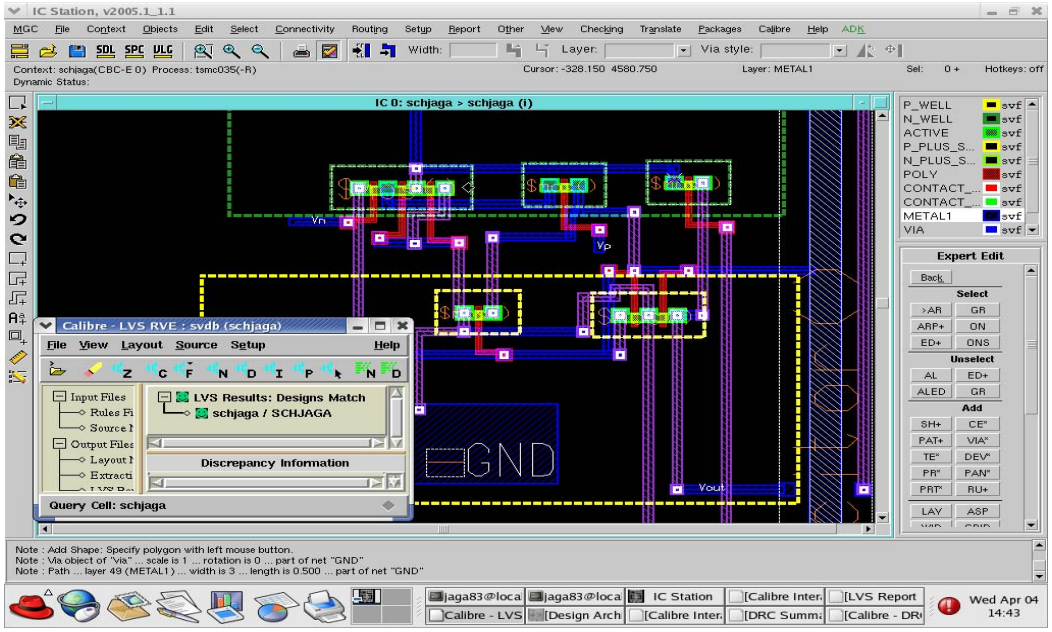


**Figure 4.9:** LVS (layout versus schematic).

## 4.7 Discussion

Overall, the final design performed above and beyond the design specification. In particular, the unity gain frequency, and power particularly excelled. The low power biasing, the moderate to small device size and hence small device capacitances, and the moderate current available to charge the capacitances helped to meet and improve on the design specifications. There are few issues affected the whole circuit and are described here.

Initially there were problems in meeting the DC gain and the unity gain bandwidth specifications. Those problems were then resolved by adjusting the biasing currents in the 2 gain stages, especially in the first, by varying the widths of the transistors.

Another issue that hampered the initial design stages was the fact that the calculated values differed somewhat from the simulated values, as can be seen in Table 3.0. It appears that short channel effects caused the differences in gain and in the output swing and CMR values. With an Leff of 0.44 um for the PMOS transistors and 0.56 um for NMOS, short channel effects become significant, reducing the gain and $V_{DSAT}$ of the devices, especially for the smaller PMOS transistors.