CHAPTER 3

METHODOLOGY

The methodology is undertaken of this project are divided into two main parts. The first part is designing the switching pulse using VHDL programming and the second part is developing the hardware.

3.1 Project methodology

The flow chart in Figure 3.1 as shown details the methodology used in this project. It is consists of four stages including the development of the software and hardware of the control circuit.

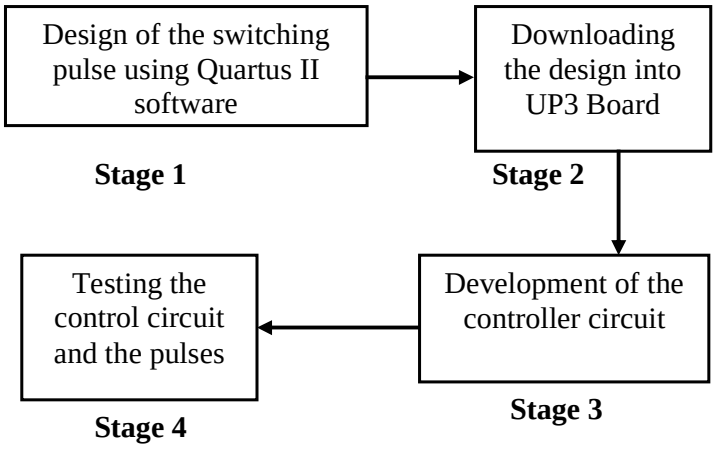


Figure 3.1: The project methodology

At the first stage, the switching pulse is designed based on theories and the Quartus II software environment. In the next stage, the FPGA (Field Programmable Gate Array) technology by using the UP3 board as main controller. The predetermined duty cycle and frequency is then programmed using Quartus II software. Next stage is to develop of the controller circuit. The controller circuit consists of the buffer, interface circuit. Development of the control circuit is done after the generated signal from the main controller is simulated and downloaded. Each stages of the circuit design are tested through

experiments. The testing for overall circuit is done and the output signal from the control circuit is compared with the one calculated in theories. The control circuit is used as the signal generator for the single phase full bridge inverter circuit to be tested.

3.2 Designing switching pulse

At the first stage, the design of the switching pulse is studied based on theories and the Quartus II software environment. Then the calculation for the duty cycle and frequency of the sinusoidal pulse width modulation (SPWM) to be generated is calculated. Generally Computer Aided Design (CAD) software makes it easy to implement a desired logic circuit by using programmable logic device, such as a field-programmable gate array (FPGA) chip. Figure 3.2 shown that the progress flow for the switching pulse design approach.

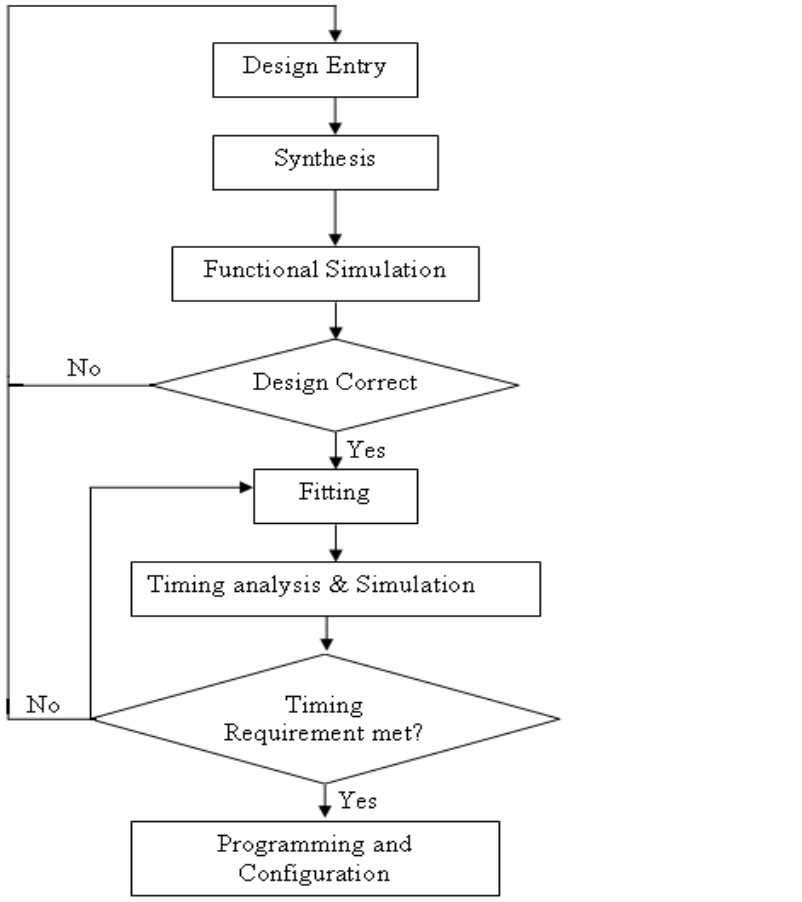


Figure 3.2: SPWM Switching Pulse

The design flow involves the following basic steps:

1) Design Entry – the desired circuit is specified by using hardware description language, VHDL.
2) Synthesis – the CAD (Computer Aided Design) Synthesis tool synthesizes the design into a netlist that gives the VHDL coding needed to realize the coding.
3) Functional Simulation – the synthesized VHDL coding is tested to verify its functional correctness; the simulation does not take into account any timing issues.
4) Fitting – the CAD Fitter tool determines the placement of the VHDL coding defined in the netlist into the Les (logic elements) in an actual FPGA chip; it also chooses routing wires in the chip to make the required connections between specific Les.

5) Timing Analysis – propagation delays along the various paths in the fitted VHDL or design are analyzed to provide an indication of the expected performance of the circuit.
6) Timing Simulation – the fitted VHDL or design is tested to verify both its functional correctness and timing.
7) Programming and Configuration – the designed is implemented in a physical FPGA chip by programming the configuration switches that configure the LEs and establish the required wiring connections.

3.3 Downloading the Design into UP3 Board

The important thing before downloading the design is the design should been clearly with errors during compilation and simulation process. Figure 3.3 shown that the summary of compilation process before creating the block diagram; if the flow summary like as Figure 3.3 appears, the process could continue to the next process.

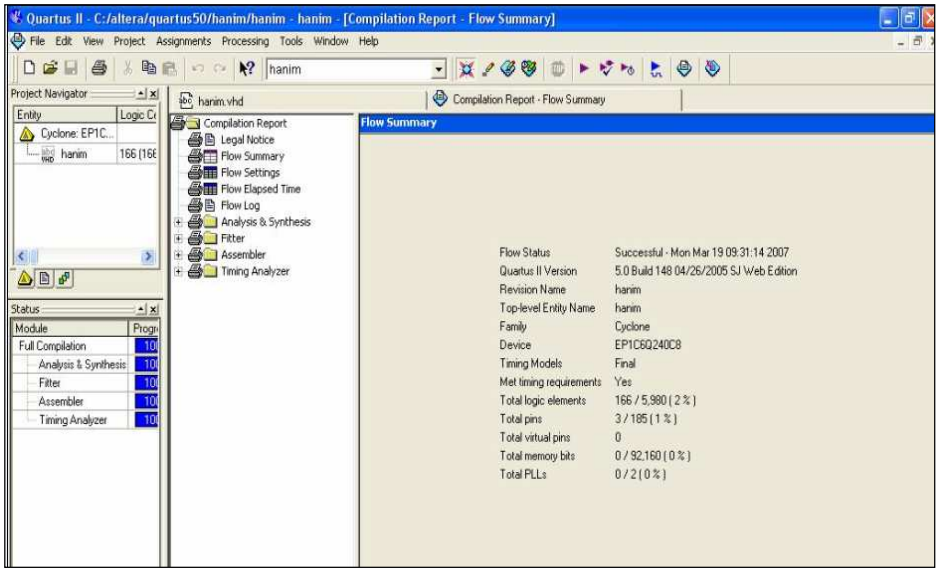


Figure 3.3: Summary for compilation of VHDL Programming

From that successful design, the block diagram had been created. The input and output pin had been created based on the design; which is had one input and two output. Figure 3.4 is shown the block diagram.

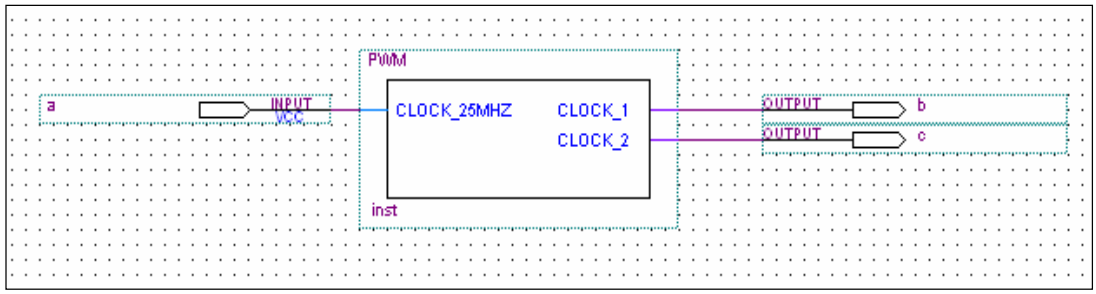


Figure 3.4: Block Diagram

The input and output pin had been assign based on UP3 Board manual. It is because all pins on UP3 board had their own function. Output pin b and output pin c from block diagram are using J2 connector, FPGA pin number is 194 for output b and 195 for output c as shown in Figure 3.4. Figure 3.5 is shown the FPGA pin number.

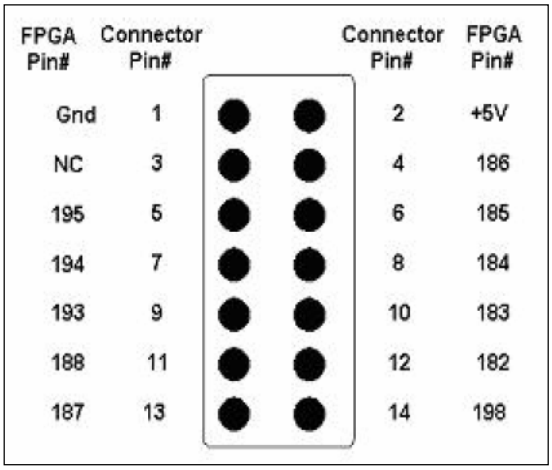


Figure 3.5: Expansion prototype connector-J2

J2-connector had 14 connector of pins which is had their function. Each of the pin number is equal to FPGA pin number. The function of FPGA pin number had been referred on UP3 board manual [12]. Active serial configuration is carried out through serial configuration device EPCS1. Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone FPGA read configuration data via the serial interface decompresses data if necessary and program their SRAM cells. These scheme is referred to as an AS configuration scheme because the FPGA controls the configuration interface. The Quartus II software automatically generates files that can be downloaded into the configuration devices using Byte-Blaster II for Active serial configuration. Figure 3.6 is shown that pin had using to load the design.

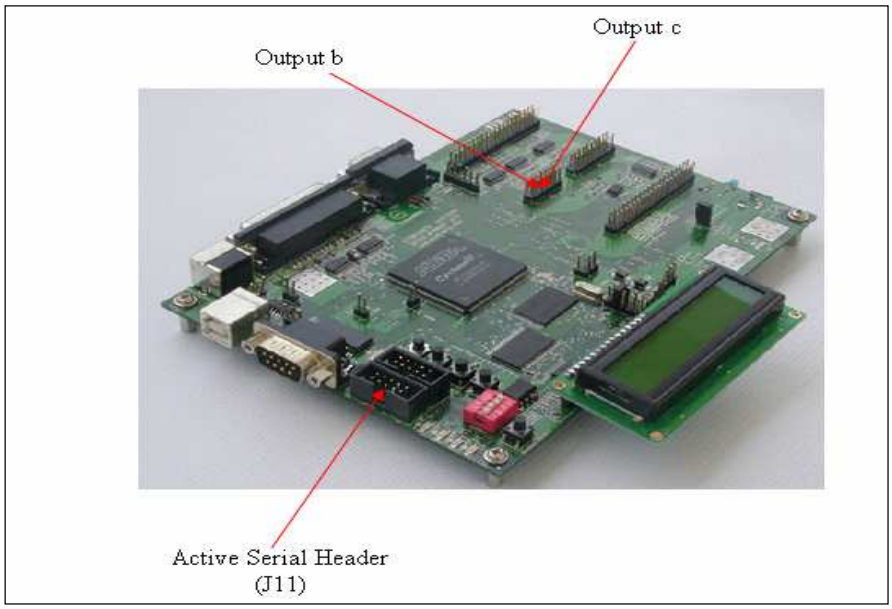
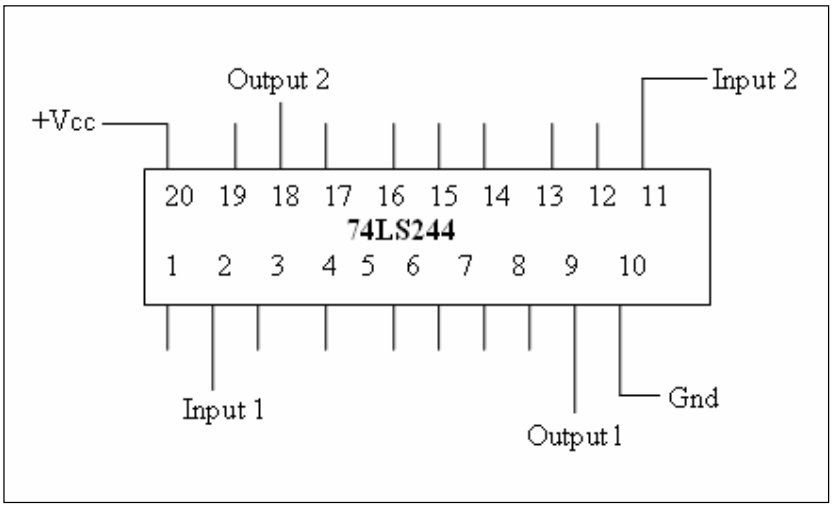


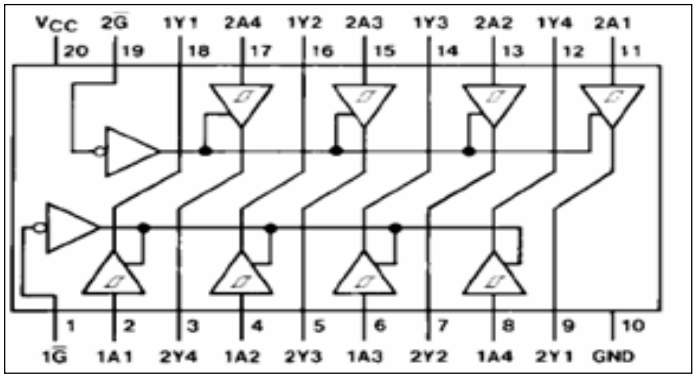
Figure 3.6: Connection till load the design

3.4 Development of the controller circuit

This part details the hardware part, where is included buffer, interface circuit, and single phase bridge inverter. Figure 3.7 is shown the connection diagram for buffer. Output from UP3 board is becomes an input for the buffer. This buffer is used to provide improved noise rejection.



a)



b)

Figure 3.7: (a), (b) Connection Diagram

Figure 3.7 (a) and (b) are shown the connection diagram of buffer by using 74LS244 chip. Figure 3.7 (a) illustrated the connection pin had used for this project and also shown that unused pin for no connection. Figure 3.7 (b) shown that the connection diagram based on the datasheet [13]. To connect the 74LS244 chip for this project; the datasheet and function table for connection 74LS244 as shown in Table 3.1 must be referred.

For this project; the inverter is desired to produce purely sine wave of the output voltage with less harmonics contents. To produce proper design of the control signal with high flexibility by using 74LS244 chip in this project as the buffer This buffer provide improved noise rejection and high fan out output Proper designs of control signal with powerful switches are very important in order to reduce the harmonics contents of the inverter output voltage. This approach hopefully will replace the existing analog controller due to it ability to produce precise control, low overall system cost, lower power dissipation and resulting longer life of operation.

Table 3.1: Function table for connection 74LS244

Output Enable	Input	Output
1G,2G	1A,2A	1Y,2Y
0	0	0
0	1	1
1	Either 0 or 1 logic level	High impedance

Table 3.1 illustrated that the function table for 74LS244 chip. The chip had two inputs; it is G input and A input and one output. If G input in low logic level (0), A input also in low logic level (0), the output is in low logic level (0). When G input in low logic level (0), A input in high logic level (1), the output is in high logic level. If G input

in high logic level (1), A input in either low or high logic level (0 or 1), the output is in high impedance.

The output from the buffer is input to the interface circuit. The interface circuit had used to high the voltage because the output voltage from the buffer is low.

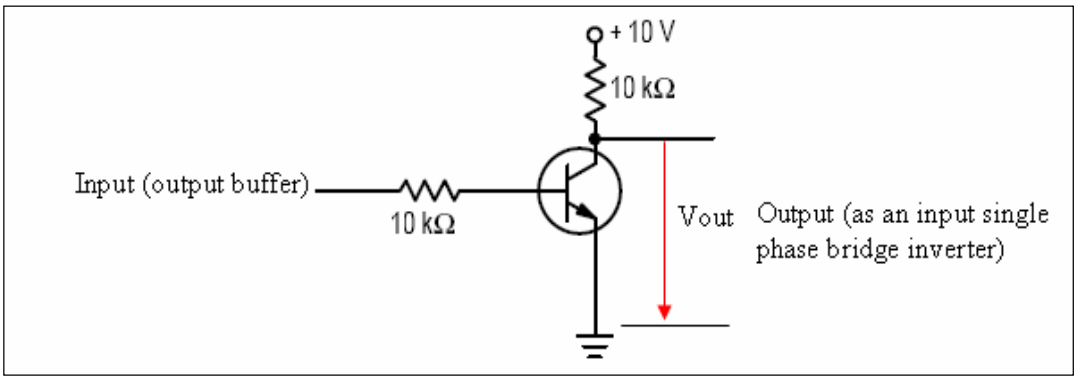


Figure 3.8: Interface Circuit

Figure 3.8 is shown the interface circuit; which is need 10Volts of voltage supply, an input of this circuit is comes from output of buffer. The output from interface circuit is becomes the input for single phase bridge inverter. The output from this circuit should be higher than the input, because the interface circuit is used to increase the voltage from output voltage of buffer.

Single phase bridge inverter is the last part of this project. Figure 3.9 illustrated the single phase bridge inverter scheme.

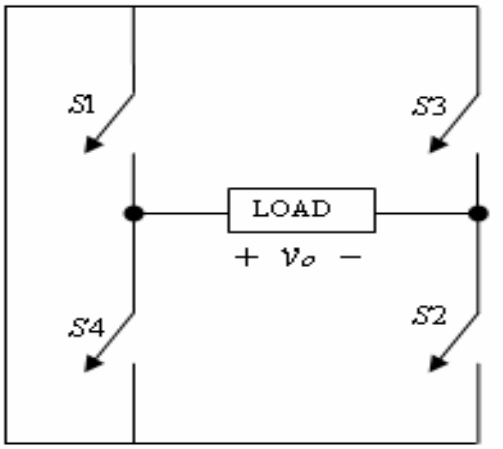


Figure 3.9: Single Phase Bridge Inverter

The basic single phase bridge inverter topology with the control circuit is shown in Figure 3.9. The single bridge inverter consists of four switches represented by switches S1 through S4. Channel 1 consists of switches S1 and S4, while channel 2 consists of switch S2 and S3. The switches (S1 and S2) and (S3 and S4) are operated as two pairs during switching time. The control strategy is performed in such away a pair (S1 and S2) of switches is turn on during another pair (S3 and S4) is turn off. The sequences of on and off of the switches occurred continuously and sequentially. This produces and alternating output voltage across the load. Different switching scheme produces different shape of the output voltage across the load of the inverters.

Table 3.2 is shown the control strategy represented by channel 1 and channel 2 that consists of switches S1 through S4. The control strategy is performed in such away a pair (S1 and S2) of switches is turn on during another pair (S3 and S4) is turn off that occurred continuously and sequentially.

Table 3.2: The inverter switching control strategy

SPWM Pulse	Switches	
Channel 1	S1	S4
Channel 2	S2	S3

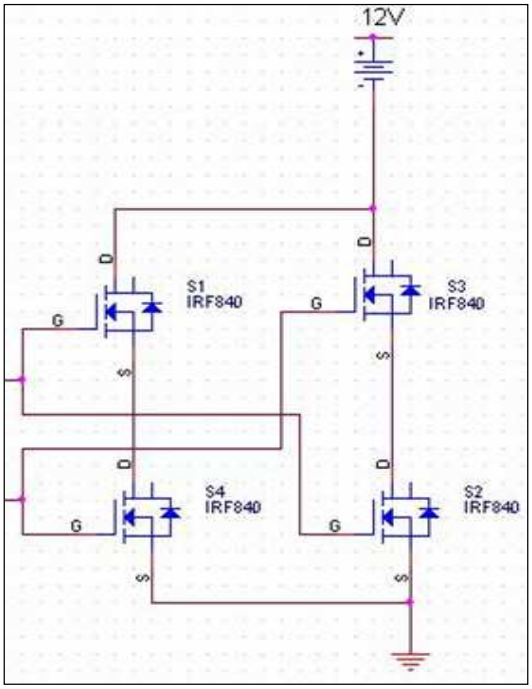


Figure 3.10: Inverter Circuit

The control signals of an inverter like as the pulse width modulated inverter switching scheme is shown in Figure 3.11. The waveform similar to a pulse width modulated waveform that used the control signals to control the inverter switches. For the pulse width modulated inverters, the control signals used to control the inverter switches is shown in figure 3.11 (a) and (b) represented as $g1$ and $g2$ respectively. The gating signal $g1$ is in the form of pulse width modulated waveform used as a control signal for switches S1 and S2. Another control signal $g2$ is for switches and S3 and S4. The following describes the switch on states and the corresponding voltage levels

1. S1, S2 on: $v_{AN} = +V_{DC}$, $v_{BN} = 0$; $v_o = v_{AN} - v_{BN} = +V_{DC}$
2. S3, S4 on: $v_{AN} = 0$, $v_{BN} = +V_{DC}$; $v_o = v_{AN} - v_{BN} = -V_{DC}$
3. S1, S3 on: $v_{AN} = +V_{DC}$, $v_{BN} = +V_{DC}$; $v_o = v_{AN} - v_{BN} = 0$
4. S2, S4 on: $v_{AN} = 0$, $v_{BN} = 0$; $v_o = v_{AN} - v_{BN} = 0$

The output voltage from the pulse width modulated inverter switching scheme is shown in Figure 3.11(e). It has a waveform similar to a pulse width modulated waveform used as the control signals to control the inverter switches and changes between zero to $+V_{DC}$ or between zero to $-V_{DC}$ voltage levels. The advantage of this switching technique it is has effectively doubling the switching frequency and it appears in the harmonic spectrum of the output voltage waveform, where the lowest harmonics appears in sidebands of twice the switching frequency. This produces the output voltage with fewer harmonic as the switching frequency is increased.

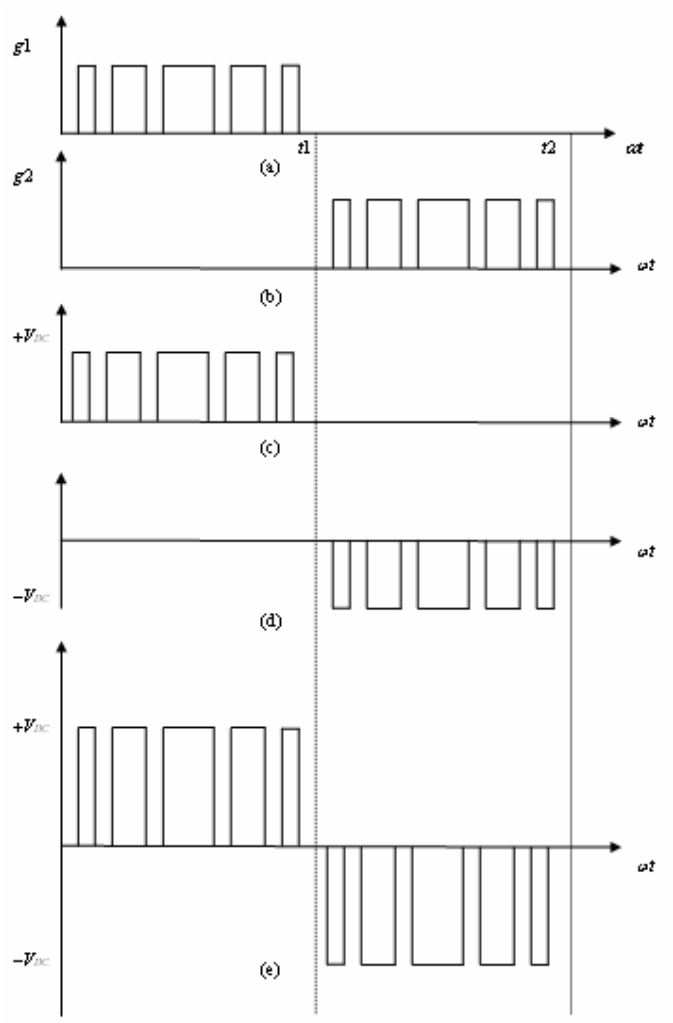


Figure 3.11: PWM inverters; (a), (b) switching signals, (c) V_{AN} , (d) V_{BN} , (e) v_o

In order to explain this switching scheme, the basic bridge inverter circuit as shown in Figure 3.9 is referred. The diagonally opposite switches (S1, S2) and (S3, S4) from the two channels are switched as switch pairs 1 and 2 respectively. This PWM switching method produces the output voltage of channel 1 is identical to the output of the basic one-leg inverter. The output of the inverter channel 2 is negative of the channel 1 output.

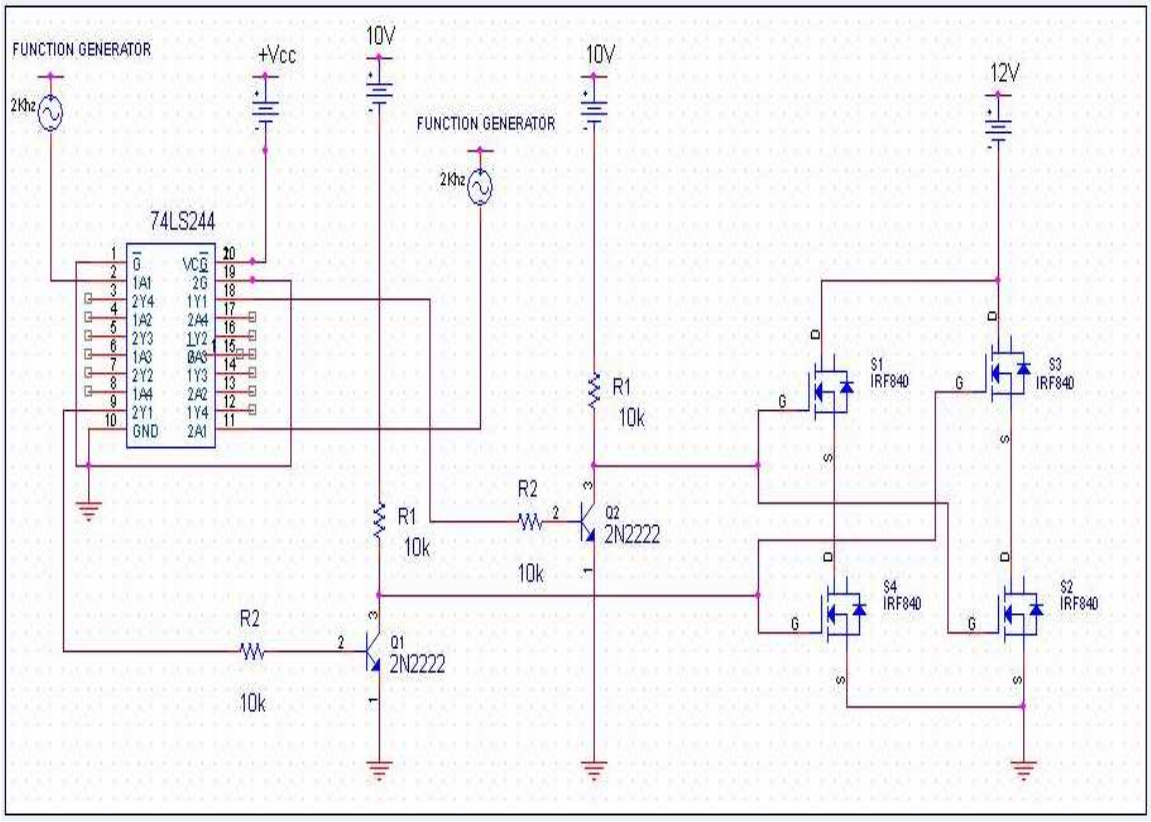


Figure 3.12: Control Circuit Schematic

3.5 Testing Control Circuit and the Pulses

The control circuit schematic and actual control circuit as shown in Figure 3.12 and 3.13.

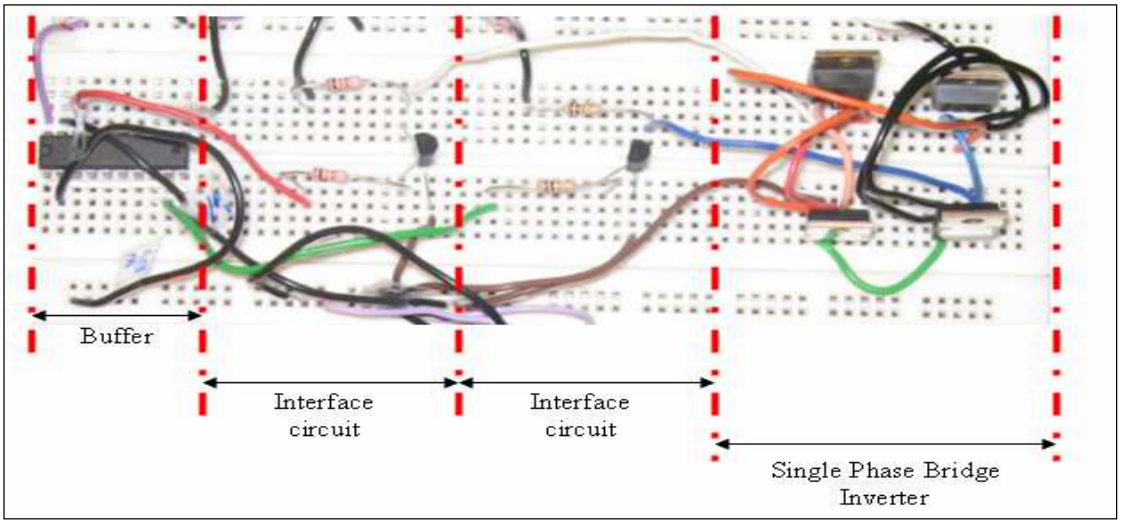


Figure 3.13: Actual Control Circuit

Figure 3.13 is shown that the actual of control circuit, which is buffer, interface circuit and single phase bridge inverter circuit. The two outputs from buffer become the input for interface circuit. Each output from buffer is input for each interface circuit. The output from interface circuit as a input of single phase bridge inverter circuit.

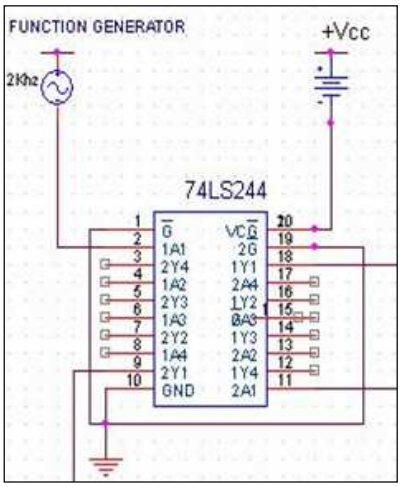


Figure 3.14: Buffer Circuit

Figure 3.14 shown that the buffer circuit, which is used 74LS244 chip. This chip had 20 pins. This project had used 8 pins. The input (pin number 20) of this circuit is 5v of supply voltage and function generator (pin number 2). The grounding connection is pin number 10. Pin number 1 and 19 which are labeled with G and 2G is an output enable and connect to ground. The other pin (pin number 9 and 18) are connected to input of interface circuit.

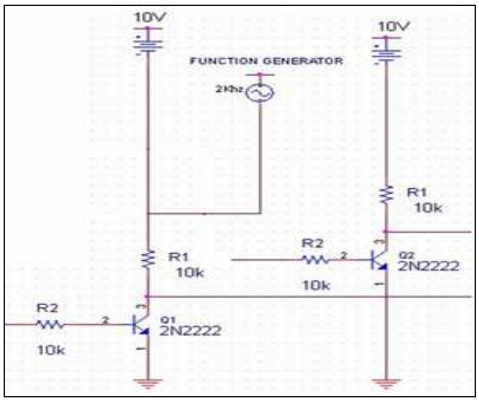


Figure 3.15: Interface Circuit

Figure 3.15 shown an interface circuit, which is had two parts of interface circuit. The input voltage is 10v. This circuit used resistor and transistor only. The function of interface circuit is to high the output voltage from buffer.

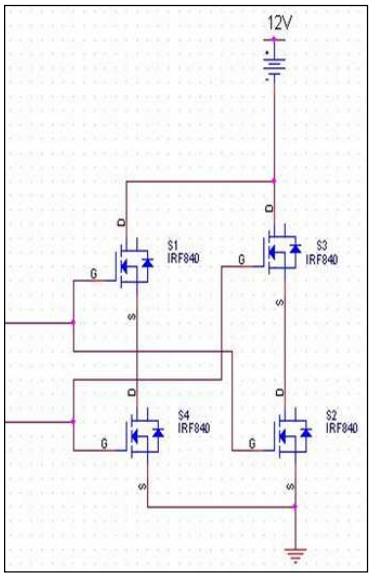


Figure 3.16: Inverter Circuit

Figure 3.16 is shown that an inverter circuit which is used IRF840 chip. The input of this part is from output of interface circuit. This circuit had used 12v for voltage supply.

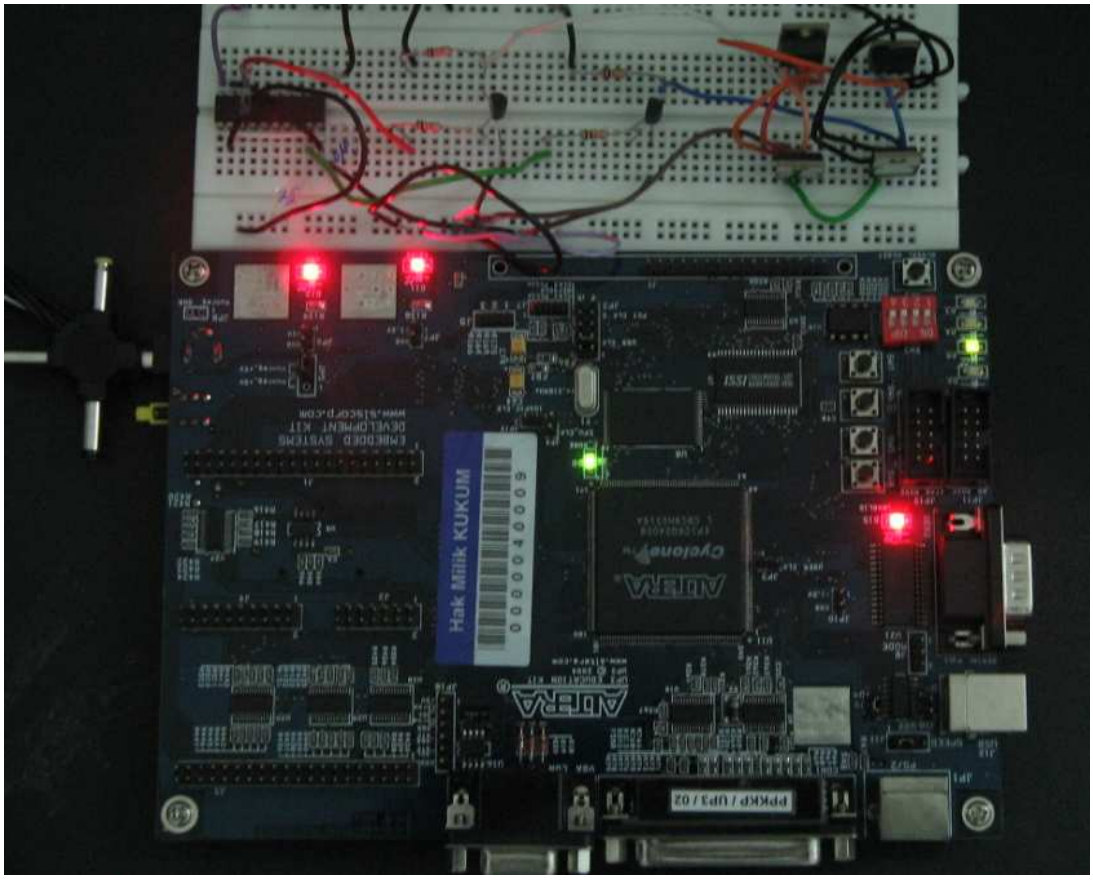


Figure 3.17: Connection for testing Control Circuit

Figure 3.17 are shown the actual control circuit and UP3 board connection for testing the output. The connection shown like as in figure, which is the output from UP-3 board becomes the input of buffer and the overall output had checked from output of inverter circuit that can see on oscilloscope. The details of pulses or output had discussed in the next chapter.