DESIGN AND IMPLEMENTATION OF A VGA DISPLAY GENERATOR USING FPGA

HASLINDA BINTI HASSAN

SCHOOL OF MICROELECTRONIC ENGINEERING
UNIVERSITI MALAYSIA PERLIS
2007

DESIGN AND IMPLEMENTATION OF A VGA DISPLAY GENERATOR USING FPGA

by

HASLINDA BINTI HASSAN

Report submitted in partial fulfillment
of the requirements for the degree
of Bachelor of Engineering

APRIL 2007

APPROVAL AND DECLARATION SHEET

This project report titled Design and Implementation of a VGA Display Generator Using FPGA was prepared and submitted by Haslinda binti Hassan (Matrix Number: 031030117) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in Universiti Malaysia Perlis (UniMAP).

Checked and Approved by

_____

(PN SITI ZARINA MOHD. NAZIRI)
Project Supervisor

School of Microelectronic Engineering
Universiti Malaysia Perlis

March 2007

REKABENTUK DAN PENGGUNAAN PAPAN SKRIN VGA MENGGUNAKAN PERANTI FPGA

ABSTRAK

Projek ini adalah aplikasi kepada skrin VGA dengan menggunakan peranti FPGA. Sasaran projek ini ialah untuk menghasilkan suatu imej video. Imej tersebut ialah sebiji bola yang berbentuk segiempat yang boleh menghasilkan imej gerakan yang bergerak secara melintang di skrin VGA. Projek in menggunakan papan pembangunan UP2 oleh Altera dengan menggunakan cip FLEX10K. Program ditulis dalam bahasa tinggi VHDL.dengan menggunakan Quartus II. Imej keluaran akan dipaparkan pada monitor VGA yang mempunyai piksel 640 x 480. Projek ini mengandungi dua program kecil dan satu program akhir yang akan menggabungkan kedua-dua program kecil tersebut. Program pertama menghasilkan isyarat video, program kedua untuk mengaktifkan paparan tujuh bahagian. Program akhir adalah untuk menghasilkan imej objek dan pergerakan objek. Secara keseluruhannya, projek ini berjaya memenuhi objektif dengan menghasilkan paparan imej video yang diinginkan.

DESIGN AND IMPLEMENTATION OF A VGA DISPLAY GENERATOR USING FPGA

ABSTRACT

This project is an implementation of a VGA display generator, using FPGA device. The goal of this project is to design a simple video image. The image is a square ball shape in red color that bounces up and down the screen of a monitor. This project is using Altera UP2 board, FLEX 10K device. The source code is designed using VHDL language processed using Quartus II Design Software. The output is displayed using a standard VGA monitor with 640 by 480 pixels. The design of this project consists of two sub programs, and one top level entity. All three programs compiled and simulated individually. The first sub program is to generate timing signals for VGA display, the second sub-program is a seven segment display needed to track the vertical motion of the image. Both programs are combined in one entity. The top level entity combines all sub programs, and most importantly it draws the shape of the ball and provides the motion for the ball. Final output produced the targeted result with a red square ball moves vertically up and down the screen, and seven segment display produce a counting in hexadecimal in rapid movement which shows the ball is in motion mode. Overall, this project has reached its objectives.

TABLE OF CONTENTS

CHAPTER 3 MATERIALS AND METHOD

CHAPTER 4 RESULTS AND DISCUSSION

CHAPTER 5 CONCLUSION

APPENDICES

LIST OF TABLES

LIST OF FIGURES