CHAPTER 3

FABRICATION AND PROCESS PARAMETERS

3.0. Introduction

The fabrication process of the microfluidic capacitor adopts the CMOS fabrication techniques. It is fabricated on a silicon wafer. The processes involve mask designing, channel formation on silicon wafer, photolithography, thermal oxidation, metal deposition, electroplating, and anodic bonding. A total of 10 capacitors of the same dimensions were designed.

3.3 Mask Design

Masks are used as a stencil to generate patterns onto a resist coated wafers. In this project, the direct contact approach is adopted. The mask contains opaque and transparent areas that respectively hinder or allow ultraviolet rays' penetrate through. The image transfer will be of 1:1 ratio. The following describes the steps to design the mask for this fabrication purpose. The designs were made with the aid of drawing software, AutoCAD. Two masks were required for this process. Mask 1 is for interdigitated electrodes and fluid channel formation and Mask 2 is for aluminium seed deposition for electroplating.

3.1.1 Mask Design Steps

Step 1: Frame dimensions and outline of the wafer is drawn. The frame is 5 X 5 inches, to cater to the masks aligner's dimensions. The wafer's diameter is 100mm.

Step 2: The alignment mark is designed using the following dimensions. These marks serve as references for mask alignments.

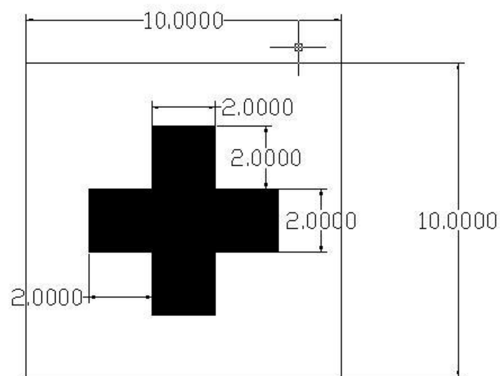


Figure 3.1: Dimensions of the alignment mark

Step 3: Mask 1 is designed. The interdigitated electrodes and fluid channels are embedded on the silicon wafer. This mask contains the design for those channels. The dimensions are critically miniscule. The following figure illustrates the design and its dimensions.

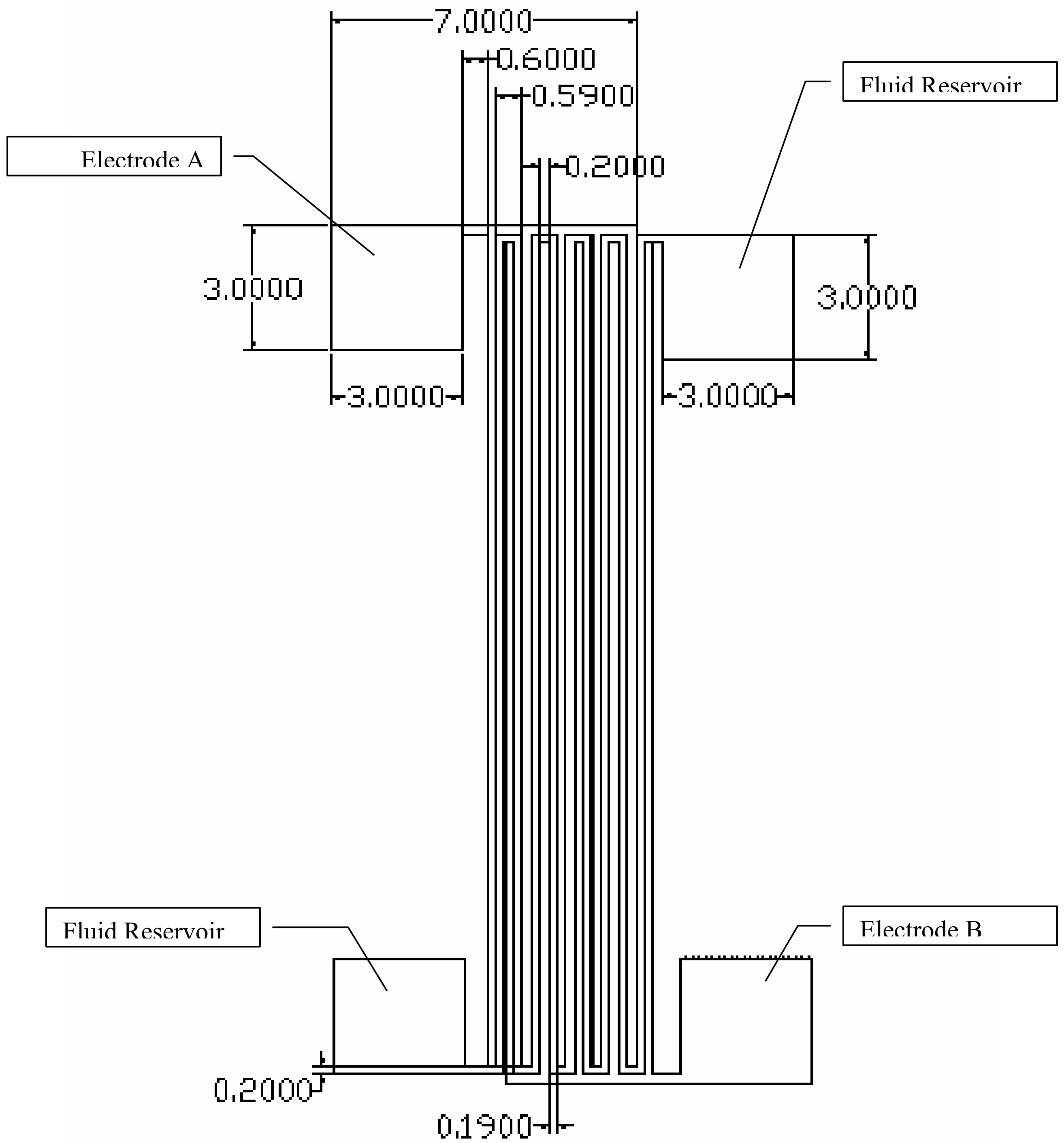


Figure 3.2: Dimensions of the microfluidic capacitor: Pattern drawn on mask 1

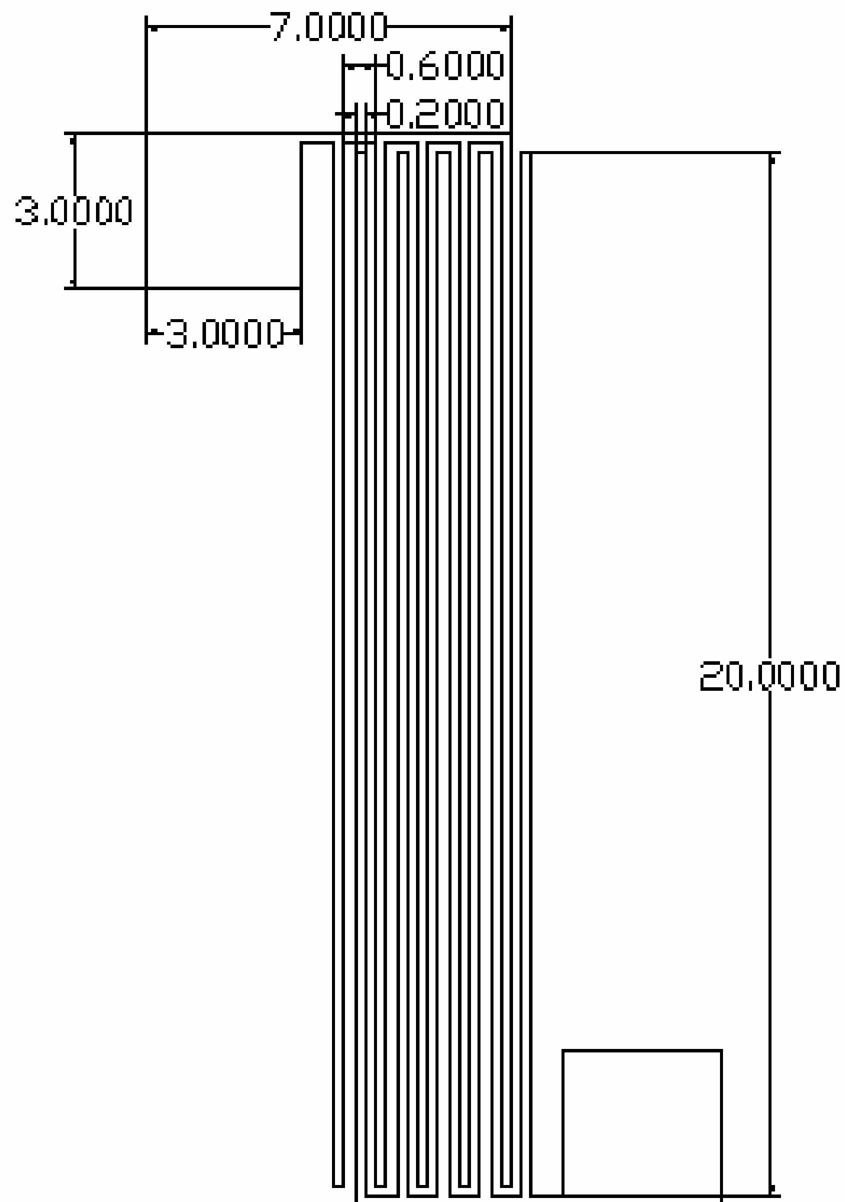


Figure 3.3: Dimensions of the aluminium electrode: Pattern drawn in mask 2

3.2 Wafer Specification and Measurements

3.2.1 Parameter Test

The wafers that come from the supplier normally follow consistent specifications. However, they may vary within a given tolerance. Prior measurements are made to verify the specifications of the wafer before the actual fabrication process. Parameters like native oxide thickness, sheet resistance, wafer type and thickness are made as they may influence the process parameters as well as the characteristic of the fabricated devices.

3.2.2 Native Oxide

The wafer might carry a certain amount of oxide called native oxide due to its exposure to oxygen dissolved in moisture. At room temperature, it has a growth rate of approximately 15 Å per hour. Oxygen molecules that are dissolved in water penetrates into the silicon surface causing oxidation to occur.

This oxide prohibits the usual electrical characteristics of the silicon wafer as SiO_2 is not conductive. It disrupts the performance and reliability of the wafer. Sometimes, it may even carry metallic impurities that further contaminate the chemical properties of silicon.

To remove this, the wafer is immersed into Buffered Oxide Etch for approximately 30 seconds.

3.2.3 Sheet Resistance

Sheet resistance is the most practical technique to evaluate the end-to-end resistance of a thin square film on the wafer. This value is independent of the size of the square sheet. Four point probes are used to do this measurement. A common multimeter may not do this task as excessive contact resistance is present on the interface between he probes and the wafer material.

The four point probe works on the good old Ohm's Law. It is made up of four probes spaced equally apart. A known current is passed through the material via the two external probes, its voltage measured via the two internal probes and the resistance calculated with basic algorithm.

3.2.4 Wafer type and orientation

The periodic arrangements of the silicon atoms form a lattice. Each unit cell is defined by three vector axis. Using Miller indices, a plane is defined as either <100>, <110> or <111>. Different orientations yield different etch profiles. In this project, a wafer with <100> orientation is selected. In the <100> oriented wafer, truncated pyramids or truncated v-grooves deepen but do not widen. So, no undercuts will be formed.

The etch stop at the <111> sidewall's intersect is 0.7 times the mask opening.

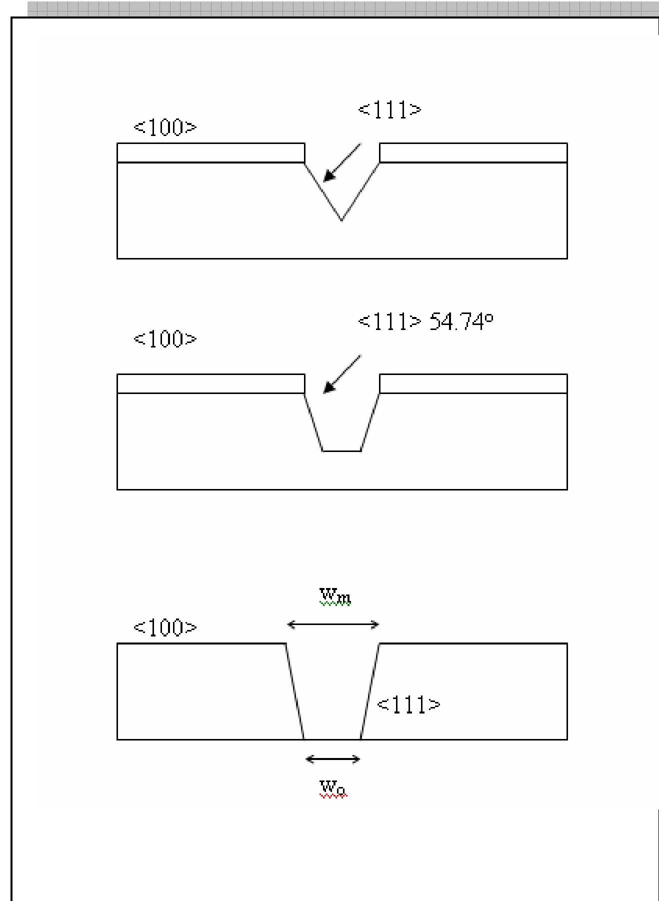


Figure 3.5: Etch profile on <100> oriented wafers

3.3 Photolitography

This is a technique used for pattern transfer. Several steps are involved in this process: Photo resist spin coating, soft bake, UV exposure, hard bake, develop and visual inspections. Normally, a vapour prime bake is done to drive out any moisture absorbed into the wafer. This promotes better adhesion of photoresist on the wafer surface. HMDS (Hexamethyldisilazane) should be spin coated on the wafer to promote resist adhesion. But due to limitations within the facility, this step is inevitably left out.

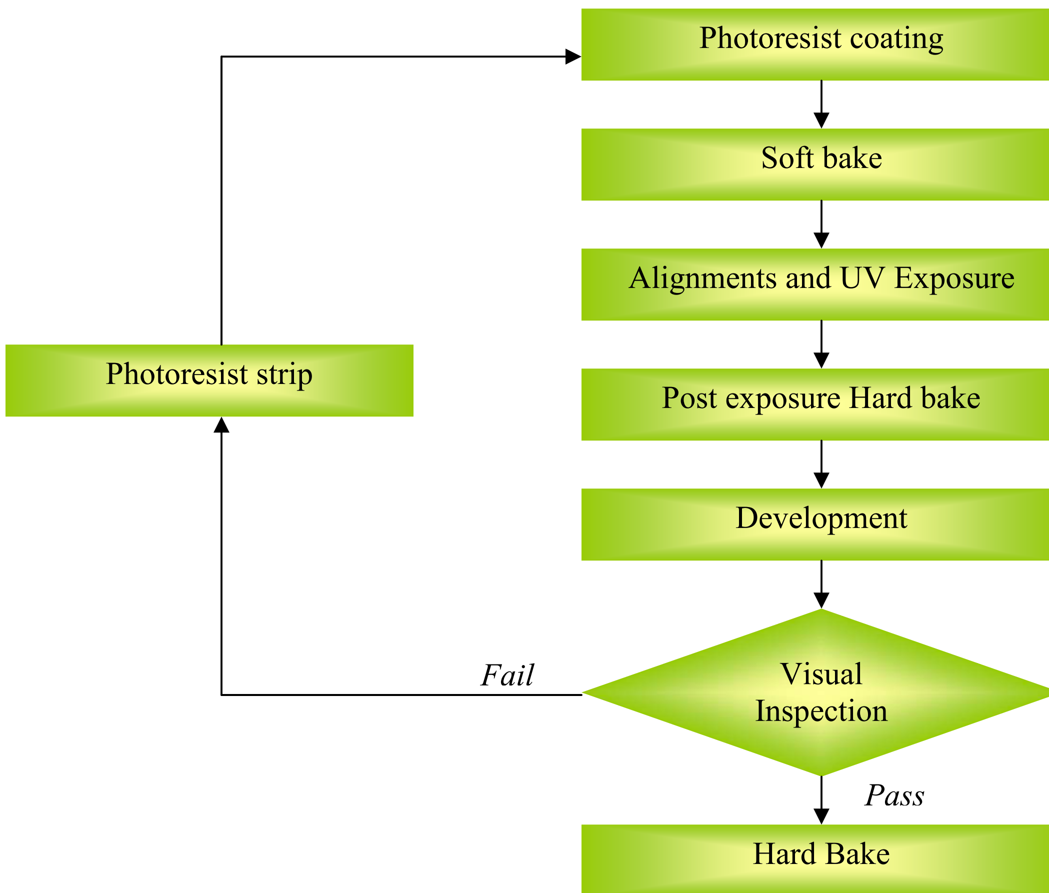


Figure 3.5: Photolitography Process Flow

3.3.1 Photoresist defined

Photo resist is a photo sensitive chemical used to hold a pattern. It is made up of polymers (resin based), sensitizer and a casting solvent. During UV radiation, the polymer changes structure. The solvent contributes to its liquefied properties to assist application. The sensitizers control the photochemical reactions in the polymeric phase. Solvents and other potential additives do not interfere in the photochemical reaction.

3.3.2 Spin Coating

This method is used to dispense the viscous solution of the polymer (Photoresist) onto the wafer lying on a wafer platen. The wafer is held securely by a Teflon vacuum chuck.The wafer is then spun at high speed between 500-6000rpm. The speed and ramp up parameters are determined by the thickness of coating and its viscosity. The high speed generates a centrifugal force that causes the solution to flow to the sides, forming a uniformly thick coating. The thickness of the resist can be varied depending on the chemical resistance and the fineness of lines and space to be resolved.

3.3.3 Soft Bake

This is done to remove the part of the solvent in the photoresist, remove stress and to promote adhesion of the resist on the silicon wafer. Failure of doing this may cause blurred pattern images as the resist is still in fluidic form and flows. In this project, the optimum soft bake parameters would be 90°C for 90 seconds.

3.3.3 Exposure (UV Radiation)

The photoresist coated wafer is then exposed to UV radiation with masks as stencils. The mask must be precisely aligned to wafer. The alignment technique must be capable of precise super imposition. A UV lamp is used as the source of illumination. It delivers light in predetermined intensity, directionality, spectral effects and uniformity. Light with smaller wavelengths are better as the diffract less. During exposure, exposed resist is rendered transparent to incoming wavelength. The photons will either break or polymerize the photosensitive substance in the photoresist. The exposure time is

influenced by the absorbency of the resist. Better absorbency, requires shorter the exposure time.

3.3.5 Development

This process involves the immersion of the exposed wafer in s developer bath. This process transforms the latent resist image formed during exposure into a relief image that will be used as a mask for further subtraction and additive steps. The developer selectively dissolves the resist.

3.3.6 Hard Bake

This process is to remove residual solvents and anneal the resist film to promote interfacial adhesion of the resist. This subsequently hardens the resist. This improved hardness increases resistance for consequent etch processes. The major limitation for heat application is excessive flow or melt that degrades the wall and angle profiles. It also makes it difficult to remove the resist.

3.4 Reactive Ion Etch (RIE)

This process is carried out to make trenches on the wafer as channels for fluid and aluminium electrodes. The etching process is anisotropic in nature and utilizes the billiard-ball effect. Inert ions are used to bombard the area that has to be etched. This causes breakage and ballistic material ejection.

The kinetic energy of the ions dictates the event that takes place; physisorption, surface damage, substrate heating, reflection, sputtering and ion implantation. At low kinetic energies, the ions are reflected. At higher energies, implantation occurs. Approximately 4-10eV is used for surface damaging and migration.

The ions impinge on the substrate in a direction normal to the substrate. These impinging ions erode and sputter etches the surface by momentum transfer. The advantage of dry etch is that it has high fidelity of mask pattern transfer with minimal distortions to critical dimensions. It entails directional anisotropy where no under cuts occur. Anisotropy is controlled by plasma conditions and it is only possible as long as the dimensions of surface topography structures are small compared with thickness of sheath between bulk plasma and etched surface.

3.5 Thermal Oxidation

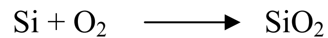
This process is necessary for growing a layer of silicon dioxide at a predetermined temperature. Thermally grown silicon is compressed because of molecular volume mismatch and thermal expansion differences. An oxide thickness above 1μm will cause bowing on wafer.

Wet oxidation has faster growth rate compared to dry oxidation. In this process, oxygen that is saturated with water molecules is used instead of dry oxygen. The water vapour is supplied from a boiler system that vaporises water to steam which is then channelled through a tube into the furnace's chamber. The reaction produces silicon dioxide and releases hydrogen gas as by product. The faster growth rate of wet oxidation is attributed to water characteristics. It has better permeability through silicon dioxide then oxygen. However, some trapped hydrogen molecules in the solid silicon dioxide makes the layer less dense compared to oxide grown in dry oxidation. The quick growth reduces compressive pressure on the wafer. The fast action leaves dangling bonds on silicon interface producing quantum states were electrons allow current to leak along the

interface. However, wet oxide has low density and low dielectric strength. This could be decreased by adding some halogens like chlorine. These elements add on to the dielectric breakdown strength and the threshold voltage. But too much of it may cause pits to form on the oxide.

In this project, the SiO_2 layer acts as the barrier between the aluminium electrodes and fluid channels.

The reaction takes place according to the following chemical equation:



$$Si + O_2 \longrightarrow SiO_2$$

3.6 Physical Vapour Deposition

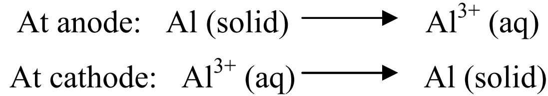
This is done to deposit aluminium. Aluminium is heated to its melting point rapidly. The aluminium atoms move trajectory and is deposited on the wafer. A very thin layer is deposited. This layer is then patterned and used for interconnections. In this project however, it is used as mask for Reactive Ion Etch.

3.7 Electroplating

This is an application of electrochemistry, where the wafer is coated with aluminium to the desired thickness. This process requires the use electrolyte, anode (sacrificial electrode), substrate (as cathode) and power supply. In this project, 2 mol aluminium nitrate aqueous is used. Aluminium is used as anode whereas the substrate becomes the cathode.

Aluminium from the anode which is positively charged oxidizes to aluminium ions (Al^{3+}) that dissolve into the aqueous. Aluminium ions (Al^{3+}) in the electrolyte will be

attracted to the negatively charged substrate, and reduces to aluminium solids, thus creating a deposition or plating. Electrons flow through the external power supply connections. This is the principle of electrochemistry, a REDOX process with the aid of electricity.


At anode: Al (solid) $\longrightarrow$ Al^{3+} (aq)

At cathode: Al^{3+} (aq) $\longrightarrow$ Al (solid)

The quality of deposition depends on the drift current. High current produces uneven and porous deposition. A lower drift current produces better deposition but may take a longer time.

3.8 Anodic Bonding

This is a method to bond two wafers together. Several other methods that can be employed are Fusion bonding and Glass-frit bonding. In this project, the fluid channels in the device must be fully enclosed to ensure that the fluid motion via capillary action takes place. The bond has to be tightly sealed to prevent fluid leakages that will eventually cause shorts and be detrimental in the electrical characteristics of the final product.

Anodic bonding is similar to electrostatic bonding. To bond two wafers or wafer and glass, elevated voltages are used, up to 1000 volts. The high electric fields in the entire area create a strong electrostatic force, pulling the two surfaces together. During boding, oxygen from the glass is transported to the glass-silicon interface. Because of the movement, SiO_2 is formed which in turn creates a permanent bond. During the process, the electric filed is high enough to allow a drift of oxygen to the positive electrode (Si), which the reacts with silicon (wafer) and creates a Si-O bond.

3.9 Process Flow for Device Fabrication

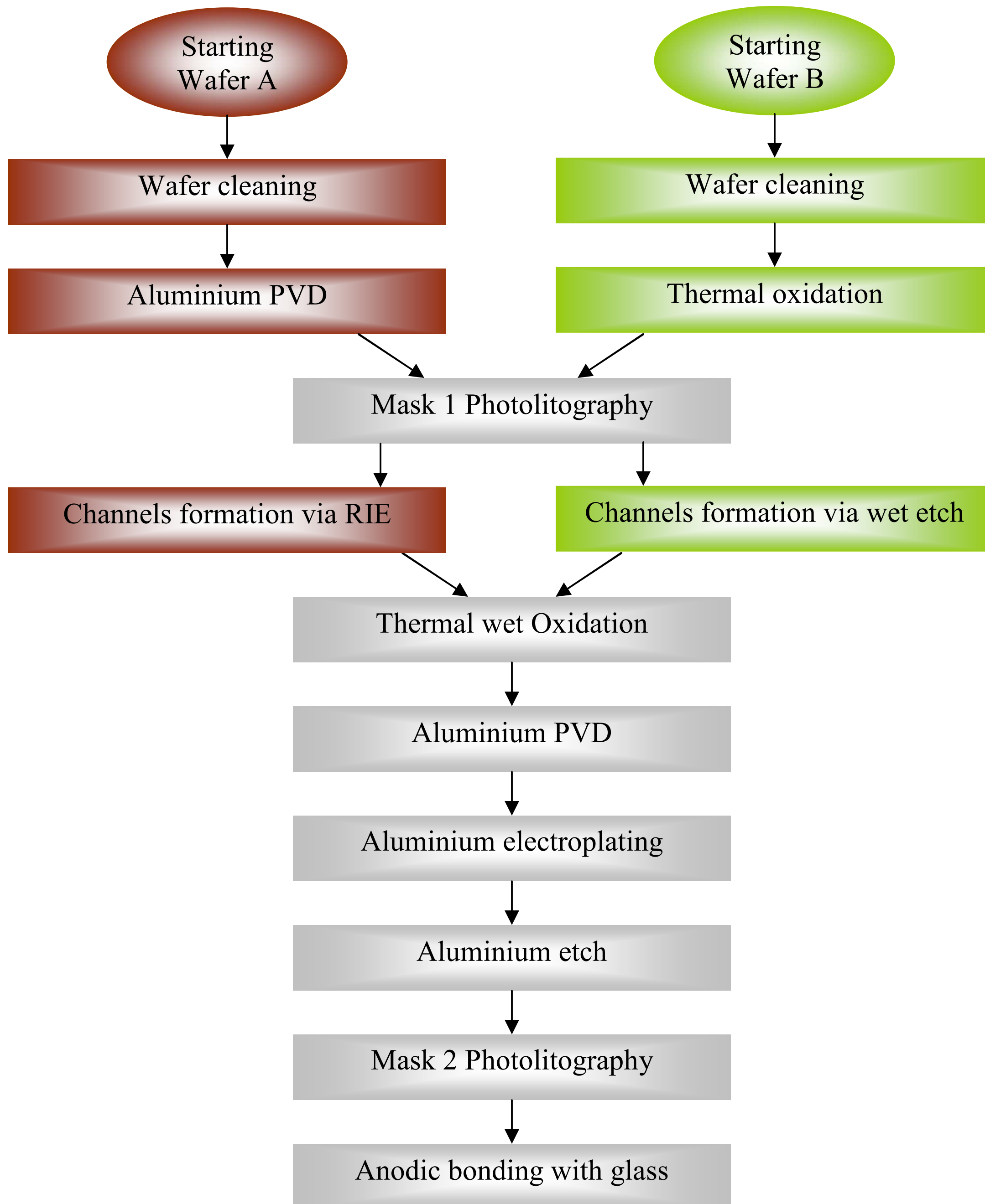
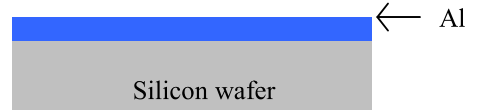


Figure 3.6: Process Flow for Fabrication of Device

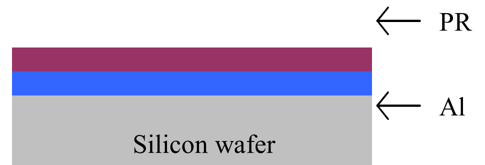
Fabrication Process Flow

1. **Starting wafer:** cleaned in BOE and pre-fabrication measurements are made.

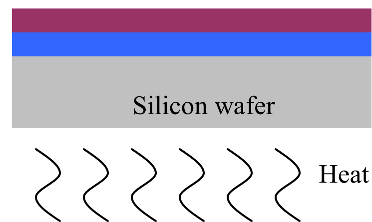
2. **Aluminium physical vapour deposition:** A thick layer of Aluminium deposited is deposited as mask for RIE



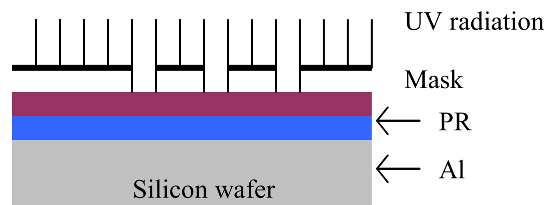
3. **Photoresist spin coating:**
   - ✓ 5 seconds: 700 rpm
   - ✓ 20 seconds: 3000 rpm
   - ✓ 5 seconds: 0 rpm



1. **Soft bake:** this is done to reduce part of the solvent in the photoresist. This is done at 90^{0}Celsius for 90seconds. The PR which is in fluidic state will cause blurry images.

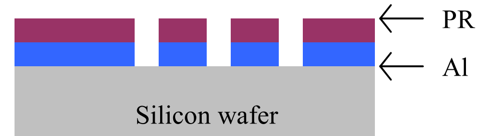


2. **Mask 1 Alignment, UV Exposure and Development** Mask 1 contains the pattern for electrode and fluid channels. The image is transferred by exposure to UV radiation for 100 seconds.



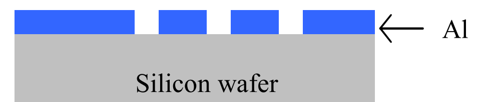
3. **Aluminium Etch:**

   With PR as the sacrificial mask, aluminium is etched in Aluminium etch.



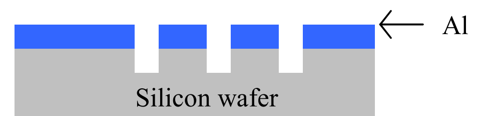
4. **Photoresist Strip:**

   The resist is stripped using acetone in the spinner.



5. **Silicon etch using RIE/ KOH:**

   The silicon layer is etched to produces trenches that will be come channels for fluid and electrodes.



6. **Aluminium strip:**

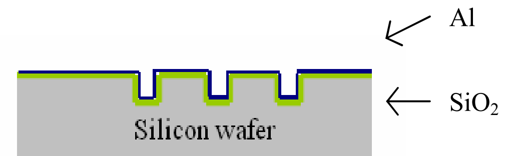
   The aluminium layer previously used as mask is no longer necessary. It is etched away in Aluminium etch

7. **Thermal Oxidation:**

   This process grows silicon dioxide on the surface of the wafer. It will act as the insulation material at the interface of a electrode and fluid. Thermal oxidation is done in the furnace at 1000^0C for 17 hours.

8. **Aluminium Physical Vapour Deposition**

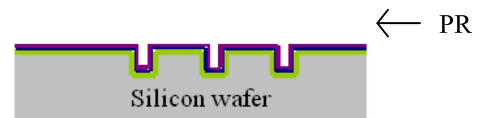
A thin layer of aluminium is deposited on the wafer via PVD. This aluminium will act as the seed layer for aluminium electroplating.



9. **PR coating**

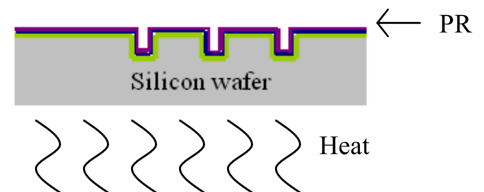
A layer of photoresist is spin coated onto the wafer. The following parameters were used:

- ✓ 5 seconds: 700 rpm
- ✓ 20 seconds: 3000 rpm
- ✓ 5 seconds: 0 rpm



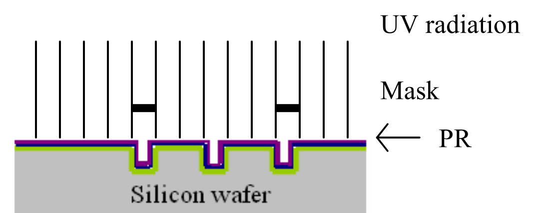
10. **Soft Bake**

This is done to reduce part of the solvent in the photoresist. This is done at 90^0Celsius for 90seconds.The PR which is in fluidic state will cause blurry images



11. **Mask 2 Alignment, UV Exposure and development**

Mask 2 carries the pattern for aluminium seed in the electrode areas. It prevents photo-solubalization from taking place in those areas. This process is critical as the alignment must meet Mask 1's alignment.



The following parameters were used for this process:

- ✓ Light intensity:
- ✓ Bla
- ✓ Bla
- ✓

12. Aluminium Etch:

The wafer is immersed into Aluminium etch to remove unwanted aluminium but retaining it at the electrode channels.

13. Photoresist Strip

The resist is stripped using acetone in the spinner

14. Aluminium electroplating

This process is necessary to grow 10 microns of aluminium which will serve as electrodes.

3.10 Equipments and Consumables

The following were the equipments used to fabricate the microfluidic capacitor

- ✓ Wet Bench
- ✓ RIE
- ✓ Spin coater
- ✓ Hot Plate
- ✓ Fume hood
- ✓ Mask aligner and UV radiator
- ✓ PNT Conduction gauge
- ✓ Spectrophotometer
- ✓ Single electron Microscope
- ✓ 4 Point Probe
- ✓ High Power Microscope
- ✓ PVD
- ✓ Wet Oxidation Furnace

The following are the consumables used

- ✓ Positive photoresist
- ✓ Aluminium
- ✓ Pure Oxygen gas supply
- ✓ Pure nitrogen gas supply
- ✓ De-ionized water
- ✓ Acetone
- ✓ Aluminium nitride aqeues
- ✓ Buffered oxide etch
- ✓ Aluminium etch
- ✓ Developer