GATE OXIDE INTEGRITY (GOI) CHARACTERIZATION FOR DEEP SUBMICRON CMOS DEVICE

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APPROVAL AND DECLARATION SHEET

This project report titled Gate Oxide Integrity (GOI) Characterization for Deep Submicron CMOS Device was prepared and submitted by Norain Bt. Mohd. Saad (Matrix Number: 031010364) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Microelectronic Engineering) in Universiti Malaysia Perlis (UniMAP).

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PENCIRIAN INTEGRITI GET OKSIDA (GOI) UNTUK PERANTI CMOS BERSKALA MIKRON

ABSTRAK

Sejak era (Integrasi Berskala Besar) VLSI penskalaan ketebalan get oksida merupakan asset dalam pengawalan impak saluran pendek peranti seperti mana dimensi get MOS yang telah mengalami penskalaan kecil sehingga 0.1um panjang saluran. Projek ini bertujuan untuk mengkaji hubungan antara fenomena kerosakkan get oksida dan impak atau kesan yang berkaitan dengan saluran pendek. Penekanan yang lebih diberikan kepada kemasukkan pembawa yang berkaitan dengan kemerosotan oksida yakni penerowongan electron Fowler Nodheim (F-N) kerana fenomena tersebut merupakan isu penting yang berkaitan dengan ketebalan get oksida yang agak nipis. Pencirian piawai untuk kerosakkan get oksida seperti ujian voltan tanjakan dan pengukuran arus dasar dilakukan dengan mengunakan struktur ujian kapasitor MOS yang berlainan saiz .Di dapati, penghasilan cas positif dan mekanisme perangkap merupakan faktor atau punca utama yang menyebabkan kerosakkan intrinsic get oksida. Selain itu,kemusnahan kekisi electron Wolter juga dipercayai sebagai salah satu faktor yang turut menyumbang ke arah kerosakkan get oksida. Namun demikian, ujian selanjutnya seperti ujian kerosakkan penebat berkadar dengan masa (TDDB) harus di jalankan. Ujian diperlukan untuk mengkaji adan mengesahkan hubungan antara kemusnahan kekisi electron Wolter dan kerosakkan get oksida.

GATE OXIDE INTEGRITY (GOI) CHARACTERIZATION FOR DEEP SUBMICRON CMOS DEVICE

ABSTRACT

Since the early days of Very Large Scale Integration (VLSI) era, the scaling of gate oxide thickness has been instrumental in controlling the short channel related effects in state-of-the-art device structure, as MOS gate dimensions have been scaled-down dramatically to a present day size of sub-0.1um channel length. This project studied the relationship between the gate oxide breakdowns phenomena with short channel related effects. Special attention was given to the carrier injections related oxide degradation which is Fowler-Nordheim (F-N) Tunneling, since this phenomenon was becoming profoundly important in ultra-thin gate oxide thickness. Standard gate oxide breakdown characterizations such as V-ramp test and substrate current measurement have been performed on MOS capacitor test structure of different sizes. Holes generation and trap mechanism is found to be one of the main cause for the intrinsic gate oxide breakdown. Other mechanism such as Wolter’s electron lattice damage might also be of a possible candidate, however further characterization such as Time Dependent Dielectric Breakdown (TDDB) Test is required to establish the relationship.

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LIST OF ABBREVIATIONS

AHI	Anode Hole Injection
API	Anti Punch through Implant
AR	Auger Recombination
BTBII	Band To Band Impact Ionization
CHE	Channel Hot Electron
CMOS	Complementary Metal Oxide Silicon
DAHC	Drain Avalanche Hot Carriers
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
FET	Field Effect Transistor
FN	Fowler Nodheim
HR	Hydrogen Release
IC	Integrated Circuit
JEDEC	Joint Electron Device Electronic Council
LDD	Lightly Doped Drain
LOCOS	Local Isolation Of Silicon
MOS-C	Metal Oxide Silicon Capacitor
MOSFET	Metal Oxide Silicon Field Effect Transistor
Qp	Hole-charge-to-breakdown
SGHE	Secondarily Generated Hot Electrons
SHE	Substrate Hot Electron
SMU	Source Measure Units
STI	Shallow Trench Isolation
T_{bd}	Time to breakdown
ULSI	Ultra Large Scale Integration
V-Ramp	Voltage ramp