TEMPERATURE CYCLING RELIABILITY TEST FOR A BALL GRID ARRAY (BGA) PACKAGE USING FINITE ELEMENT ANALYSIS (FEA)

by

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LIST OF ABBREVIATIONS

APDL	ANSYS™ Parametric Design Language and Macros
BGA	Ball Grid Array
CCD	Central Composite Design
CTE	Coefficient of Thermal Expansion
DFR	Design for Reliability
DIE	Die Thickness
DOE	Design of Experiment
FEA	Finite Element Analysis
GUI	Graphical User Interface
HAST	Highly Accelerated Temperature and Humidity Stress Test
JEDEC	Joint Electron Device Engineering Council
MLD	Mould Compound Thickness
MTTF	Mean Time to Failure
PCB	Printed Circuited Board
PDS	Probabilistic Design System
RSM	Response Surface Method
SFAIL	Solder Joint Fatigue Life
SSE	Sum of Squares of the Errors
SSR	Regression Sum of Squares
SST	Total Sum of Squares
STD	Solder Joint Standoff Height

TK	PCB Core Thickness
YOU	PCB Core-in-Plane Young's Modulus

LIST OF SYMBOLS

λ	Failure Rate Function
β	The Mean of Exponential Distribution
σ	Shape Factor
μ	The Log Mean
α	The Scale Parameter
$\Gamma(x)$	The Gamma Function
$\dot{\gamma}$	The Total Shear Strain
$\dot{\gamma}_e$	The Elastic Shear Strain Component
$\dot{\gamma}_p$	The Plastic Strain Component
$\dot{\gamma}_c$	The Creep Strain Component
N_f	The Mean Cycles to Failure
C	The Fatigue Ductility Coefficient
$d\varepsilon_{eq}^{pl}$	The Stabilized Incremental Equivalent Plastic Strain
$\Delta\varepsilon_{eq}^{pl}$	The Summation of the Stabilized Incremental Equivalent Plastic Strain
T_m	Melting Temperature
$\frac{d\varepsilon_S}{dt}$	The Steady State Strain Rate
k	Boltzmann's Constant
T	The Absolute Temperature

σ	The Applied Stress
Q_a	The Apparent Activation Energy
n	The Stress Exponent
α	The Stress Level at Which the Power Law Dependence Breaks Down
ε_C	The Creep Strain
ε_T	Transient Creep Strain
B	The Transient Creep Coefficient
$\frac{d\varepsilon_C}{dt}$	Instantaneous Creep Rate
ε_p	Time-Independent Plastic Strain
G	Shear Modulus
ε_{in}	Total Inelastic Strain Energy
ε_p	Time Independent Plastic Strain
ε_c	Time Dependent Creep Strain
ΔW_{ave}	The Average Viscoplastic Strain Energy Density Accumulated per Cycle
V	The Volume of Each Element
N_0	The Number of Cycles to Crack Initiation
$\frac{da}{dN}$	The Crack Growth Rate per Thermal Cycle
α	The Characteristic Solder Joint Fatigue Life
a	The Total Distance the Crack Travels
S_0	Initial Value of Deformation Resistance
Q/R	Activation Energy / Boltzmann's Constant

A	Pre-Exponential Factor
ζ	Multiplier of Stress
m	Strain Rate Sensitivity of Stress
h_0	Hardening Constant
s^	Coefficient of Deformation Resistance Saturation Value
n	Deformation Resistance Value
a	Strain Rate Sensitivity of Hardening

ABSTRAK

UJIAN KEBOLEHARAPAN SUHU BERKITAR BAGI PAKEJ BEBOLA TATASUSUNAN GRID (BGA) MENGGUNAKAN ANALISA UNSUR TERHINGGA (FEA)

Ujian suhu berkitar adalah salah satu daripada ujian kebolehharapan yang selalunya digunakan untuk menilai kebolehharapan sambungan pateri di dalam pembungkusan mikroelektronik. Tujuan ujian suhu berkitar adalah untuk mencirikan mekanisme kegagalan mekanik haba ke atas pembungkusan mikroelektronik. Penyelidikan ini menggunakan keupayaan komputer untuk melakukan ujian suhu berkitar melalui analisa unsur terhingga. Analisa unsur terhingga untuk ujian suhu berkitar dijalankan dengan menggunakan perisian unsur terhingga ANSYS™. Satu per empat model pakej bebola tatasusunan grid (BGA) dibina secara berparameter menggunakan APDL (bahasa dan makro rekabentuk berparameter ANSYS™). Dua jenis analisa digunakan untuk menilai keupayaan keboleharapan sambungan pateri ke atas pakej BGA, iaitu analisa secara fizik dan analisa secara statistik. Model lesu berdasarkan tenaga Darveaux digunakan sebagai persamaan juzuk untuk pateri. Keadaan suhu berkitar G berdasarkan piawaian JEDEC JESD22-A104 digunakan di dalam analisa unsur terhingga. Kesan perubahan suhu berkitar dikaji dengan menggunakan beberapa nilai berbeza bagi masa inap dan masa tanjakan. Dua kaedah rekabentuk ujikaji statistik iaitu rekabentuk komposit berpusat (CCD) dan rekabentuk matriks Box-Behnken digunakan untuk memperolehi faktor terpenting daripada beberapa pembolehubah rekabentuk seperti ketinggian sambungan pateri, ketebalan papan litar tercetak (PCB), modulus Young teras di dalam satah PCB, pekali pengembangan haba (CTE) teras di dalam satah PCB, ketebalan *die*, dan ketebalan *mold*. Proses pengoptimuman menggunakan kaedah permukaan sambutan (RSM) digunakan untuk mengesan pembolehubah atau faktor yang mempunyai kesan langsung ke atas kegagalan pembungkusan mikroelektronik dan juga interaksi antara faktor. Simulasi Monte Carlo digunakan untuk melakukan penilaian kewarakan ke atas keputusan yang diperolehi melalui pengoptimuman berdasarkan rekabentuk komposit berpusat (CCD) dan rekabentuk matriks Box-Behnken. Daripada pemerhatian didapati bahawa perubahan pada masa tanjakan menghasilkan kesan langsung ke atas hayat lesu pateri berbanding daripada perubahan pada masa inap. Walaubagaimanpun, masa inap pada suhu tinggi memberikan kesan yang boleh diabaikan ke atas hayat lesu sambungan pateri. Ketebalan *mold* didapati mempunyai kesan langsung paling tinggi terhadap perubahan keupayaan keboleharapan pateri (lebih daripada 50%) daripada faktor-faktor yang lain. Selain daripada kesan individu bagi setiap faktor, interaksi antara faktor juga dapat mengubah keupayaan keboleharapan pateri. RSM berdasarkan kepada rekabentuk matriks Box-Behnken menghasilkan hayat lesu ciri sambungan pateri paling tinggi iaitu bersamaan dengan 2861 kitaran atau 44.1% peningkatan daripada nilai awal set rekabentuk. RSM berdasarkan kepada rekabentuk CCD menghasilkan pengiraan kebagusan padanan yang terbaik. Oleh itu RSM berdasarkan kepada CCD mempunyai ketepatan yang terbaik dalam mewakili titik sampel terhadap permukaan sambutan.

ABSTRACT

Thermal cycling test is one of the reliability test that has been used to evaluate the reliability of the solder joint interconnect in ball grid array (BGA) package. The purpose of thermal cycling test is to characterize thermomechanical failure mechanism on microelectronics package. This research utilizes the computer capability to run the thermal cycling test by using finite element analysis (FEA). FEA of thermal cycling test is done by using ANSYS™ finite element software. Quarter symmetry BGA package model is built parametrically by using APDL (ANSYS™ Parametric Design Language and Macros). Two types of analyses are used to evaluate the reliability performance of solder joints in BGA package, namely the physics based analysis and the statistical based analysis. Darveaux's energy based fatigue model is used as the constitutive equation for solder. One of the temperature cycling conditions namely, G based on JEDEC JESD22-A104 standard is used throughout the finite element analysis. The effect of different temperature cycling condition is studied by applying different value of dwell times and ramp rates. Two screening design methods namely, Central Composite Design (CCD) and Box-Behnken Matrix Design method are used to isolate the most important factors amongst six design variables such as solder joint standoff height, printed circuited board (PCB) core thickness, PCB core-in-plane Young's Modulus, PCB core-in-plane coefficient of thermal expansion (CTE), die thickness and mold compound thickness. The optimization process is carried out using response surface methodology (RSM) to predict appropriate variables or factors that have a significant influence on BGA package failure and their interactions. Monte Carlo simulations are used to validate the randomness of the results obtained through CCD and Box-Behnken matrix design based optimization methods. It is observed that changes in ramp rate produce significant effect in solder joint fatigue life rather than changes in dwell time, but the dwell time at high temperature (high dwell) has a negligible contribution to solder joint fatigue life. It is also found that the thickness of the mold has a significant effect on the performance of the solder joint reliability (more than 50 %) as compared to that from other factors. Besides the effect of individual factor, the interaction among factors also changes the solder joint reliability. RSM based on Box-Behnken Matrix design offers the highest characteristic solder joint fatigue life with a value of 2861 cycles or 41.1% enhancement from the initial design set. RSM based on CCD offers the best goodness-of-fit measures over RSM based on Box-Behnken Matrix design. These results show that RSM based on CCD has better accuracy in representing the sample points on response surface.

CHAPTER 1

INTRODUCTION

1.1 Microelectronics Packaging Technology Trends

Microelectronics packaging is one of the major fields in microelectronics engineering. The functions of a microelectronics package are to protect, power, and cool the microelectronic chips or components and provide electrical and mechanical connection between microelectronics parts and outside world (Tummala, 2001). The technology and business trend of microelectronics such as further miniaturization, high performance electronic product, increasing level of technology and function integration, cost reduction and also short time to market lead to increase chances of failures and design complexity of microelectronics packaging (figure 1-1).

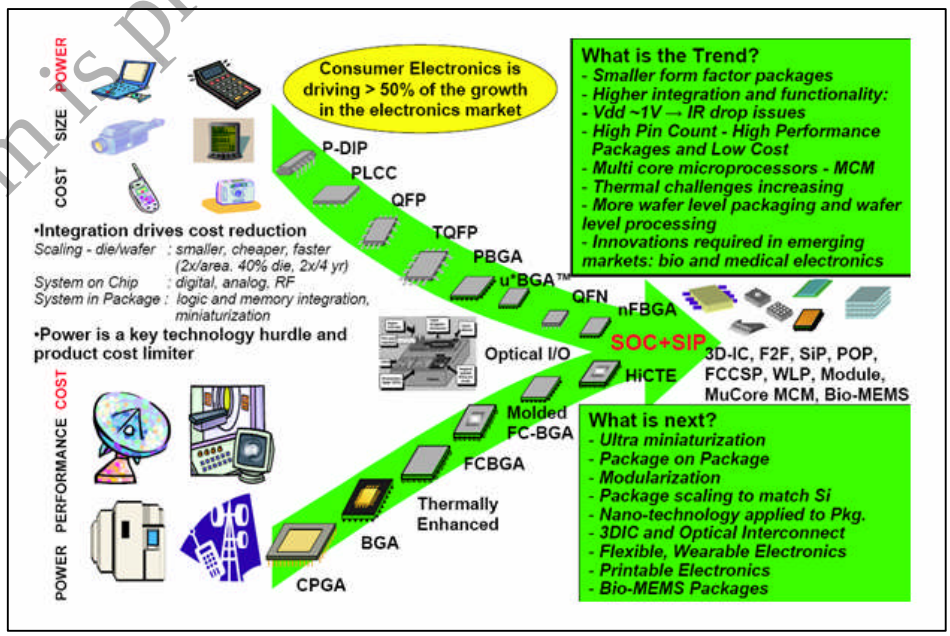

Figure 1-1: Microelectronics Packaging Technology Trend (Bolanos, 2006)

Performing reliability tests is important before any microelectronics product goes to the market. The tests are becoming more challenging as more complex processes and products must be developed in shorter time scale. Furthermore, the next generation of microelectronics packages is expected to perform with ten time higher reliability than today's packages (Tummala, 2001). The packages should perform under various stress environments, with temperature ranging from -60 °C to 175 °C for the automotive and aerospace industries, and -50 °C to 150 °C for the telecommunication, consumer and computer industries. Nowadays, product qualification requires many reliability tests such as thermal shock, temperature cycling, highly accelerated temperature and humidity stress test (HAST), to name a few. All of these tests require expensive equipment and long testing time and this in turn will add to the total cost of the packages.

To reduce cost and process or product development time and to improve reliability performance, integrated design for reliability (DFR) at the earlier stage of development has become a vital practice. DFR process can be done by utilizing the capability of commercial finite element software. By utilizing the computational capability of computer, DFR can produce reliability test results faster than the actual reliability test. This will help in reducing the time to market the product and also to make sure that reliable product is produced before entering the market.

Thermal cycling test is one of the reliability tests that has been used to evaluate the reliability of the solder joint interconnect in microelectronics package. Solder joint fatigue crack failure caused by thermomechanical mechanism is one of the major failures in microelectronics package. The purpose of thermal cycling test is to characterize thermomechanical failure mechanism on microelectronics package. Finite element

software is used to run the thermal cycling test virtually to evaluate the reliability of the solder joint. Solder joint reliability using finite element analysis is evaluated on the basis of physical analysis and statistical analysis. Physical analysis is used to analyze the effect of several factors such as component geometry, material properties and loading conditions on the performance of solder joint reliability. The statistical analysis is used to find the critical factors and to see the interaction among the factors affecting the performance of solder joint reliability.

1.2 Problem Statement

Solder joint fatigue crack failure is one of the major reliability issues in microelectronics package. The evaluation of solder joint reliability by using thermal cycling test requires a lot of time and very costly. To reduce cost and time consumption of reliability test, finite element analysis (FEA) is usually used to run an actual reliability test virtually. In this present analysis, commercial finite element software ANSYS™ is used to run thermal cycling test on a BGA package to evaluate the reliability of solder joint. Solder joint reliability using finite element analysis is evaluated on the basis of physical analysis and statistical analysis which provide a more comprehensive and in-depth results compared to the results obtained through an actual thermal cycling test.

1.3 Objectives

The objectives of this research are:

- To extend the work of Hossain et al. (2007) by adding two additional design variables (mold compound thickness and die thickness) and using a different type of screening design (Box-Behnken Matrix design).
    - To build a BGA package model for the finite element analysis using ANSYS™.
    - To understand the effects of several factors on solder joint reliability of BGA package through physical analysis and statistical analysis.
    - To find the value of inelastic strain energy and characteristic solder joint fatigue life.
    - To find the critical factors that affects the reliability performance of solder joint.
    - To find the optimum value of solder joint fatigue life.
    - To develop a solder joint reliability predictive equation based on response surface methodology.
- To analyze the effect of different temperature cycling loading condition (ramp rate and dwell time) on the characteristic solder joint fatigue life.

1.4 Thesis Outline

Chapter 2 outlines a literature review about basics of reliability, statistical experimental design, screening design, solder fatigue models, and optimization technique approaches. Chapter 3 explains the analysis to develop BGA package model in ANSYS™ finite element software and the procedure needed to run an optimization process in ANSYS™ built-in feature known as Probabilistic Design System (PDS). Chapter 4 describes and discusses the results obtained from the analysis. Chapter 5 provides the conclusions and suggestions for future work. Appendix A provides the APDL code used for finite element analysis in ANSYS™ and Appendix B includes the publication that has been published based on this present analysis.

1.5 Publication

Some of the results and discussions of this research presented in chapters 3 and 4 in this thesis have been published in the following scientific literature (Appendix B):

- Zulkifli, M. N., Jamal, Z., Quadir, G.A., and Hashim, U. (2008). Thermal Cycling Analysis of SnAgCu and SnPb Solder Joints Reliability. *Proceeding of Malaysian Technical Universities Conference on Engineering and Technology (MUCET) 2008,* 26-31.

CHAPTER 2

LITERATURE REVIEW

2.1 Reliability

The reliability of a packaged microelectronics system is defined as the probability that this system will be operational within acceptable limits for a given period of time (Tummala, 2001). Usually, the effect of microelectronics package reliability issues are often realized at the system level, but the actual failure mechanism occurs at the lowest hardware level. Therefore, in order to run reliability analysis on microelectronics packages, it will require a thorough understanding about failure modes and failure mechanisms relevant to microelectronics packaging.

The reliability of semiconductor packaging is always related on interconnection issues such as the reliability of solder joints. This is because most of the failure modes such as fatigue, creep, crack and voids often occur at the solder joints area (Li et al., 2007). In electronic assemblies, fatigue of solder joints is believed to play a major role in about 90 % of all structural and electrical failures (Tummala, 2001).

2.1.1 Temperature Cycling

To asses the reliability of microelectronic package, several reliability tests or accelerated tests are usually used in the industry. One of the reliability tests that has been used is thermal cycling test. Thermal cycling test is used to characterize thermomechanical

reliability issues in microelectronics package in order to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high and low extremes (JEDEC, 2000). The repeated temperature cycling produces stress that eventually causes solder joint fatigue crack failure because of the thermomechanically-induced strains and stresses generated at the solder joints. Figure 2-1 shows temperature cycle profile that is usually used in a thermal cycling test (JEDEC, 2000).

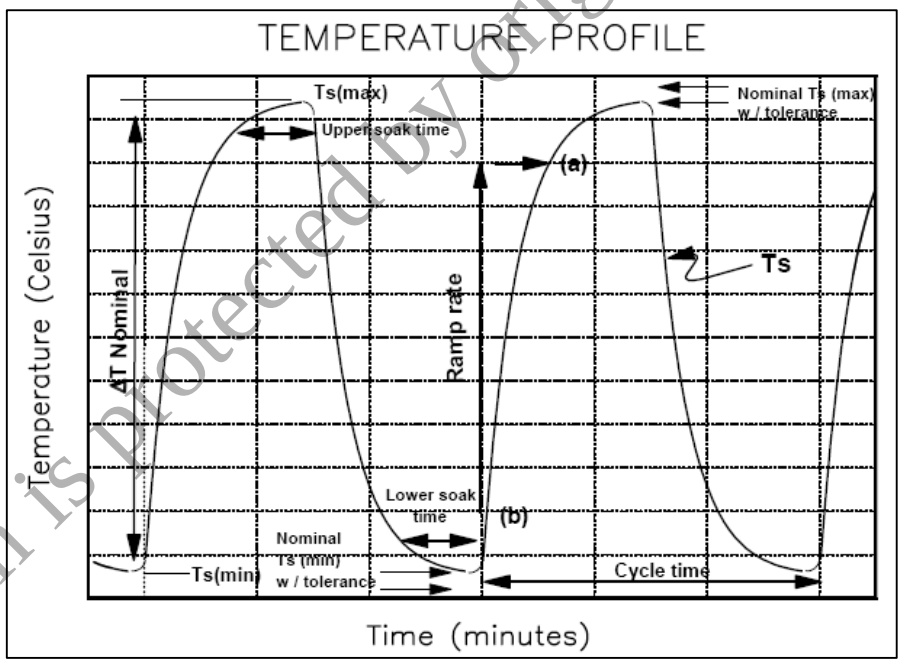

Figure 2-1: Temperature Cycle Profile

There are two types of thermal cycling tests that have been used in industry; thermal cycling and thermal shock tests. The major difference between these two tests is the physical chamber used for testing. Thermal shock test is conducted in two separate liquid thermal baths or two separate air chambers in which the tested components are