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SOI Single-Electron Transistors (SET) Design and Process Development

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***Abstract* - Single-electron transistor (SET) is attractive devices to use for large-scale integration. SET can be made very small, dissipate little power, and can measure quantities of charge much faster than MOSFETs. This makes SET would replace field-effect transistor (FET). In this paper, Electron Beam (E-Beam) GDS II Editor Software is utilized to design a mask for SOI SET fabrication. This system show promising result producing structure at nanometer scale node. Four masks step are involved namely source/drain & gate mask, Poly-Si gate electrode mask, contact mask, and metallization mask. SOI SET device design with a gate length and gate width of approximately 0.1µm and 0.02µm respectively is generated for fabrication process. In addition, the processes involve in SOI SET fabrication are also discussed.**

I. INTRODUCTION

Lithography is the process of transferring patterns from one medium to another medium. Other lithography techniques, which use different forms of radiation including extreme UV, x-ray, electron beams, and ion beams, to offer higher resolution, are growing importance [1]. In the semiconductor industry, electron beam lithography (EBL) has been routinely used to generate master masks and retackles from computer aided design (CAD) files [1]. These masks are usually used in optical projection printing to replicate the patterns on silicon wafers.

Electron Beam Lithography (EBL) is a specialized technique for creating the extremely fine patterns (much smaller than can be seen by the naked eye) required by the modern electronics industry for integrated circuits [2]. Because of its very short wavelength and reasonable energy density characteristics, e-beam lithography has the ability to fabricate patterns having nanometer feature sizes. In addition, EBL inherently has higher spatial resolution and wider process than optical lithography [3]. Therefore, EBL can also use the step and scan techniques to expose the electron-sensitive polymer resist on the wafer surface and transfer the pattern from the retackle to the resist.

In principle, SOI SET device fabrication consists of four masks such as source/drain & gate mask, Poly-Si gate electrode mask, contact mask, and metallization mask will be discussed in section II. The masks were designed using E-Beam GDS II Editor Software. This mask design include gate or channel length varied from 100nm, 200nm, 300nm, 400nm and 500nm; and channel width varied in the range of 20nm to 100nm. The device is created with varied dimensions for allowing us to observe the effect of size on device performance.

This present paper is organized as follows. We start with the SOI SET mask design in section II. In section III, we described the SOI SET process development. Finally, conclusion of our discussion is presented in section IV.

II. SOI SET MASK DESIGN

As been reported [4-5], we decided to fabricate SOI SET device based on four level mask steps. The four level mask steps of SOI SET was design with different gate length and gate width. These masks were designed using E-Beam GDS II Editor Software.

A. *E-Beam GDS II Editor Software*

Before reviewing the masks design of SOI SET, a few important aspects of E-Beam GDS II Editor Software should be addressed. The GDS II is by far the most stable, comprehensive and widely used format for lithography. This software is used for design of structures and proximity correction is shown in Figure 1.

Here is an overview of Desktop 1 in E-Beam GDS II Editor Software which is made for design of the pattern to be written. From Figure 1, at the top there is the menu bar with drop-down menus. The menus change depending on which window is active on the desktop. Below the drop-down menu bar there is a function-buttons bar. These also change depending on which window is active. The windows opened on this Desktop 1 are (starting at top, left):

1. The GDS II database selector, where you load a design and switch between structures showing within the design.
2. The Toolbox belonging to the GDS II viewer.
3. The Layer selector, where you decide what layers will be displayed.
4. The GDS II Viewer, i.e. a window showing your design in view-only mode.

1. The Working Area selector/edit window. It is possible to have several work areas saved with your GDS II database.

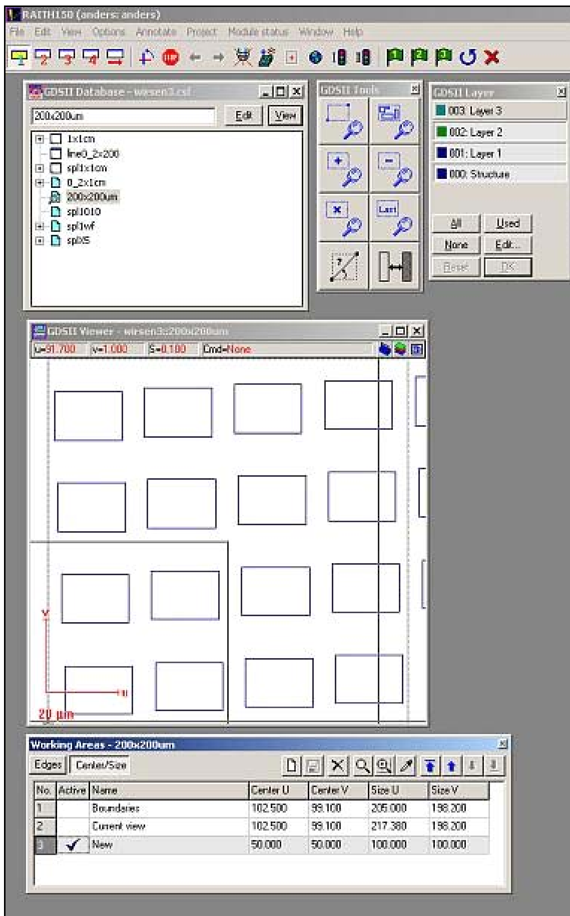


Figure 1. An overview of E-Beam GDS II Editor Software.

On the other hand, we can design the various pattern of SET if the Desktop 1 in E-Beam GDS II Editor Software is ready. The SET masks were designed using E-Beam GDS II Editor Software is shown in Figure 2. From Figure 2, the SET masks were designed in nanometer scale size. A source/ drain length and width are 500 nm while a gate length and width is 100 nm and 20 nm. The gate mask was designed with various gate length and gate width but for working at room temperature operation and low capacitance (1 aF) [6-8], a gate length and gate width of SET must be at 100 nm and 20 nm.

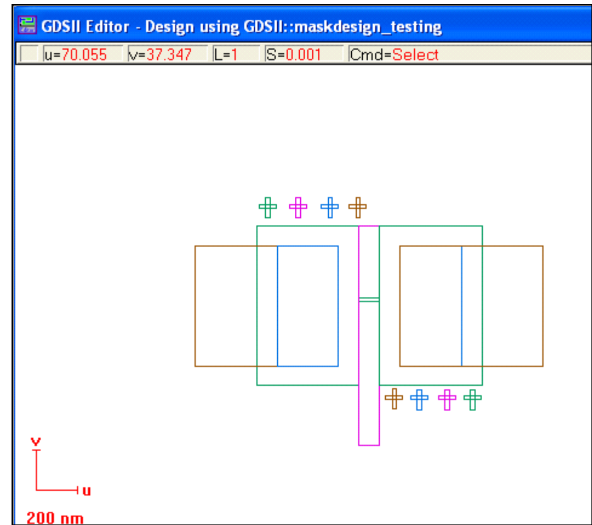
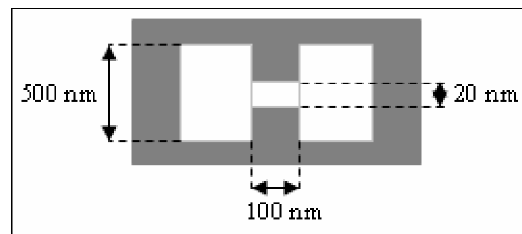


Figure 2. The SET masks design using E-Beam GDS II Editor Software.

In addition, the Poly-Si gate electrode mask length is 100 nm while their width is 700 nm. For contact mask, the length and width are 300 nm. The last mask for SET is metallization mask. The metallization mask length is 700 nm and the width is 400 nm. Other dimensions of this device are also varied including source/ drain size, gate length and width, contact size, and metallization area. The explanation of SET mask design will be discussed in section B.

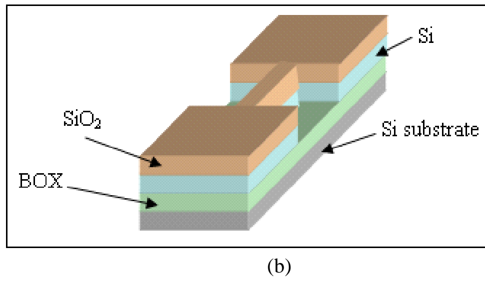
B. Mask Design

Under this study, a SOI SET device consists of four level mask steps. The mask set comprises the source/drain & gate mask, Poly-Si gate electrode mask, contact mask, and metallization mask. The SOI SET mask designed is started with the source/drain & gate mask as shown in Figure 3.



(a)

Figure 3 (a). The source/drain & gate mask.

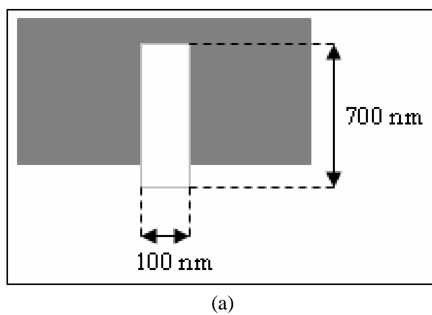


(b)

Figure 3 (b). Three-dimensional image of source/ drain and gate structure after lithography process.

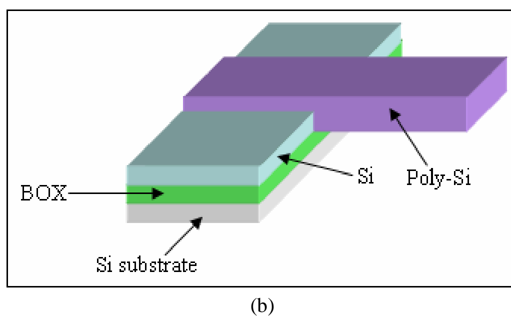
From Figure 3, the source/drain mask is used to control the heavily phosphorous doped and create source and drain region [5]. The spacing between the source and drain region is the gate or channel length. The gate mask is used to define the gate region. The gate length ranged from 100 nm to 500 nm and gate width varied in the range of 20 nm to 100 nm. In our research, we were designed the gate length is 100 nm and gate width is 20 nm for SOI SET device working at room temperature operation.

The second masks for this device is Poly-Silicon gate electrode mask. As shown in Figure 4, the mask is used to deposit Poly-Silicon on the wafer.



(a)

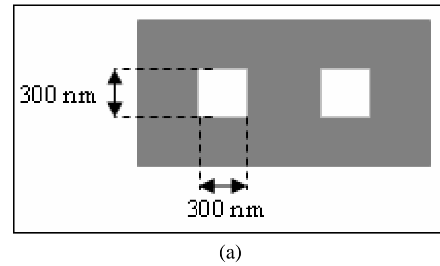
Figure 4 (a). Poly-Silicon gate electrode mask.



(b)

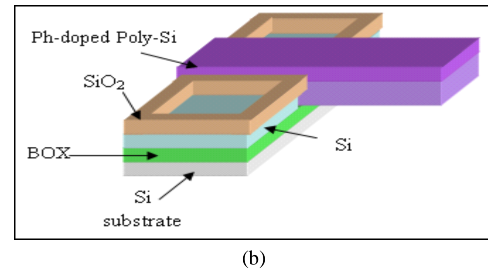
Figure 4 (b). Three-dimensional image of Poly-Si gate electrode structure after lithography process.

The third mask is contact mask (see Figure 5). This mask is used to define an opening to the source and drain so the metal lines in metallization process are connected to the source and drain.



(a)

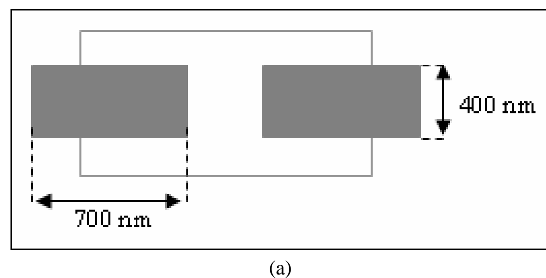
Figure 5 (a). Contact mask.



(b)

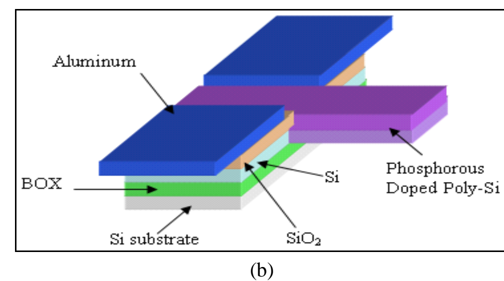
Figure 5 (b). Three-dimensional image of contact structure after lithography process.

Finally, the connection was done using metallization mask (Figure 6) for electrical characteristic. The Aluminum film on the wafer will be etched away by using metallization mask.



(a)

Figure 6 (a). Metallization mask.

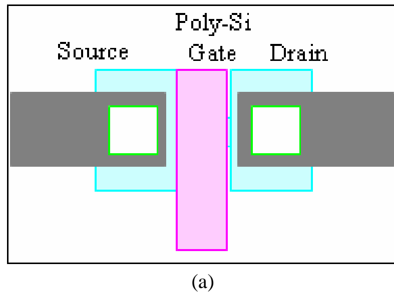


(b)

Figure 6 (b). Three-dimensional image of metallization structure after lithography process.

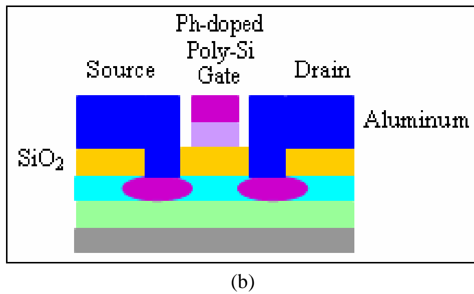
In principle, the layout of the masks set design is shown in Figure 7(a). This figure clearly shows a complete SOI SET device, which consists of a source and drain region, Poly-Silicon gate electrode, a contact window, and

metallization area. The cross-section of the device will determine which region that should be masked (Figure 7(b)).



(a)

Figure 7 (a). SOI SET device layout.



(b)

Figure 7 (b). The cross-section of SOI SET device.

III. SOI SET PROCESS FLOW DEVELOPMENT FOR FABRICATION

Before reviewing the specific methods of fabricating of SOI SET device, a few important aspects of SET fabrication should be addressed. One is island size reduction. In such a small Si island, the energy separation due to the quantum-size effect is expected to appear and relax the requirement for shrinking the island size [9]. Another point is the attachment of two tunnel junctions to such a small island, and with what material. Low tunnel resistance is preferable for achieving reasonable derivability, though is theoretically limited by quantum resistance, R_q. Lastly, there is control of the size and the position of Si islands with good reproducibility. From the view point of LSI application, the device fabrication method must have sufficiently good controllability and reproducibility.

In this experiment, the SOI wafer prepared from separation by implanted oxygen (SIMOX) [6-11] process will be used as the base material for the SOI SET fabrication. Silicon-on-insulator (SOI) technology has gained increasing acceptance in recent years as a technology for scaling conventional CMOS technology below the 10nm gate length node [12]. SOI technology has also proved promising in realizing SET structures with potential for room temperature operation. The SOI structure can remove the undesirable bulk effect of the Silicon (Si) wafer and is very effective for limiting the channel width. The structure of SOI wafer is shown in Figure 8.

Figure 8. Schematic structure of SOI.

The SOI wafer structure has several important advantages over CZ bulk or epitaxial starting wafer architectures. SOI wafers potentially offer "perfect" transistor isolation (lower leakage), tighter transistor packing density (higher transistor count), reduced parasitic drain capacitance (faster circuit performance and lower power consumption), and simplified processing relative to bulk or epitaxial silicon wafers [13].

In order to fabricate SOI SET, e-beam lithography combined with an image reversal process using inductive coupled plasma (ICP) etcher will be used. In principle, this fabrication consists of four major processes such as source/drain & gate formation, Poly-Si gate electrode formation, contact formation, and metallization.

The device characteristic will be measured by a precision semiconductor parameter analyzer which located in Failure Analysis Laboratory. In addition, scanning ion mass (SIM), scanning tunneling microscope (STM), tunneling electron microscope (TEM), scanning electron microscope (SEM) and other characterization tools will be utilize as well to characterize the device. The ten processing steps of SOI SET process flow that involve changes to the surface of the wafer are shown in Figure 9.

The SOI SET under study is fabricated on p-type silicon-on-insulator (SOI) wafers <100> with the resistivities of 1-20 Ωm. The fabrication of SOI SET started with cleaning the SOI wafer (Figure 9(a)) with acetone and HF to remove both organic contaminants and the native silicon dioxide from the surface. The wafer is rinsed with deionized (DI) water and spun dry. The sheet resistance of the wafer is measured to provide comparative data for calculations. Then, a 30 nm thick silicon oxide (SiO_2) and 40 nm thick amorphous silicon were sequentially deposited on the wafer surface (Figure 9(b)) using Physical Enhanced Chemical Vapor Deposition (PECVD).

A 50 nm thick Polymethyl methacrylate (PMMA) resist is subsequently coated on the amorphous silicon layer for pattern creation (Figure 9(c)). The first mask (Figure 3(a)) is transferred onto the PMMA layer using the e-beam lithography process. After exposure, the wafer is baked at

95°C before dip into developer. Finally, the oxide layer underneath the PMMA is etched anisotropically using high density plasma etcher. The etched layer in the oxide will become the source/ drain and gate of the SET (Figure 9(d)).

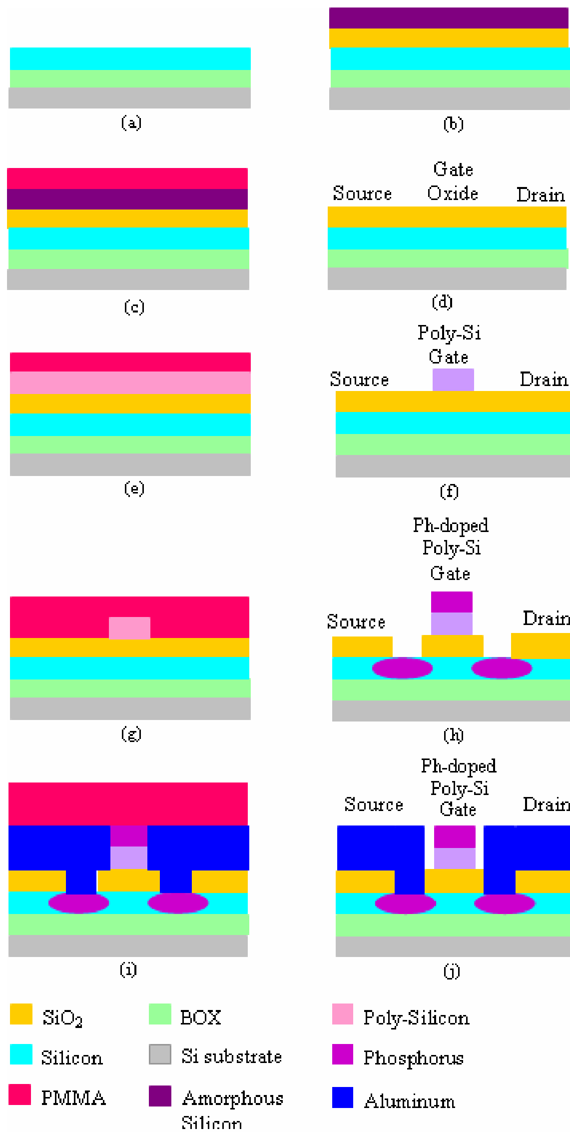


Figure 9. The cross-section illustrating each step of the process. (See text for details.)

After define the source/ drain and gate region, a 60 nm thick Poly-Silicon is then deposited on the gate oxide. Then, the second mask (Figure 4(a)) is transferred on the gate oxide layer using the e-beam lithography process (Figure 9(e)). After etching the unmasked region, the Poly-Silicon gate electrode is formed on the gate oxide layer (Figure 9(f)).

Next, another lithographic step (Figure 9(g)) is used to pattern the oxide layer creating contact holes through which the aluminum probe pads contact the silicon. Once the contacts are opened (Figure 9(h)), a 200 nm aluminum is evaporated onto the entire surface of the wafer using the aluminum PVD module. A final lithographic step (Figure 9(i)) is used to pattern the probe pads and interconnections. Then, the final structure of SOI SET is completed (Figure 9(j)). The three-dimensional image of SOI SET device that we want to produce is shown in Figure 10.

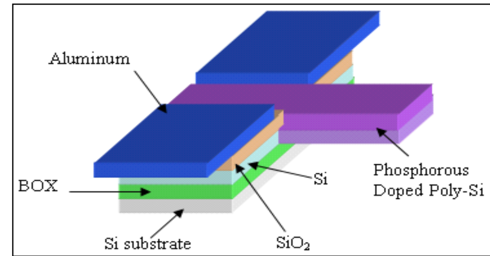


Figure 10. Three-dimensional image of SOI SET.

Ultimately, this project is targeted to produce a SOI SET device with a gate length and gate width of approximately 0.1 μm and 0.020 μm respectively which is currently in progress. Our existing CMOS process coupled with E-beam lithography and high density plasma capability able to make the project target more realistic.

IV. CONCLUSION

The SOI SET device fabrication consists of four masks are source/drain & gate mask, Poly-Si gate electrode mask, contact mask, and metallization mask. The masks were designed using E-Beam GDS II Editor Software. The GDS II is by far the most stable, comprehensive and widely used format for lithography. In addition, the SOI SET device was designed with a gate length and gate width of approximately 0.1μm and 0.02μm respectively is generated for fabrication process. On the other hand, the process flow development for SOI SET device fabrication is completed and the fabrication process of the device is currently in progress.

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