Redesign the 4:2 compressor for partial product reduction

In this paper, we attempt to redesign the 4:2 compressors. Since its inception by Weinberger in 1981[1], this concept of compressor has been used in most digital multiplications and multi operand operation scheme. The original of 4:2 compressor has been build using the full adder unit. Hence this compressor is no improvement compare using Wallace tree or other tree structure. Early 90's some designer has modified the 4:2 compressor in order to reduce the critical path. As a result, a worse case to cross a level of 4:2 compressor is 3 XOR [4]. While in this paper, we have redesign 4:2 compressor based on modification of 4:2 compressor [2, 3, 4]. This design has been simulated using Quartus II software to verify the circuit. As a result, total transistor used in our compressor is less 4 than the modified 4:2 compressor and less 2 transistor than the original 4:2 compressor. In term of speed, the critical path of Carry Out signal is same as the original 4:2 compressor. Our compressor is 0.05% faster than modified 4:2 compressor.