

Design Of 100nm Single-Electron Transistor (SET) By 2D TCAD Simulation

Abstract:

One of the great problems in current large-scale integrated circuits (LSIs) is increasing power dissipation in a small silicon chip. Single-electron transistor (SET) which operate by means of one-by-one electron transfer, small size and consume very low power are suitable for achieving higher levels of integration. In this paper, SET is designed with 100 nm gate length and 10 nm gate width is successfully simulated by Synopsys TCAD. The power of SET device that obtained from simulation is 3.771 times 10^{-9} Watt for fixed current and 3.3565 times 10^{-9} Watt if fixed the gate voltage, V_G , and the capacitance of this device is 0.4297 aF. These results were achieved at room temperature operation.