The Performance Study of Two Genetic Algorithm Approaches for VLSI Macro-Cell Layout Area Optimization

 Abstract:

Very large scale integrated (VLSI) design has been the subject of much research since the early 1980s where the VLSI cell placement emerges to be a crucial stage in the chip design. Its area optimization is very important in order to reduce the delay and include more functionalities to the designed chip. The VLSI cell area optimization continues to become increasingly important to the performance of VLSI design due to the accelerating of the design complexities in VLSI. Thus, this paper addresses the performance comparisons of two different types of genetic algorithm (GA) techniques for VLSI macro-cell layout area optimization by utilizing the adopted method of cell placement that is binary tree method. Two GA approaches which are simple genetic algorithm (SGA) and steady-state genetic algorithm (SSGA) have been implemented and their performances in converging to their global minimums are examined and discussed. The performances of these techniques are tested on Microelectronics Center of North Carolina (MCNC) benchmark circuit's data set. The experimental results demonstrate that both algorithms achieve acceptable area requirement compared to the slicing floorplan approach (Lin et al., 2002). However, SSGA outperforms SGA where it achieves faster convergence rate and obtains more near optimum area.