

Improved booth encoding for reduced area multiplier

In designing high density circuit, size is a major concern in design. This paper presents a simple modification to the Booth Multiplier that can effectively reduce the area with an accepted scarified in speed. A conventional Booth Multiplier consists of Booth Encoder, Partial Product and Summation Tree. Rizalafande[1] introduced new design technique in generating the partial product's row. Meanwhile Hsin-Lei[2] introduced a novel circuit for Booth Encoder/Decoder which claims his design a smaller design. In this propose design, we are still using Rizalafande's architecture but replace the booth encoder with Hsin-Lei encoder. The design was implemented using the FLEX10K EPF 10K70RC240-4 device and Altera MaxPlus+II software.