IMPLEMENTING A LARGE DATA BUS VLIW MICROPROCESSOR

Abstract

Microprocessors have grown tremendously in its computing and data crunching capability since the early days of the invention of a microprocessor. Today, most microprocessors in the market are at 32 bits, while the latest microprocessors from IBM, Intel and AMD are at 64 bits. To further grow the computational capability of a microprocessor, there are two possible paths. One method is to increase the data bus size of the microprocessor to 128/256/512 bits. The larger the data bus size, the more data can be crunched at any one time. The second method is to implement multiple microprocessor core in a single microprocessor unit. For example, Intel's Pentium 4 Dual Core and AMD's Athlon Dual Core both have two microprocessor core within a single microprocessor unit. Latest from Intel and AMD are quad core microprocessors with four microprocessor core within a single microprocessor unit. Both methods have its advantages and disadvantages. Both methods yields different design issues and have different engineering limitations. This research looks into the possibility of implementing a large data bus size VLIW microprocessor core of 256 bits on the data bus. VLIW is chosen as opposed to CISC and RISC due to its ease of scalability.