DESIGN, SIMULATION AND PROCESS DEVELOPMENT FOR SOI SINGLE-ELECTRON TRANSISTOR (SET) FABRICATION

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by

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GLOSSARY OF ABBREVIATION

SET	=	Single-electron transistor
E_C	=	Charging energy (Joule)
C	=	Capacitances (F)
R	=	Resistance (Ohm)
P	=	Power (Watt)
Si	=	Silicon
SiO_2	=	Silicon dioxide
SOI	=	Silicon-on-insulator
V_{TH}	=	Threshold voltage (V)
I_D	=	Drain current (A)
V_G	=	Gate voltage (V)
V_D	=	Drain voltage (V)
T	=	Temperature (K)
e	=	Electron charge (Coulomb)
TCAD	=	Technology computer aided design

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ABSTRAK

Transistor Elektron Tunggal (SET) adalah salah satu daripada nanoteknologi yang berkebolehan dan berbeza dari segi saiz peranti yang sangat kecil dan pembuangan kuasa yang rendah. Tesis ini menerangkan mengenai rekabentuk topeng SET, pembangunan proses aliran SET, dan simulasi proses dan peranti SET. Rekabentuk topeng SET mengandungi empat peringkat topeng iaitu topeng salir dan sumber, topeng get, topeng tingkap, dan topeng logam. Topeng-topeng ini direkabentuk dalam saiz nanometer (10^{-9} m) menggunakan *ELPHY Quantum GDS II Editor Software*. Topeng salir dan sumber dihubungkan dengan dawai nano yang terletak di antara bahagian salir dan sumber. Dawai nano ini direkabentuk dengan 100 nm panjang dan 10 nm lebar. Proses aliran yang mengandungi detail parameter pula dibangunkan untuk simulasi proses dan peranti SET. Proses aliran SET ini mengandungi sepuluh proses modul iaitu proses pembersihan wafer, pemendapan bahan, pembentukan salir/sumber dan dawai nano, pengoksidaan haba, pemendapan *polysilicon*, pembentukan get *polysilicon*, resapan salir/sumber, pembentukan tingkap, pemendapan dan pembentukan logam, dan akhir sekali proses pemanasan dan aloi. Alat simulasi *Synopsys TCAD* telah digunakan untuk melakukan simulasi proses dan peranti SET. Keputusan dari simulasi proses dan peranti menunjukkan bahawa transistor elektron tunggal yang mana dawai nano telah direkabentuk dengan 100 nm panjang dan 10 nm lebar beroperasi pada suhu bilik (300 K) dengan kapasitans adalah 0.4297×10^{-18} F dan tenaga pengecasan adalah 186.4 meV.

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ABSTRACT

Single-electron transistor (SET) is one of the promising nanotechnologies and distinguished by a very small device size and low power dissipation. This project explains the SET mask design, SET process flow development, and SET process and device simulation. The SET mask design consists of four level masks namely source and drain mask, polysilicon gate mask, contact mask, and metal mask. These masks were designed in nanometer (10^{-9} m) size using ELPHY Quantum GDS II Editor Software. The source and drain mask is connected by a nanowire placed between source and drain regions. The nanowire is designed with dimension of approximately 100 nm long and 10 nm wide. The process flow which includes the detailed parameters is developed for SET process and device simulation. This process flow consists of ten process modules include wafer cleaning process, material deposition, source/drain and nanowire formation, thermal oxidation, polysilicon deposition, polysilicon gate formation, source/drain implantation, contact formation, metal deposition and formation, and finally annealing and alloying process. The Synopsys TCAD simulation tools are utilized in SET process and device simulation work. The process and device simulation result shows that the single-electron transistor design with a 100 nm length and 10 nm width of the nanowire is working at room temperature (300 K) operation with a capacitance 0.4297×10^{-18}F and a charging energy 186.4 meV.

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CHAPTER I

INTRODUCTION

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1.1 An Introduction to Semiconductor Devices

Recent advances in deep-submicron complementary metal-oxide semiconductor (CMOS) technologies have made it possible to load a small Silicon (Si) chip with an enormous number of transistors. However, the power consumption of the chip increases due to the increased number of transistors [1, 2]. This will limit the integration scale because the power consumption will go beyond the cooling limit [1].

Gordon Moore, the co-founder of Intel Corporation, noted that the number of transistors on a chip roughly doubled every 18 months [3]. A consequence of this doubling is that the individual feature sizes of the electronic components decreases every year (Figure 1.1). Another consequence of Moore's Law is that as transistors get smaller they contain fewer and fewer electrons.

According to the latest roadmap for the microelectronics industry, chips containing one billion transistors and operating with a clock cycle of a billionth of a second will be on the market just a few years into the new millennium. Christopher Wasshuber, a Texas Instruments (TI) scientist said that, in the next 15 years the industry will reach a point where it can no longer scale metal-oxide semiconductor (MOS) field-effect transistors (FETs) any more [6]. "We'll have to do something different if we want

to continue Moore's Law and continue to shrink these devices and make them cheaper and faster with low power and so on [7]."

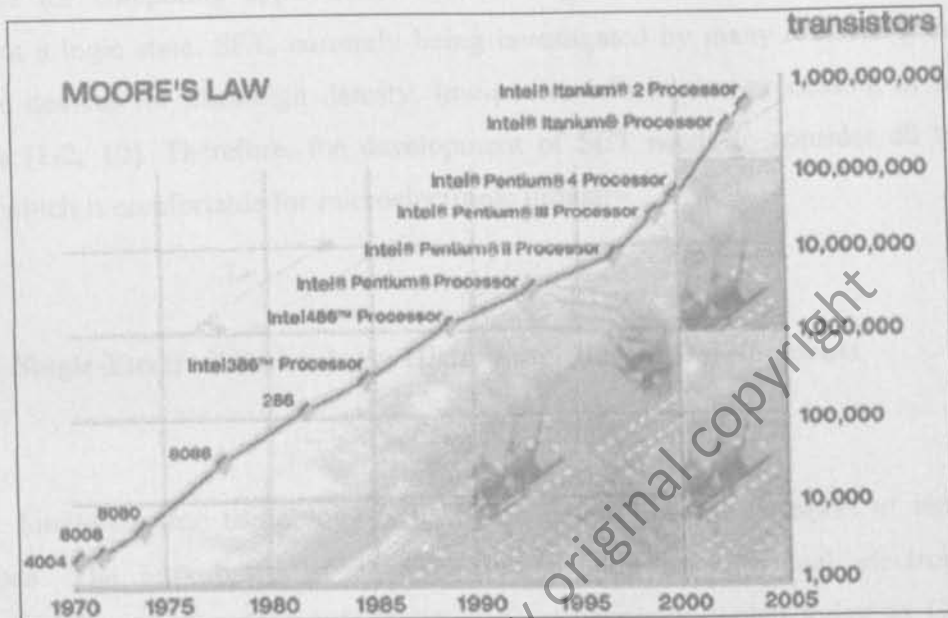

Figure 1.1: An illustration of Moore's Law [4, 5]. The number of the transistors decreases every year.

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Nowadays, single-electron devices (SEDs) [2, 8-9] are believed to be one of the top-candidates to replace standard complementary metal-oxide semiconductor field-effect transistor technology at the end of the conventional semiconductor roadmap. SEDs are drawing a lot of attention for future large-scale integration because of its low-power nature and small size [10].

Among various single-electron devices, the single-electron transistor (SET) [11-15] is the most fundamental. Christopher Wasshuber, a Texas Instruments scientist said that, it is starting to look viable for CMOS to continue to play a major role by providing a traditional system interface to millions of radically smaller, lower power, single electron transistors [16]. The functionality of these transistors (SET) is different and higher than with MOSFET. "I can do more with these than I can with 20 MOSFETs. I can put more functionality into a smaller area for lower power and lower cost," said Wasshuber [6].

In addition, SET is believed to be able to replace standard MOSFETs in the nano scale regime. SET can potentially take the industry all the way to the theoretical limit of electrons for computing applications by allowing the use of a single electron to represent a logic state. SET, currently being investigated by many research groups as possible devices for ultra-high density, low-power information processing or storage systems [1-2, 10]. Therefore, the development of SET needs to consider all type of aspect which is comfortable for microelectronic industry.

1.2 Single-Electron Technology: History and Recent Developments

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Single-electron technology is based on controlling the transport of individual electrons. The importance of charging effects due to individual electrons was recognized in 1951 by Gorter [17]. This phenomenon is known today as Coulomb blockade. In 1987, Likharev had proposed a single-electron transistor (SET) in which the tunneling of electrons can be controlled by a bias applied at the centre electrode [15].

The first SET was experimentally demonstrated by Fulton and Dolan [18] and single-electron charging effects were observed. Dolan [19] developed the double shadow evaporation technique and its variations are untill today the most prevalent ones to manufacture single-electron devices in metallic material systems (mainly Al/ Al_2O_3).

The pioneering work on silicon (Si) SET was done in 1989 by Scott-Thomas *et al* [20, 21], which also reported the first observation of Coulomb blockade oscillation in semiconductors. The observed Coulomb blockade oscillation in conductance was attributed to Si islands unintentionally formed in a narrow one-dimensional channel in a double-gate Si MOSFET.

In 1991, similar characteristics were observed in a double-gate Si MOSFET with a point contact [22]. Before that, in 1990, Meirav *et al* [23] reported on a SET fabricated with a GaAs/AlGaAs two-dimensional electron gas system. The operating temperature

of these early-era SET was below 1 K because the Coulomb blockade islands were not small enough.

Ono *et al* [24] used a technique called pattern dependent oxidation (PADOX) to make a small silicon SET. These SET had junction capacitances of about 1 aF and a charging energy, E_C of 20 meV. Postma *et al* [25] made a SET that operates at room temperature by using an AFM to buckle a metallic carbon nanotube in two places. The total capacitance achievable in this case is also about 1 aF.

Pashkin *et al* [26] fabricated Al/Al_2O_3 SET by means of angled evaporation, a technique that is commonly used for metal SET using e-beam lithography with an aluminum island that had a diameter of only 2 nm. They developed an oxidation process to shrink the island and reported E_C of 115meV, junction capacitance of 0.7 aF and operated at room temperature. Matsumoto *et al* [27] fabricated SET with Ti/TiO_x systems. They employed an atomic-force-microscope (AFM) based oxidation technique to define islands and achieved E_C of a few tens of meV.

A promising way to further reduce the island size is to use a two-dimensional silicon-on-insulator (SOI) layer of separation-by-implanted-oxygen (SIMOX) or bonded wafers, instead of bulk silicon wafers. The use of SOI wafers in SET fabrication was first reported by Ali and Ahmed [28]. In a more recent study, SET operating at room temperature has been fabricated in a process which is compatible with silicon technology [29]. This dissertation reviewing the background of SET, designing of SET masks, SET process flow development, and demonstrate SET process and device simulations.

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1.3 Problems and Parameters

In the past several decades, many companies in Malaysia and also in other parts of the world have been involved in semiconductor industry especially in producing the transistors as the main components for computation and communication. Indeed, these transistors are transferring millions of electrons at a time on single semiconductor chips,

whereas the power consumption of the chip increases as the number of transistor increases [3, 4-5].

Additionally, the current size of circuit components in the conventional microelectronic industry is around 0.13 μm [3]. However, this size is not too small since the current semiconductor technologies are focused towards on device dimensions down to or even below 10 nm. At the end of the semiconductor roadmap, devices with 10 nm gate length should become commercially available.

To overcome this problem, SET's are being investigated by many scientists and researchers. In this research, the development of SET is to help the microelectronic industry to decrease power consumption and device dimensions for the higher devices performance. Basically, SET has only one electron beneath the gate at any given time whereas CMOS transistors still operate with hundreds electrons at any given time underneath the gate [7, 16].

Therefore, the development of SET needs to consider all type of aspects which are comfortable for the microelectronics industry. Meanwhile, the SET structure must be in a nano scale regime (smaller size), low power consumption and also operate at room temperature. These three requirements can be achieved from the SET mask design using ELPHY Quantum GDS II Editor Software and SET process and device simulations using Synopsys TCAD simulation tools. The difficulty of doing the process and device simulations of SET will be taken as a challenge in this project.

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1.4 Research Objectives

This research consists of three main objectives which are:

1. To design a mask for single-electron transistor using ELPHY Quantum GDS II Editor Software.
2. To develop process module for silicon-on-insulator (SOI) single-electron transistor simulation and fabrication.
3. To do process and device simulation using Synopsys TCAD tools.

1.5 Research Scopes

The SET which is being investigated covers the following scopes:

1. Reviewing the theoretical aspects of the single-electron transistor such Coulomb blockade effects and orthodox theory.
2. Designing masks for single-electron transistor namely source and drain mask, polysilicon gate mask, contact mask, and metal mask.
3. Developing and integrating the process modules for single-electron transistor simulation and fabrication which include cleaning, material deposition, source/drain and nanowire formation, thermal oxidation, polysilicon deposition, polysilicon gate formation, source/drain implantation, contact formation, metal deposition and formation, and annealing and alloying process.
4. Performing the process simulation for single-electron transistor to get device structure and device parameter, and device simulation to obtain the device characteristics.

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1.6 Dissertation Outline

A brief outline of the objectives and scopes of this project had been given in the preceding pages. In the following pages, the project is broken down to the chapters as given following this.

In Chapter II, the subject matter of single-electron transistor (SET) is introduced. Here a SET structure and its equivalent circuit, and also operation principle of SET is presented. Then, the theoretical background of SET which is Coulomb blockade effects and orthodox theory is briefly discussed. This chapter ends up with discussion about silicon-on-insulator (SOI) which is utilized as a starting material for SET.

Chapter III discuss on the mask design for single-electron transistor (SET). Explanation on the design methodology using ELPHY Quantum GDSII Editor Software and its result is covered.

Chapter IV explains and describes the process module development of SET prior SOI SET fabrication. This process module will be used for SET simulation (for both process and device) and also for actual SET fabrication.

Chapter V presents the simulation of SET that includes process and device simulation by using the Synopsys TCAD tools. First, the methodology of the experiment is presented and followed by the simulation results which are based on this tool. The Taurus TSUPREM-4 is employed as a process simulator whereas the Taurus Medici is used as a device simulator.

Chapter VI summarizes the overall scope of the project. The suggestion for future developments is also included.

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CHAPTER II

LITERATURE REVIEW

2.1 Introduction

Scaling down of electronic device sizes has been the fundamental strategy for improving the performance of ultra-large-scale integrated circuits (ULSIs). Metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the most prevalent electron devices for ULSI applications, and thus the scaling down of the sizes of MOSFETs [9] has been the basis of the development of the semiconductor industries for the last 30 years.

The most authoritative industrial forecast, the International Technology Roadmap for Semiconductors [30] predicts that this exponential (Moore's Law) progress of silicon MOSFETs and integrated circuits will continue at least for the next 15 years [31].

Figure 2.1 shows predicted features sizes of transistors. Within 15 years, the device size will be on the nanometer order [30]. However, higher levels of integration produce greater power dissipation in a small silicon chip. Even now, the power consumption of some microprocessor chips used in personal computers is more than 50W [32].

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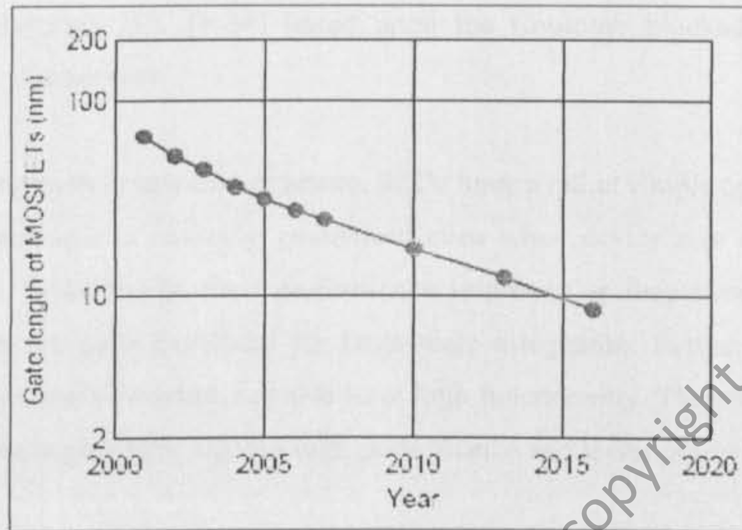

Figure 2.1: Gate length of MOSFETs predicted in International Technology Roadmap for Semiconductors [30].

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Currently, several tentative technologies are investigated in order to overcome the problems arising from scaling device dimensions (transistor gate length L) down to or even below 10 nm [31-35]. Eventually it makes device to be extremely difficult to fabricate and to achieve high performance. Another difficulty in current large-scale integration circuits (LSIs) is increasing power dissipation in a small silicon chip [10].

However, if the minimum feature size is reduced below ~10 nm, quantum mechanical effects such as tunneling affect device performance significantly [14]. The scaling down of devices also leads to a reduction in the number of electrons available for digital switching operations. However, a continuous success in device scaling is necessary for the further development of the semiconductor industries in the coming years.

Especially, single-electron devices (SEDs) [2, 8-9] are believed to be able to replace standard MOSFETs in this nanoscale regime. SEDs is drawing a lot of attention for future large-scale integration because of its low-power nature and small size [10, 32].Besides, SEDs are the key to minimizing power consumption because they can control the transfer

of individual electrons [32, 36-38] based upon the Coulomb blockade effect will be discussed in the next section.

In addition to their low-power nature, SEDs have a rather simple operation principle. The operation principle is basically guaranteed even when device size is reduced to the molecular level. Additionally, their performance improves as they become smaller [2]. These properties are quite beneficial for large-scale integration. Furthermore, SEDs can work not only as simple switches, but also have high functionality. Therefore, these special features should be exploited to achieve high performance and lower power dissipation.

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2.2 Single-Electron Transistor (SET)

"The Smaller We Are, The Better We Perform." That is the siren song of SEDs, in which electrons skip on and off quantum dots or tunnel through barriers thought impenetrable in the world of classical physics [39]. The SEDs are the ultimate low-power consumption device because, as the name implies, they operates on just a single electron based on the Coulomb blockade and quantum size effect [40].

The most fundamental three-terminal SEDs are called single-electron transistor (SET) [12-13, 15]. SET is always three-terminal devices with gate, source, and drain, unlike quantum dots (QDs) and resonant tunneling devices (RTDs) which may be two terminal devices without gates [11]. The SET is expected to be a key device for future extremely large-scale integrated circuits because of its ultra-low power consumption and small size. The schematic structure of SET is shown in Figure 2.2.