U MAP

Characterization of Alignment Mark to Obtain Reliable Alignment Performance in Advanced Lithography

By

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DECLARATION

I hereby declare that the work in this thesis is my own except for quotations and summaries which have been duly acknowledged.

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PENGAKUAN

Saya akui kerja ini adalah hasil kerja saya sendiri kecuali nukilan dan ringkasan yang tiap satunya telah saya nyatakan dengan jelas sumbernya

20 Julai 2006 NORMAH BT AHMAD

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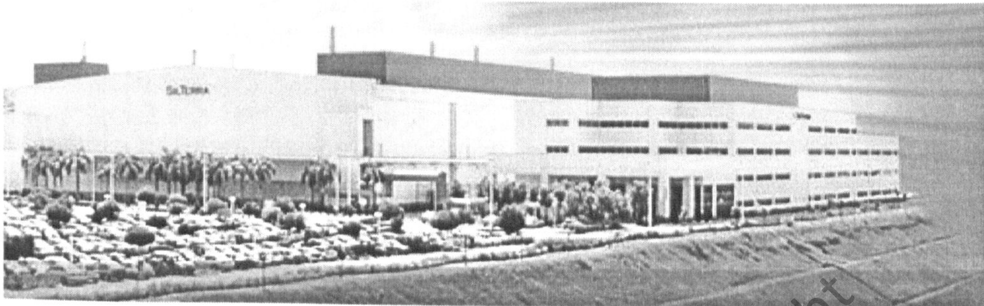
SILTERRA (M) SDN BHD



Silterra (M) Sdn Bhd was founded in November 2005 as Wafer Technology (M) Sdn Bhd. It was renamed as Silterra Malaysia Sdn Bhd in December 1999. It is a project from Malaysia national government to promote front-end semiconductor manufacturing and a catalyst for high technology investment in Malaysia

Its manufacturing facility is situated at Kulim High Technology Park, Kulim Malaysia. It is a SMIF Class 1 mini environment, which utilizes Computer Integrated Manufacturing (CIM) for control of all process equipment. The fab is designed with a maximum capacitiy of 40 thousands wafer per month. It utilize 100% scanner lithography equipment and able to manufacture wafer technology to 0.13mm process technology

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GLOSSARY OF ABBREVIATION

IC	=	Integrated Circuit
CD	=	Compact Disc
PVD	=	Physical Vapor Deposition
CVD	=	Chemical Vapor Deposition
CMP	=	Chemical Mechanical Planarizing
ILD	=	Interlayer Dielectric
IMD	=	Inter Metal Dielectric
DOE	=	Design of Experiment
ATHENA	=	Advanced Technology using High Order Enhanced Alignment
WQ	=	Wafer Quality
MCC	=	Multiple Correlation Coefficient
DS	=	Delta Shift
OA	=	Off Axis
TTL	=	Through-the-lens
BARC	=	Bottom Anti Reflective Coating
C18	=	CMOS18 Process Technology
C13	=	CMOS13 Process Technology
CMOS	=	Complimentary Oxide Semiconductor
WQ	=	Wafer Quality
WWQ	=	Worst Wafer Quality

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LIST OF TECHNICAL DEFINITION

Wafer Quality	=	A ratio signal strength to baseline signal comes directly from alignment mark (%)
Multiple Correlation Coefficient	=	The fit of the measured alignment signal to the baseline signal
Delta Shift	=	Systematic shift between 8.0 micron signal and 8.8 micron signal generated by alignment marks.
Mark Residue	=	How well does each mark fit to the calculated grid
Overlay	=	The difference, O, between the vector position, P1, of a substrate geometry and the vector position of the corresponding point, P2, in an overlaying layer. O = P1-P2

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Abstract (BM)

Pengecilan semikonducktor fabrikasi telah mengetatkan overlai toleran. Toleran yang ketat ini memerlukan prestasi jajaran yang sangat stabil. Tujuan kajian ini dijalankan adalah untuk membentuk satu eksperimen pencirian tanda jajaran yang systematic dan menentukan tanda jajaran yang mantap bagi lapisan via1 dan metal1. Kajian ini meliputi empat aspek iaitu untuk mendapatkan tanda jajaran yang mantap bagi lapisan via1 dan metal1, perbandingan antara tanda jajaran 'via' dan 'metal', perbandingan antara saiz tanda jajaran, dan menilai pretasi tanda jajaran 'metal' yang baru. Untuk mencapai objective ini, sebuah experiment telah dibentuk dengan mengvariasikan ketebalan tungsten, aluminum, lapisan oksida, dan masa 'over polish'. 15 tanda jajaran telah dinilai dalam kajian ini. . Terdapat lima penemuan utama dalam eksperimen ini. B2 dengan 'weighted' score tertinggi (4979 untuk kemampuan analysis dan 75.16 untuk Cpk analysis)adalah tanda jajaran yang terbaik untuk lapisan Metal1. A3 dengan weighted score tertinggi (2173.52 untuk kemampuan analysis dan 2800 untuk Cpk analysis)adalah tanda jajaran yang terbaik untuk lapisan Via1 dalam proses variasi yang telah ditetapkan. Apabila perbandingan dibuat antara tanda jajaran via dan tanda jajaran metal, tanda jajaran via lebih peka kepada proses variasi. Satu lagi penemuan penting adalah tanda jajaran baru 'wall' sesuai digunakan dalam persekitaran pembuatan ini kerana ia menunjukkan signal kualiti yang bertambah baik. Penemuan dalam eksperimen ini telah menjadi dasar kepada penggambaran cirri jajaran utk C18 teknologi dan teknologi yang lebih terkini.

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Abstract (English)

The continued downscaling of semiconductor fabrication has imposed increasingly tighter overlay tolerances. Such tight tolerances will require very high performance in alignment. Hence, the objective of this research to establish characterization process for alignment evaluation and to determine the robust alignment strategy for via 1 and metal 1 masking layers. This research covers four aspects, namely to find robust alignment mark for Metal1 and Via1 layer, alignment performance comparison between via mark and metal mark, alignment mark feature size effect on alignment signal, and to evaluate the new metal alignment mark performance. In order to achieve these objectives, a fractional factorial experiment with 4 parameters variation (tungsten thickness, over polish time, aluminum thickness, and final oxide thickness) and one duplicate was developed. Fifteen alignment mark types were evaluated. Based from the characterization experiment, B2 mark with highest capability score (4979) and weighted Cpk score (75.16) is the most robust alignment mark for Metal1 layer. A3 is the most robust alignment mark for Via 1 layer. A3 mark gives the highest total score in weighted average capability analysis (2173.52) and Cpk analysis (2800). Based on this work, contact mark is more sensitive to process variation as it pattern formation involved 6 processing steps compared to 3 steps for metal mark. For via mark, big mark size (more than 2.6 μm) gives bad alignment signal quality compared to the smaller feature size. Regardless of mark size, alignment signal generates by metal mark gives comparable results. Two types of new metal alignment mark designs (B8 and B9) were evaluated in this experiment. The results were compared with standard metal mark (B6) and standard via mark (B4). B8 gives the best overall alignment and overlay performance since it gives the highest total in weighted average analysis (140.96 (alignment) and 53.43 (overlay)). The research findings becomes a baseline for C18 technology alignment process and already implemented in our production line.

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CHAPTER 1

BACKGROUND

1.1 Introduction

Integrated circuit is one of the important elements in today's world. It can be found in almost every modern electrical device such as cars, television sets, compact disc (CD) players, cellular phones, etc. Before IC was introduced in the 50's, electric circuits were assembled manually by soldering each discrete component and connecting them with wire [31, 32].

However, problems started to rise as the circuit becomes more complicated [33]. The tendency to make even a single faulty connection was increased. Additionally, the connection may not remain intact, which in turn lead to faulty connection. The circuit component size would not be able to shrink to the nano-scale regime. This means that the component size was big and the interconnection wire was very long. It is unadvisable to use long interconnecting wire, as the electric signal couldn't travel fast enough, eventually deteriorating the application performance [31]. Geoffrey W.A.

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