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Built-In Self-Configurable Architecture for Memristor Based Memories

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ABSTRACT

Memristor is an attractive candidate to replace the present computation and storage devices due to its novel features namely nanoscale size, low power, non-volatility, high compatibility with CMOS, and multi-bit operations. However, the memristor memories need to overcome the design challenges such as process variations, non-deterministic switching characteristics, and unreliable operation. This study suggests a built-in self-configurable architecture to detect the weak (unstable) cells of the memristor-based memories. The proposed techniques were validated by "voltage threshold adaptive memristor" (VTEAM) model by injecting various resistive faults. Additionally, this study presents the necessary mathematical analysis for the methodology. The results confirm that the investigated architecture is capable to differentiate unstable and stable memory cell.

Keywords: Built-In Self-Test, Design for Testability, Fault-Tolerance, Memristor, Stability Fault.

1. INTRODUCTION

Memristor (short form of memory resistor) is a fourth fundamental circuit component theoretically proved by Leon Chua in 1971[1] and practically demonstrated by Hewlett Packard Enterprise (HPE) labs in 2008 [2]. Memristor is an attractive candidate to replace the present computation and storage devices due to its novel features namely nanoscale size, low power, non-volatility, tight integration with CMOS, and multi-bit operations [3,4]. However, the memristive devices need to overcome the design challenges such as process variations, non-deterministic switching characteristics, and unreliable operation [5]. The resistance of any memristive device varies between low resistance state (LRS) or ON resistance (R_{on}) and high resistance state (HRS) or OFF resistance (R_{off}) based on the applied bias [6]. Basically the applied voltage or current changes the internal state of the device which in turn controls the resistance of the device. The resistance of the cell reduces when the current flows from the positive terminal to a negative terminal of the memristor, whereas the resistance of the cell rises while the current passes in the reverse direction. Suppose the current is stopped, the device remembers its resistance state. The ability of the memristor to remember its resistance value when the power is off and change its resistance value based on the bias are the key characteristics of the memristor that facilitates the applications such as non-volatile storage[7], digital logic computations, analog applications [8], neuromorphic and in-memory computations, etc. Memristors can be classified into flux controlled devices or charge controlled devices based on input bias [9]. If the bias source is voltage, then the device is assumed as a flux controlled

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device, whereas the charge-controlled devices are biased by current sources. The proposed technique assumes the voltage controlled memristor device for the analysis.

The stability fault mainly occurs due to the presence of open, short, and resistive imperfections present in the memory array, peripheral circuits, as well as interconnects. Presence of open/short/resistive faults makes the memory cell to move into the indeterminate state [10]. The classical method (scan test, March test) of detecting stability faults [11] is a tedious and costlier process for memristor-based memory. These methods operate in a functional mode to catch the stability and data retention faults. Additionally, those tests catch only the faulty cell, but not weak cells. This paper contributes a built-in self-configurable (BISC) architecture to catch the weak cells. This technique uses a design for testability (DFT) circuitry, which applies electrical disturbance to the memory cells such a way that only weak cells gets affected and all other cells expected to tolerate the stress [10][12]. Considering the process variations and non-deterministic nature of the memristive device, the proposed BIST circuit is designed to be configurable in order to adapt itself based on the behaviour of the device. The proposed architecture is more flexible, adaptable, and provides high fault coverage compared with other schemes available in the literature [13]. Moreover, the scheme was validated by a proficient, generic and extendable mathematical model called "Voltage ThrEshold Adaptive Memristor" (VTEAM) [14]. Since the proposed circuit operates in the test mode, there is no additional load or impact on the functional performance of the memory.

2. BACKGROUND

As the memristors are not available commercially, researchers are either using memristor emulator or electrical model to design, analyze, and develop memristor based applications. The first memristor model called linear ion drift model was developed by HP in 2008[2]. This model assumes that the memristor has a linear relationship between the input voltage and the internal state of the device. But the actual device shows the nonlinear relationship between the voltage and internal state. Since linear ion drift model has no threshold, the memristance of the device changes for any small change in voltage/current. Additionally, this model assumes that the oxygen vacancies have the liberty to travel around the whole length of the device, but actually the oxygen vacancies cannot move till the boundary of the device due to the presence of undoped region. Therefore, various new memristor models namely non-linear ion drift model, Simmons tunneling barrier model, "ThrEshold Adaptive Memristor model"[15] (TEAM) and VTEAM have proposed to address the nonlinearity and boundary problems. The TEAM and VTEAM model considered as a simple, generic and efficient model due to (1) its adaptability to fit any other model of the memristor, (2) no change in the device state below the threshold value, (3) polynomial relationship between the input bias and internal state of the device. TEAM model assumes that the device internal state is controlled by current while the VTEAM model adopts voltage as the controlling variable. The VTEAM model offers better accuracy (<1.5% relative root-mean-square error) as compared with other existing models. The parameters of the VTEAM model includes undoped region boundary specifications (*a_on* - upper bound of undoped region and *a_off* - lower bound of undoped region), threshold specifications (*v_on* - ON threshold voltage and *v_off* - OFF threshold voltage), non-linearity factors (*k_on* and *k_off*), and power coefficient non-linearity factors (*alpha_on* and *alpha_off*).

Weak cell detection scheme presented in Ravi and Prabaharan [13] is an extended work of weak write mode based stability test schemes [16] demonstrated for SRAM memories. The scheme [13] suggests three design for testability (DFT) techniques namely low write voltage (LWV), short write time (SWT) and short refresh time (SRT) to find the undefined state cells in the resistive random access memory. The proposed schemes determine the optimum strength and length of the write pulse based on the available pre-fabrication specifications. The memristor

memory write driver is configured to provide the fixed weak write pulse to catch the unstable cells. Hence, it cannot be modified after the fabrication of the chip in order to adapt with the process, voltage and temperature (PVT) variations of the chip. Therefore, the fixed pulse weak cell detection approach may provide over stress or under stress to the device which results in missing-out the unstable cells. So, this study herewith presented an improved built-in-self-configurable memristor memory architecture which offers improved performance with high fault coverage.

2.1 Defects, Fault and Fault Modeling

Defect is undesired deviation of the implemented hardware from the actual design, whereas the term fault indicates the functional abstracted representation of one or more defects. On the other hand, fault modeling is the electrical equivalent representation of one or more faults. In the memristor-based memories the term SET indicates the process of changing the resistance of the memristor from HRS to LRS and RESET denotes the process of altering the resistance from LRS to HRS. Figure 1 presents the symbol, SET and RESET operation of the memristor.

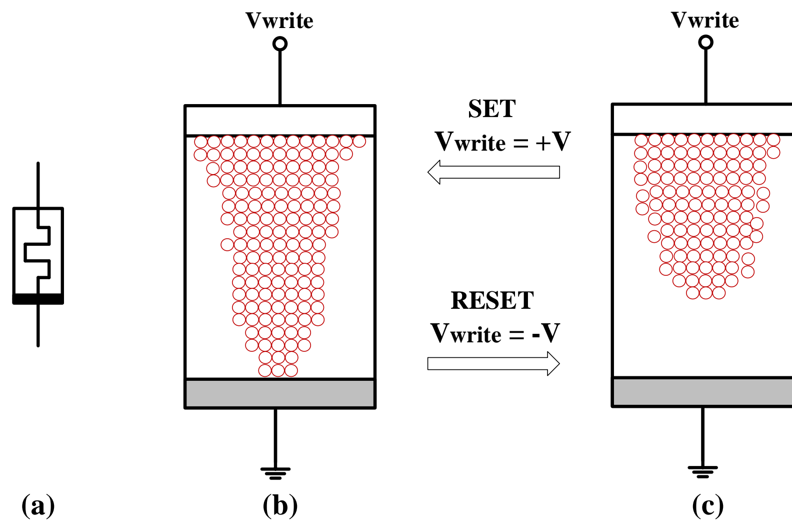


Figure 1. (a) Memristor symbol, (b) Memristor state at LRS, (c) Memristor state at HRS.

Most common intrinsic defects of memristive devices are variations in material characteristics, fabrication parameters, and size of the device [17][18]. On the contrary, the common extrinsic defects are electrical damages induced by peripheral circuits [19][20] and defects in nano vias that connect memristive structure and other devices. Table 1 lists some of the potential defects of the memristive devices and the corresponding fault models. Fault analysis shows that most of the defects ultimately influence the effective ON/OFF resistance of the memristor. Therefore, the fault tolerance of any memristive applications can be tested by varying R_{on} and R_{off} values of the device. The normalized width [9] is defined as the ratio of actual width to the total thickness of the device (w/D). The logic state of the device can be computed from the value of the normalized width. Generally, 0 to 0.4 is considered as logic-0, 0.6 to 0.8 is considered as logic-1, and 0.6 to 0.8 is treated as undefined state. Figure 2 presents the normalized width variations for the fault-free write logic-1 and read logic-1 operations while Figure 3 shows the fault-free write logic-0 and read logic-0 operations. Figure 4 illustrates the variations of memristance for faulty cell along with good cell.

Table 1 Memristor memory cell defect types and the respective fault modeling

Defect Type	Fault Modeling
Variation in size	variable resistance connected in series/parallel with memristor Variation in ON and OFF resistance
Variation in doping concentration	stuck-at-1 fault stuck-at-0 fault variable resistance connected in series/parallel with memristor Variation in ON and OFF resistance Variation in SET and RESET time
Variation in material Characteristics	Variation in ON and OFF resistance
Missing interconnects	open circuit (R = ∞)
Broken interconnects	variable resistance
Redundant interconnects	short circuit (R = 0)
Peripheral induced defects	Variation in ON and OFF resistance Variation in SET and RESET time

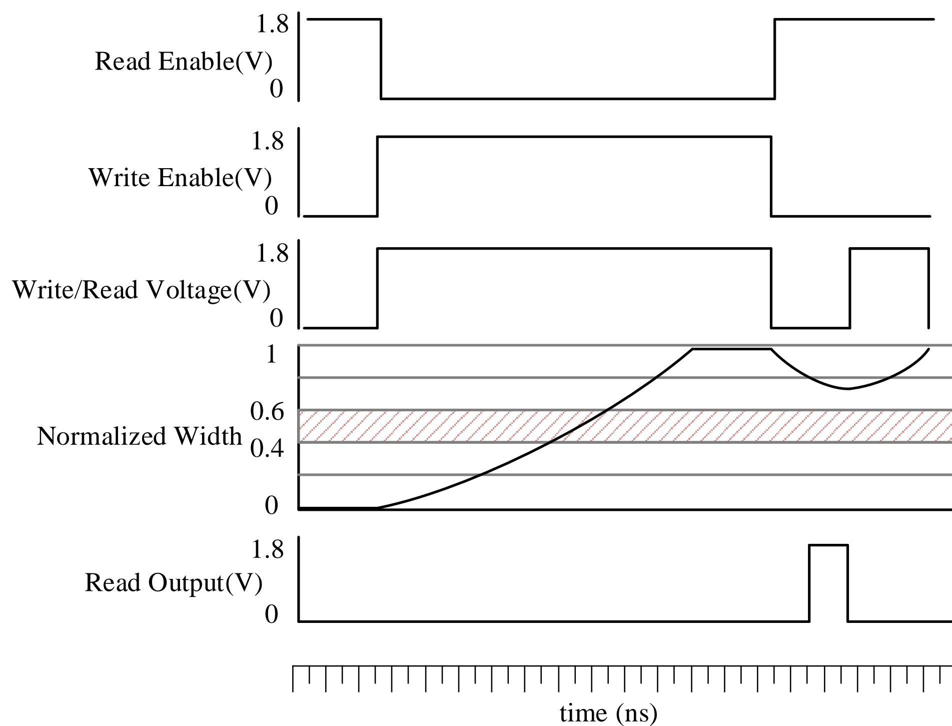


Figure 2. Fault- free write logic-1 and read logic-1 operations. The normalized width varies between 0 to1 and the region between 0.4 to 0.6 is assumed as an undefined state.

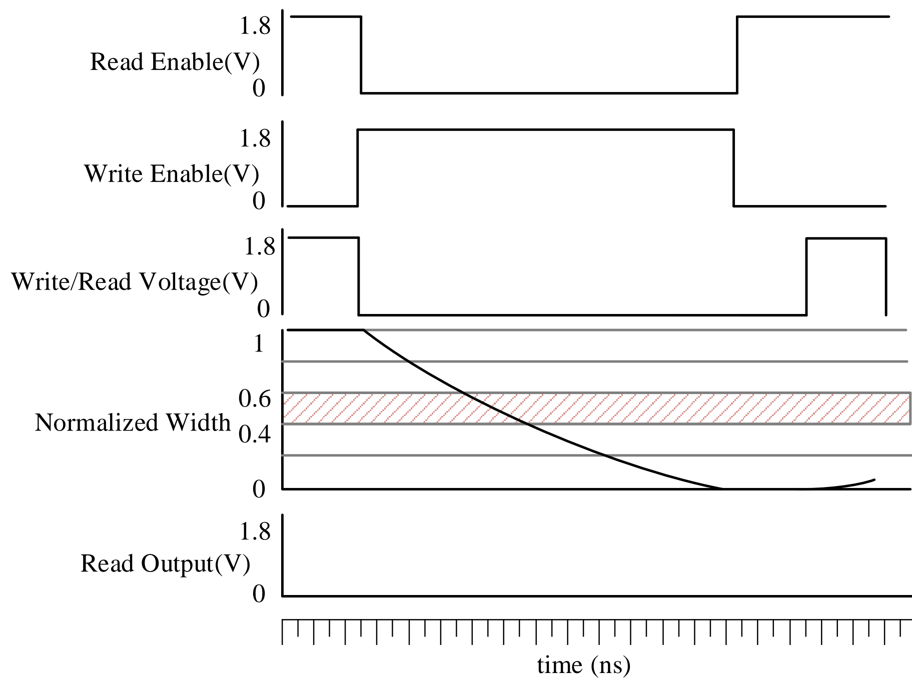


Figure 3. Fault- free write logic-0 and read logic-0 operations. The normalized width varies between 0 to1 and the region between 0.4 to 0.6 is assumed as an undefined state.

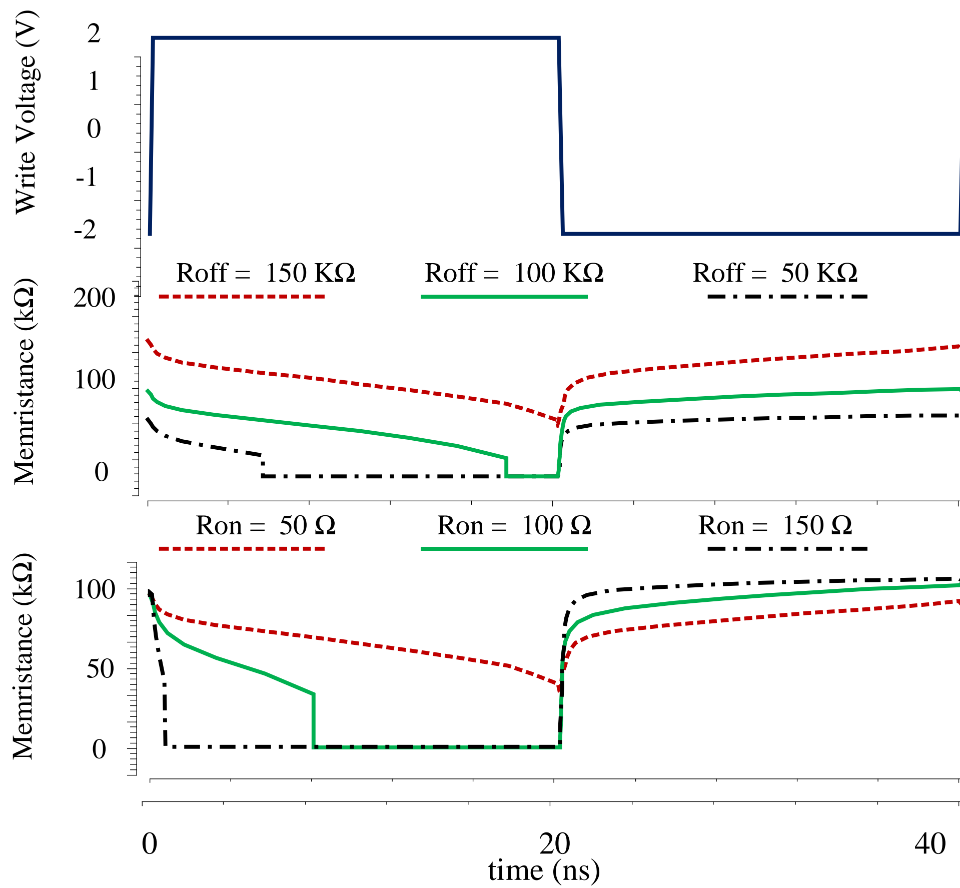


Figure 4. Variations of memristance against the write voltage (±2V) for various R_{on} and R_{off} values.

2.2 Proposed Built–In Self-Configurable Architecture

The proposed Built-In Self-Configurable (BISC) architecture is shown in Figure 5. The suggested architecture uses either low write voltage or short write time based on the configuration setting to find the unstable cells of the memory. The flow chart of the sequence of operations is presented in Figure 6. As the BISC block is operating in the test mode, there is no disruption (such as delay, power dissipation) on the function mode of the memory. Since the amplitude of the pulse, as well as the width of the pulse affects the memristance of the cell, the electrical stress signal can be generated by varying any one or both parameters of the pulse.

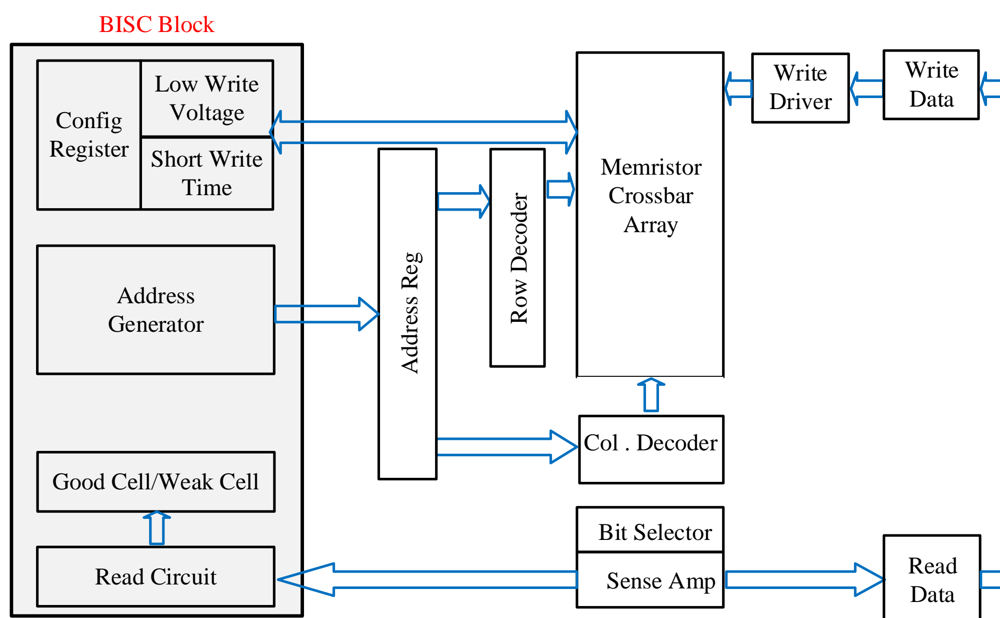


Figure 5. Memristor memory architecture includes the proposed Built-in self-configure block.

2.3 Low Write Voltage (LWV)

The "low write voltage" (LWV) technique attempts to recognize the unstable cells by reducing the amplitude of the write pulse from its typical value while keeping the width of the pulse unchanged. Therefore, the cell under test may not get sufficient bias to toggle its state. Nevertheless, if the device was hitherto in the indeterminate region (weak cell) then the write pulse with low amplitude can change the internal state of the device from intermediate state to defined state such as logic-1/logic-0. As shown in the flow chart Figure 6, a random cell is selected from the memory array to conduct the test. The selected cell has been subjected to the normal write-read routine in order to confirm that the cell is not a faulty cell. Suppose the cell passes the normal read-write operations, then the weak cell detection technique is activated to check the stability of the cell. The width of the low write voltage should be the same as that of the normal write pulse, whereas the amplitude needs to be carefully selected to have the right distinction between the weak cells and good cells. On the application of low write voltage to the cell under test, if the state of the cell is flipped, then the cell is considered as a weak cell otherwise assumed as a good cell. Simple voltage divider circuit with the appropriate timer is sufficient to generate the low write voltage signal. It is a well-known fact that the memristor shows a lot of process variations across the chips, the idea of applying a fixed amount of stress may not work well for all the chips. Hence, it is a need to have Configurable amount of stress and the respective threshold values in order to accurately differentiate the weak cells from good cells. The weak cell detection techniques can be extended from pre-fabrication verification to post-fabrication validation. Figure 7 shows the configurable BIST methodology and the corresponding modified write driver circuit to accommodate the weak write operation.

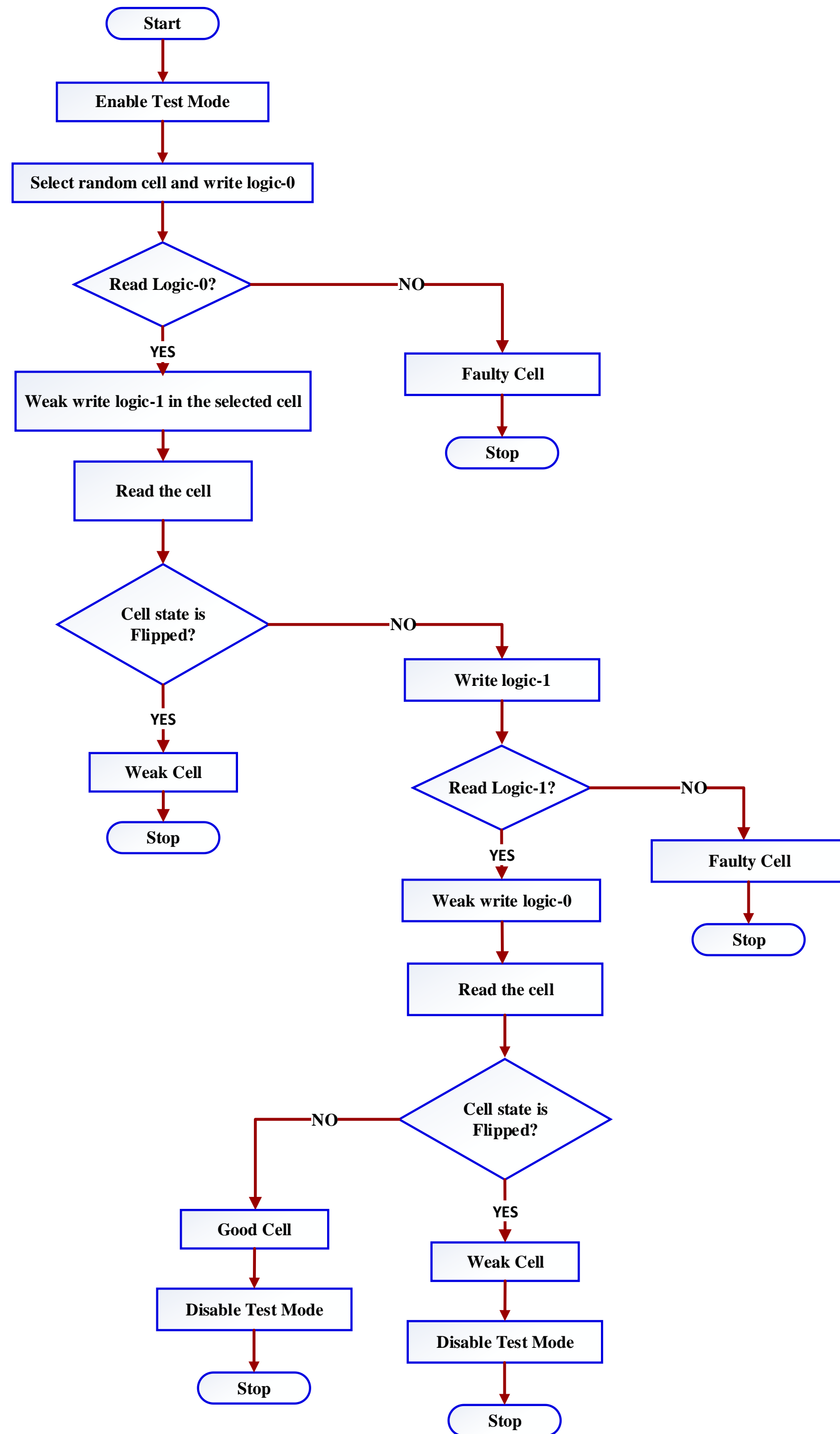


Figure 6. Flow to illustrate the step by step procedure to differentiate good, weak and faulty cells.

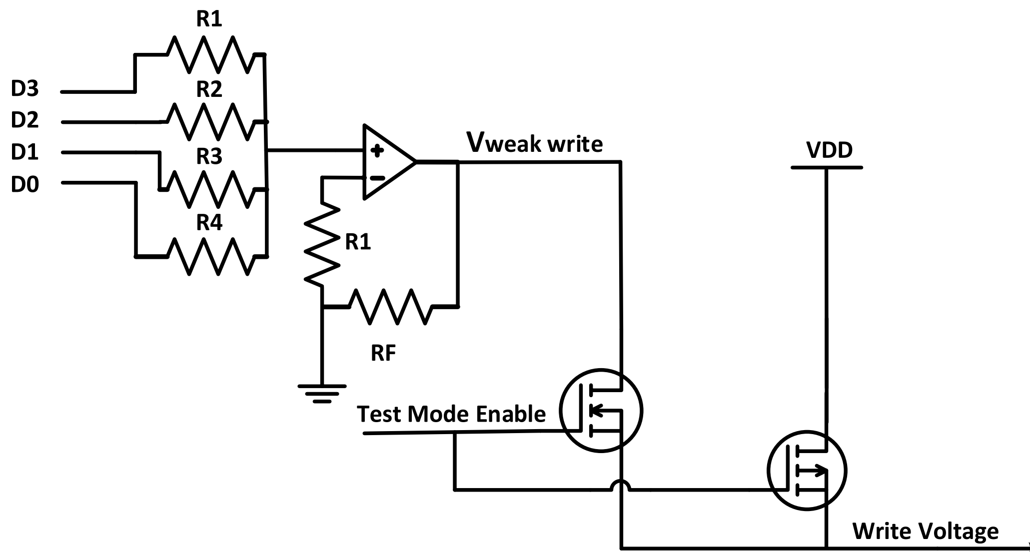


Figure 7. Write driver integrated configurable weak write circuit to perform low write voltage test.

The circuit generates the normal write pulse during the functional mode whereas the weak voltage is generated during the test mode. The circuit accepts the configurable digital inputs (D3 to D1) and produces the equivalent analog signal which will act as weak write voltage for the considered test sequence.

The memristance of the device defined by VTEAM model is given as in Equation 1.

$$m(t) = [R_{on} + \frac{R_{off}-R_{on}}{w_{off}-w_{on}} (w - w_{on})] \quad (1)$$

Here w is the state of the memristor at any point of time t, w_{on} is the internal state of the memory cell at the extreme conductive region (R_{on}) and w_{off} is the state of the device at extreme resistive region (R_{off}).

The voltage and current in the memristor at any point of time are written in Equation 2.

$$v(t) = m(t) * i(t) \quad (2)$$

Memristors can be classified into flux controlled devices or charge controlled devices based on the input bias. If the bias source is voltage, then the device is assumed as a flux controlled device (or voltage controlled), whereas the charge-controlled (current controlled) devices are biased by current sources. The proposed technique assumes the voltage controlled memristor device for the analysis.

In the case of low write voltage technique, the duration of the write bias V_{width} is fixed, but the strength of the write voltage is reduced from the normal value to the level where it can differentiate the weak cells and good cells.

The pulse-width of the write voltage during the sweep operation can be written as in Equation 3.

$$V_{LWV} = V_{Write} - V_{\Delta Write} \quad (3)$$

Where

V_{LWV} – Derived low write voltage to be applied for the cell under test
V_{write} – Amplitude of the normal write pulse or typical write voltage
$V_{\Delta Write}$ – Amount of voltage to be reduced from the write voltage

Then the rate of change of the memristor internal state (w) for the given input voltage (V_{LWV}) is given by Chua [1]

$$\frac{dw}{dt} = \frac{\mu_v . R_{on}}{D} * i(t) \quad (4)$$

Where μ_v is the average ion mobility. Rewriting the above equation in terms of resistance ratio β (R_{off}/R_{on}) as Equation 5.

$$\frac{dw}{dt} = \frac{\mu_v . V_{LWV}}{D\beta - w(t).(\beta-1)} \quad (5)$$

Simplifying the equation [] for the internal state of the memristor at any point of time is given in Equation 6.

$$w(t) = \frac{D\beta}{\beta-1}\left[1 - \sqrt{\left(1 - \frac{D\beta}{\beta-1} w_0\right)^2 - \frac{2\mu_v (\beta-1)}{(D\beta)^2} \Phi(t)}\right] \quad (6)$$

w_0 is the initial state of the device. Therefore, the state of the cell at any point of time is directly related to the flux passed through the device.

The write voltage V_{LWV} and the flux Φ (t) are related by Equation 7.

$$\Phi(t) = \int_0^t V_{LWV}(t)\, dt \quad (7)$$

Since the flux controlled memristor is considered, the normalized width (w(t)/D) at any point of time during the test is shown in Equation 8.

$$\frac{w(t)}{D} = \frac{\beta}{\beta-1}\left[1 - \sqrt{\left(\frac{m(w_0)}{R_{off}}\right)^2 - \frac{\Phi(t)}{\Phi_D}}\right], \Phi_{Min} < \Phi < \Phi_{Max} \quad (8)$$

$$\frac{w(t)}{D} = 1, \ \Phi \geq \Phi_{Max}$$
$$\frac{w(t)}{D} = 0, \ \Phi \leq \Phi_{Min}$$

Where

$$\Phi_{Min} = -\frac{\Phi_D}{R_{off}^2}(R_{off}^2 - m(w_o)^2)$$
$$\Phi_{Max} = \frac{\Phi_D}{R_{off}^2}(m(w_o)^2 - R_{on}^2)$$

$$\Phi_D = \frac{(D\beta)^2}{2\mu_v(\beta-1)}$$

The memristance of the cell is included in Equation 9.

$$m(t) = R_{off}\sqrt{\left(\frac{m(w_0)}{R_{off}}\right)^2 - \frac{\Phi}{\Phi_D}} \quad (9)$$

The flux across the memristor for the write voltage of amplitude V_{LWV} and width T_{write} is given

in Equation 10 and Equation 11.

As discussed in the last section, to perform successful write the amplitude of the write pulse should be as in Equation 10. :

$$V_{write} = \frac{\Phi(t)}{T_{write}{R_{off}}^2} * \left(R_{off}^2 - R_{on}^2\right) \quad (10)$$

When low write voltage is applied, the internal state of the memristor moves from w_0 to w, the Equation 11 is used.

$$V_{LWV} = \frac{\Phi(t)}{T_{write}{R_{off}}^2} * \left((m(\omega_0))^2 - (m(\omega))^2\right) \quad (11)$$

2.4 Short Write Time (SWT)

Short write time (SWT) is an alternative method to identify the weak cells. This method utilizes a short pulse width write pulse to catch the unstable cells. Again the good cells may not get enough bias to toggle the state, but the weak cells may switch state for the selected short pulse. Figure 8 illustrates the circuit diagram for the short write time weak cell detection technique with a configurable pulse width. The configuration data (D3 to D1) has been loaded from the configuration register. This digital is converted into equivalent analog data by the digital to analog converter (DAC) circuit. The analog signal obtained from the DAC circuit has been utilized to modulate the width of the write pulse by pulse width modulator (PWM) circuit. The mode selection circuitry used to select the appropriate mode of operation (normal mode/functional mode). Considering the process variations and other external disturbances, the circuit is designed to provide a configurable amount of stress to efficiently classify the good and weak cells.

The pulse-width of the write voltage during the sweep operation can be written as Equation 12.

$$V_{SWT} = V_{width} - V_{\Delta width} \quad (12)$$

Where

V_{SWT} – Derived write voltage with short write time to be applied for the cell under test
V_{width} –Write voltage with a typical pulse width
$V_{\Delta width}$ – Amount of pulse width to be reduced from the write voltage
Then the rate of change internal state (w) for the given write voltage (V_{SWT}) is given by Chua [1]

$$\frac{dw}{dt} = \frac{\mu_v . R_{on}}{D} * i(t) \quad (13)$$

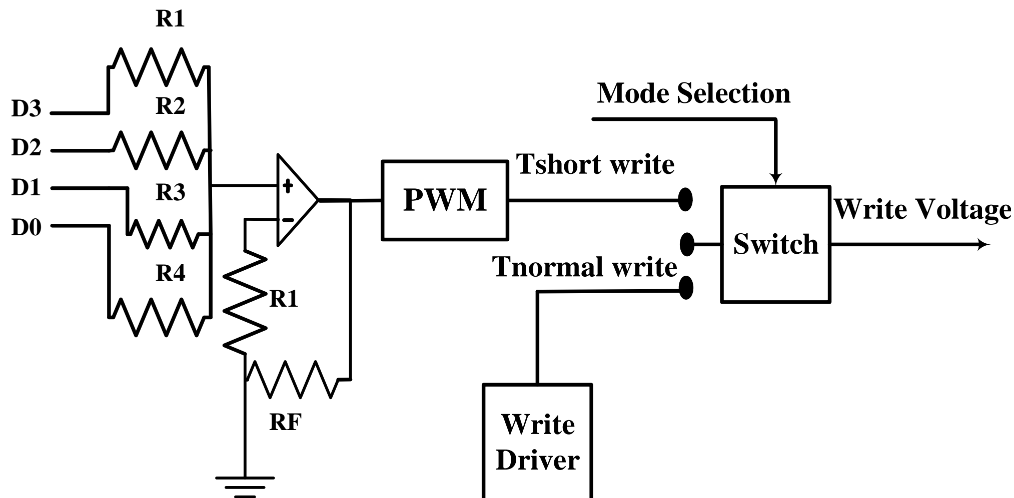


Figure 8. Write driver integrated configurable weak write circuit to perform short write time test.

Where μ_v is the average ion mobility. Rewriting Equation 13 in terms of resistance ratio β (R_{off}/R_{on}), Equation 14 is formed.

$$\frac{dw}{dt} = \frac{\mu_v . V_{SWT}}{D\beta - w(t).(\beta - 1)} \tag{14}$$

The write voltage V_{SWT} and the flux Φ (t) are related by:

$$\Phi\,(t) = \int_0^t V_{SWT}(t)\,dt$$

As discussed in the last section, to perform successful write the amplitude of the write pulse should be as in Equation 15.

$$V_{write} = \frac{\Phi(t)}{T_{write} {R_{off}}^2} * \left(R_{off}^2 - R_{on}^2\right) \tag{15}$$

When we apply low write voltage the internal state of the memristor moves from w_0 to w, Equation 17 is used.

$$V_{LWV} = \frac{\Phi(t)}{T_{write} {R_{off}}^2} * \left((m(\omega_0))^2 - (m(\omega))^2\right) \tag{16}$$

Suppose the write duration is reduced, then the cell may not get sufficient bias to toggle its state.

3. SIMULATION AND DISCUSSION

The built-in self-configurable scheme with the proposed weak cell detection methods was simulated using Cadence Virtuoso® (schematic editor and spectre) tools. The performance of the proposed scheme was evaluated using one of the most efficient and generic model of the memristor called VTEAM [14] with the parameter values [21] as device thickness (D) = 3 nm ON resistance = 100Ω, and OFF resistance = 100kΩ with Biolek window function [22]. Few resistive defects (100Ω, 5kΩ, 10kΩ, 15kΩ, 20kΩ, 30kΩ, and 40kΩ) were considered to validate the effectiveness of the proposed schemes. Figure 9 shows the output waveforms of the fault-free switching characteristics of the good cell. It confirms that the write bias is good enough to toggle the normalized width of the cell between 0 and 1. The selected memristor model requires write

pulse amplitude of ±1.8V and pulse width of 4nS to perform successful write-1/ write-0 operations.

Figure 10 presents the output waveforms of the low write voltage scheme for the assumed faults. The write voltage is reduced (0.8V) from the typical value (1.8V). The cells with s with series resistance values R_s = 100Ω, R_s = 10KΩ, and R_s = 20kΩ could able to retain the state while the remaining cells flip the state due to the applied stress. Conversely, Figure 11 illustrates the results of weak write-0. The amplitude selected for the weak write-0 scheme was -0.8V. The test result indicates that the cells with resistive defects (10kΩ, 15kΩ and 20kΩ) were not able to tolerate the stress and hence flip its present state.

Figure 12 and Figure 13 present the results of short write time operations. This test uses fixed amplitude (±1.8V) while the width of the pulse is reduced from 4nS to 2nS to determine the cells with stability faults.

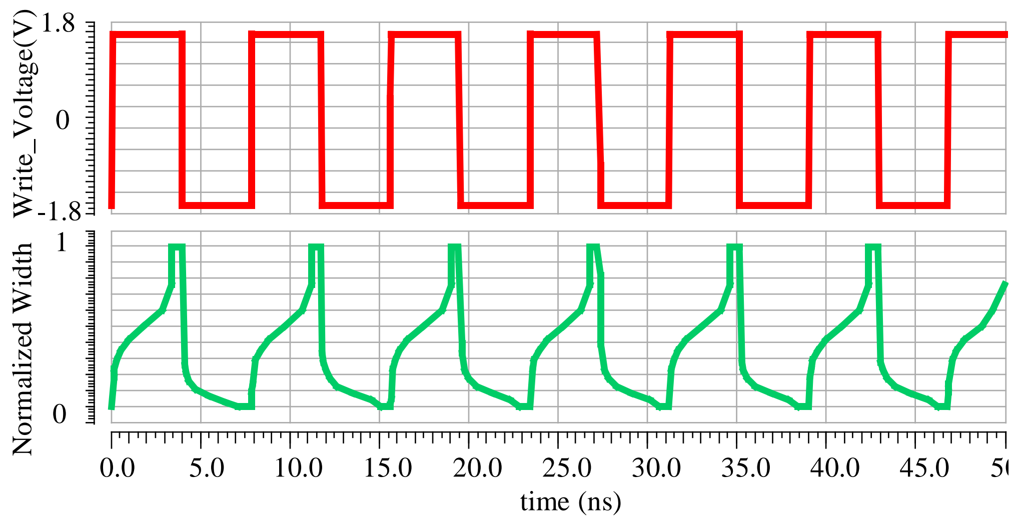
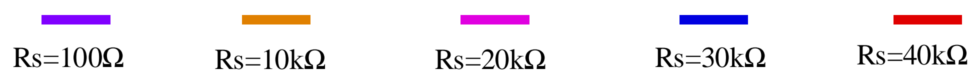


Figure 9. Fault-free write-1 and write-0 operation for the VTEAM memristor cell.



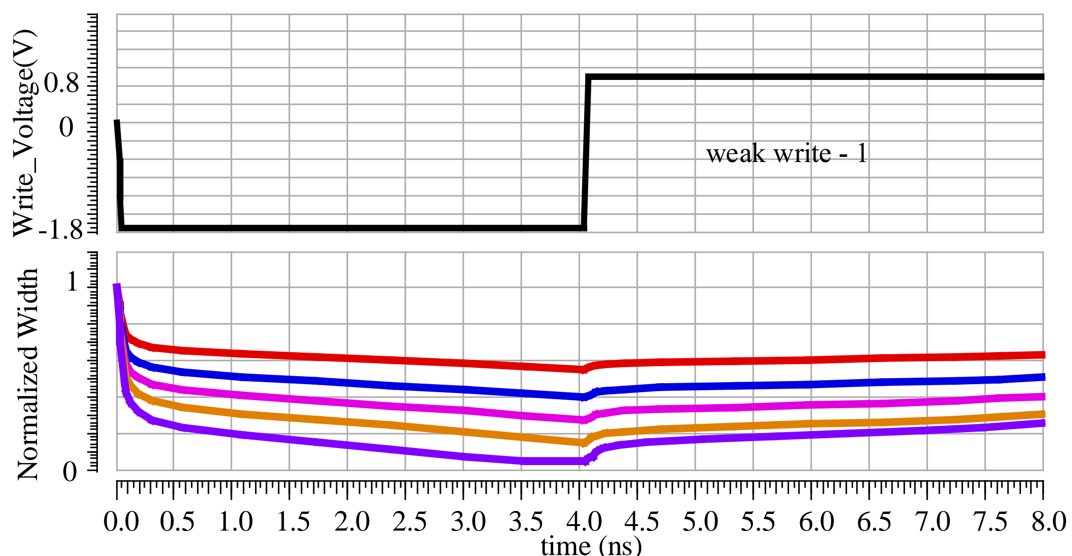


Figure 10. Normal write-0 followed by weak write-1 and the outputs for various resistive defects.

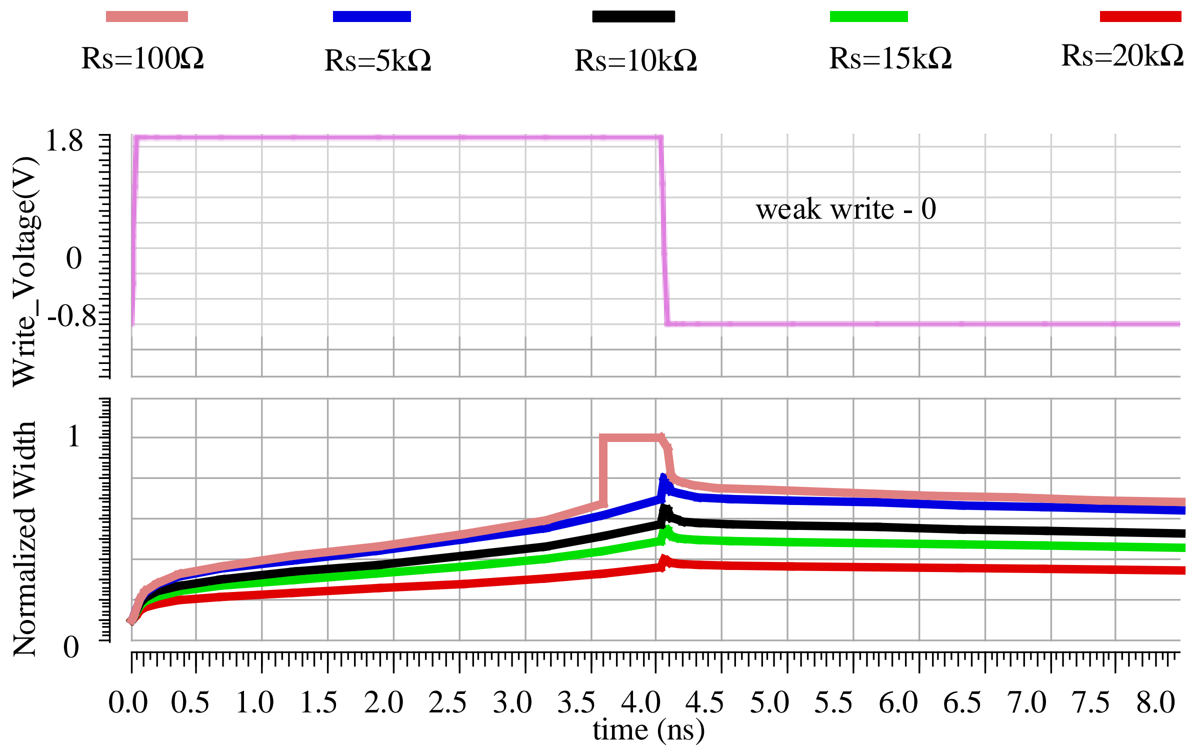


Figure 11. Normal write-1 followed by weak write-0 and the outputs for various resistive defects.

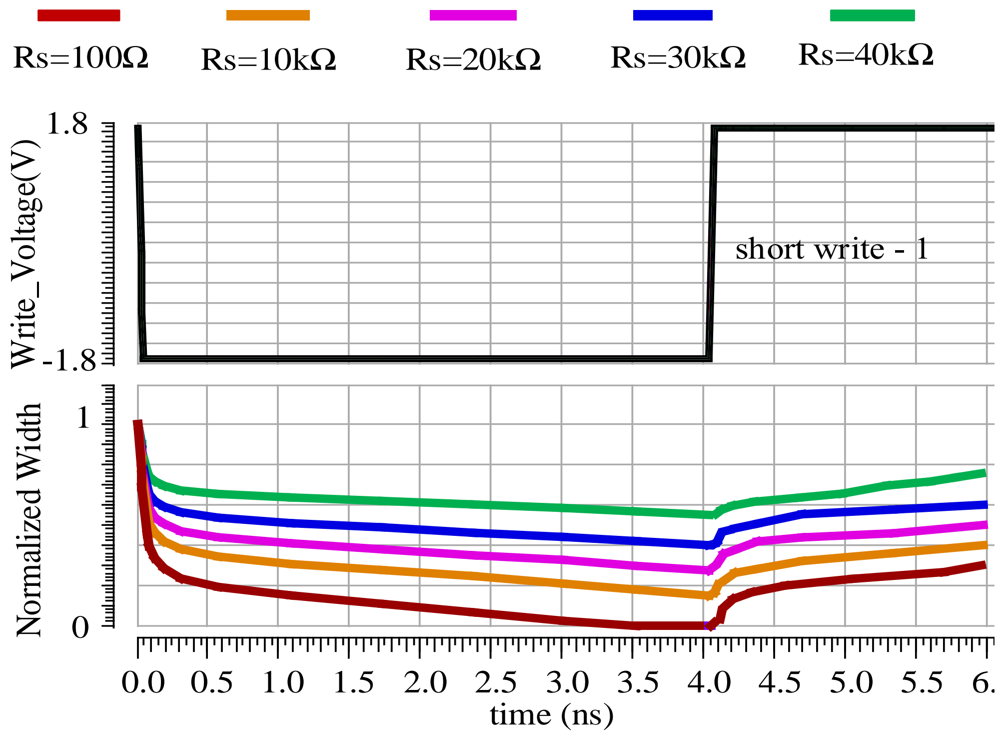


Figure 12. Normal write-0 followed by short write-0 and the outputs for various resistive defects.

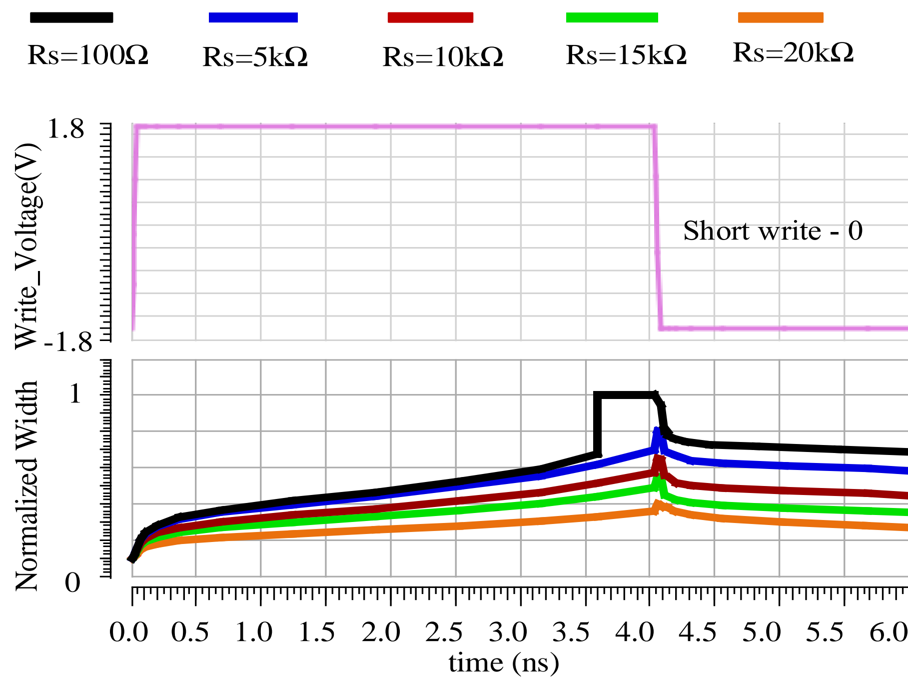


Figure 13. Normal write-1 followed by short write-0 and the outputs for various resistive defects.

3.1 Comparison of Proposed Scheme Against the Weak Cell Detection Scheme in[13]

This section presents the comparison between the existing weak cell detection scheme [13] with the proposed scheme for memristor-based memories. Table 2 presents the comparison results for the selected criteria. The proposed memristor memory architecture includes both functional mode as well as test mode building blocks in order to provide the feasibility of the design. The scheme in Ravi and Prabaharan [13] determines the weak cells by applying fixed electrical stress, so it may not catch all the weak cells under PVT variations. But the proposed BISC architecture uses 4-bit configuration register which can be loaded through a boundary scan chain with an appropriate value according to the PVT variations. Thus, the 4-bit configuration register allows setting 32 different stress levels which include 16 amplitude variations and 16 pulse width variations. Therefore, the suggested scheme provides better fault coverage against the fixed pulse scheme. Since the proposed scheme was validated with generic VTEAM model, the scheme can be extended to any resistive random access memory with minimal changes.

Table 2 Comparison of proposed built-in self-configurable weak cell detection scheme against the scheme

Criteria	Scheme[13]	Proposed
Techniques	LWV, SWT, SRT	LWV, SWT
Memristor Model	Linear ion drift (low accuracy)	VTEAM (Sufficient accuracy, efficient and adaptable)
Fault Coverage	100Ω < Rs < 10kΩ	100Ω < Rs < 40kΩ
Electrical stress	Fixed	4 bit configuration register – 32 different stress (16 amplitude variations + 16 width variations)
Scheme validation	No	Parametric analysis
Mathematical Analysis	No	Yes
Memory architecture	Functional mode only	Functional and test mode

4. CONCLUSION

This research work explores an alternative built-in self–configurable architecture to find the unstable cells of the memristor memory. As the proposed methodology was validated with generic VTEAM model, it can be quickly adapted to any other model selected for the memristor. The parametric analysis results indicate that the techniques are good enough to differentiate weak and good cells. The proposed schemes may act as a possible tool for quickly assessing the behaviour of the memory cells and help to improve the reliability of the memristor based memories. This research work can be extended to cover the weak cells in the multi-level memristor memory.

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